VP2128

2A, 18V, Synchronous-Rectified Buck Converter

Description

The VP2128 is an efficiency and low-cost buck converter with integrated low $R_{DS(ON)}$ high-side 150mΩ and low-side 130mΩ MOSFET switches. It is capable of delivering 2A output current over a wide range of supplying voltage from 4.5V to 18V. With a simple voltage divider, the output voltage is easily adjustable from 0.922V to 16V.

Other features such as programmable soft-start, integrated Boot-Diode, total fault-free protection and 93% conversion efficiency at 5V/1A output make VP2128 ideally to be used in portable consumer electronics.

The VP2128 is available in popular SO-8P green package with exposed pad.

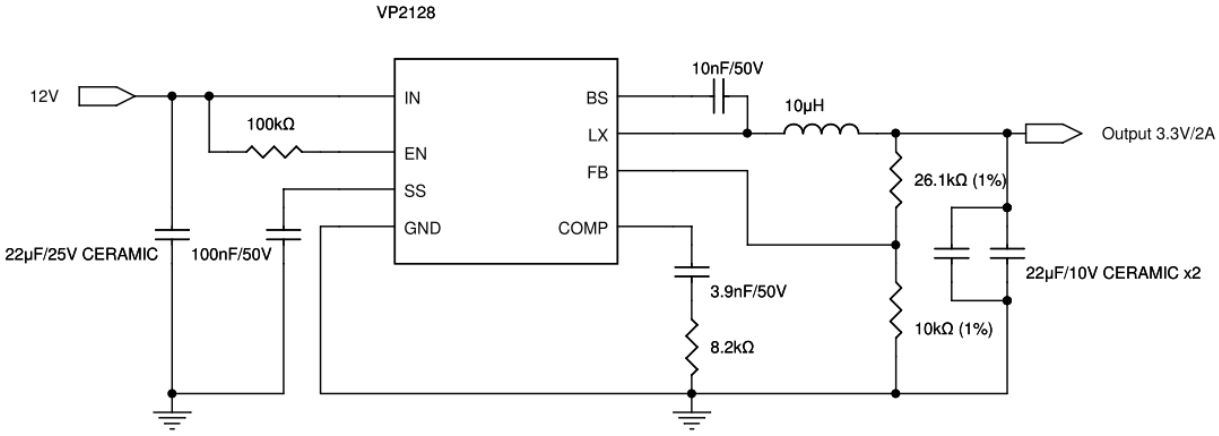
Features

- 4.5V to 18V Input Voltage Range
- Adjustable Output from 0.922V to 16V
- 2A Output Current
- Integrated 150mΩ/130mΩ MOSFET Switches
- 0.922V Voltage Reference with 2% Accuracy
- 93% Conversion Efficiency at 5V/1A Output
- Adapted Current Mode PWM Operation
- Fixed 340kHz Switching Frequency
- Integrated Boot-Diode
- Programmable Soft-Start Function
- Over Voltage and Under Voltage Protection
- Over Temperature and Over Current Limitation
- RoHS 2.0 compliant SO-8P Green Package with Exposed Pad

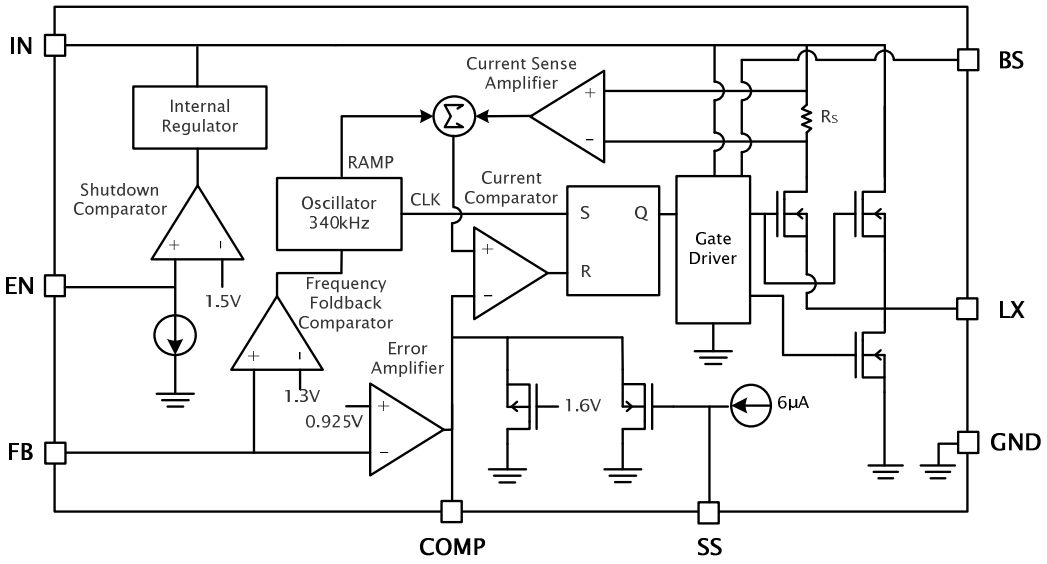
Applications

- Set-Up Box
- Networking Device
- MID/Netbook/Pad-Device
- LCD Monitor/ LCD TV

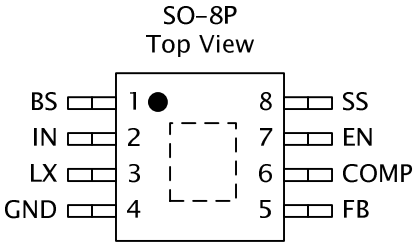
Typical Application



Functional Block Diagram



Pin Assignments And Descriptions



Pin No.	Pin	I/O/P	Function Description
1	BS	-	High-Side N Channel MOSFET Gate drive boost input. Connect at least 10nF capacitor from LX to BS to control the High-Side switch. Place the capacitor close to this pin if possible.
2	IN	P	Power Input. Drive IN with a 4.5V to 18V power source to activate the converter.
3	LX	O	Power Switching Output. LX is the switching node that supplies power to the output.
4	GND	P	Power ground.
5	FB	I	Feedback Input. FB monitors the output voltage to regulate that voltage. Use a voltage divider feedback from the output to drive FB pin.
6	COMP	-	Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND to compensate the regulation control loop. In some cases, an additional capacitor from COMP to GND is also permitted.

Pin No.	Pin	I/O/P	Function Description
7	EN	I	Chip Enable. Pull EN high to enable the converter, pull it low to turn it off. Pull up with a 100kΩ resistor to start it up automatically.
8	SS	-	Soft-Start Control. SS controls the soft-start time. A 100nF capacitor sets the soft-start time to 15ms typically. Leave it floating would make soft-start time become very short.

Absolutely Maximum Ratings

Over operating free-air temperature range, unless otherwise specified (* 1)

Symbol	Parameter	Limit	Unit
V_{IN}	Supply voltage range	-0.3 to 20	V
V_{LX}	Switch voltage range	-1 to V_{IN}+0.3	V
V_{BS}	High side gate drive voltage range	V_{LX}-0.3 to V_{LX}+6	V
V_{IN}(COMP, EN, FB, SS)	Low voltage input range	-0.3 to 6	V
T_J	Operating junction temperature range	-40 to +160	°C
T_{STG}	Storage temperature range	-65 to 150	°C
Electrostatic discharge	Human body model	±2	kV
Electrostatic discharge	Machine model	±200	V
θ_{JC}	Thermal Resistance (Junction to Case)	10	°C/W
θ_{JA}	Thermal Resistance (Junction to Air)	50	°C/W

(*1): Stress beyond those listed at “absolute maximum rating” table may cause permanent damage to the device. These are stress rating ONLY. For functional operation are strongly recommend follow up “recommended operation conditions” table.

Recommended Operating Conditions

Symbol	Parameter	Specification		Unit
		Min	Max	
V_{IN}	Supply voltage	4.5	18	V
V_{OUT}	Output voltage	0.922	16	V
T_A	Operating free-air temperature range	-40	85	°C

Electrical Characteristics

T_A = 25℃, V_{IN} = 12V (unless otherwise noted)

Symbol	Parameter	Test Condition	Specification			Unit
			Min	Typ	Max	
I_{SD}	Shutdown supply current	V_{EN}=0V		20		μA
I_Q	Supply current	V_{EN}=2.0V, Non-Switching		1.3		mA
V_{UVLO}	Under voltage lockout		3.8	4.1	4.4	V
V_{REF}	Reference voltage	4.5V≤V_{IN}≤18V	0.904	0.922	0.94	V
$R_{DS(ON)H}$	High-Side switch $R_{DS(ON)}$			150		mΩ
$R_{DS(ON)L}$	Low-Side switch $R_{DS(ON)}$			130		mΩ
I_{LKH}	High-Switch leakage current	V_{EN}=0V, V_{LX}=0V			1	μA
	Current limit			4.1		A
A_{EA}	Error amplifier voltage gain			480		V/V
G_{EA}	Error amplifier transconductance	△I_C=±10μA		800		μA/V
G_{CS}	COMP to current sense transconductance			4		A/V
f_{OSC}	Oscillation frequency			340		kHz
f_{OSC-SH}	Short circuit oscillation frequency	V_{FB}=0V		100		kHz
D_{MAX}	Maximum duty cycle	V_{FB}=0.8V		90		%
$t_{ON(min)}$	Minimum ON time			200		ns
	EN shutdown threshold voltage	V_{EN} rising		1.5		V
	EN input low current			0.1		μA
	Soft-Start time	C_{SS}=100nF		15		ms
	Thermal shutdown threshold			160		°C
	Thermal shutdown hysteresis			20		°C

Typical Characteristics

V_{IN}=12V, V_{OUT}=3.3V, Inductor=10μH, C_{IN}=10μF, C_{OUT}=22μF, T_A=25℃, unless otherwise noted.

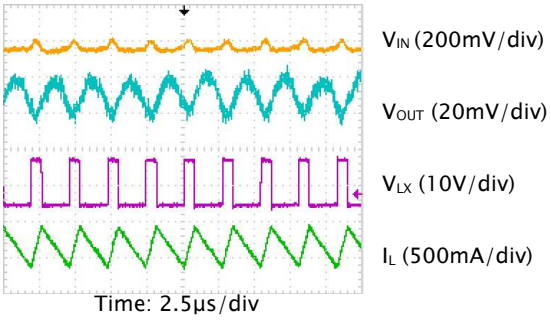


Figure 1. Steady State Operation

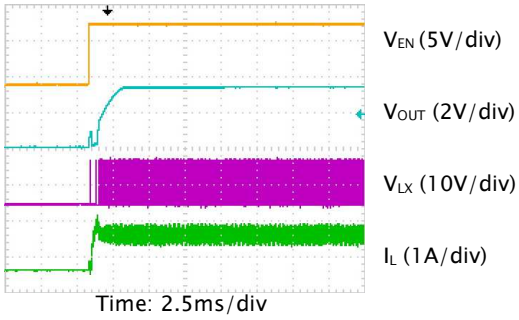


Figure 2. Start-Up Through Enable

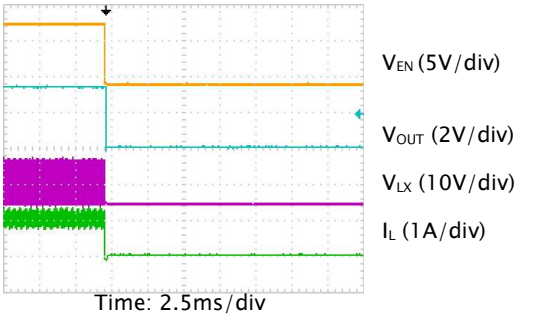


Figure 3. Shutdown Through Enable

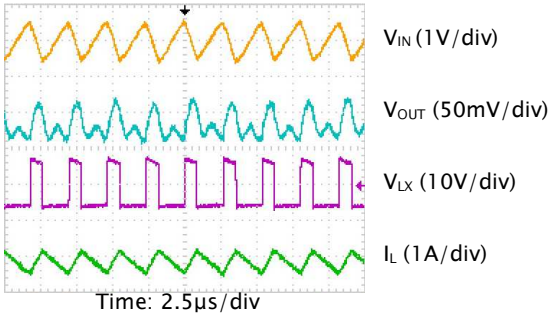


Figure 4. Heavy Load (2A) Operation

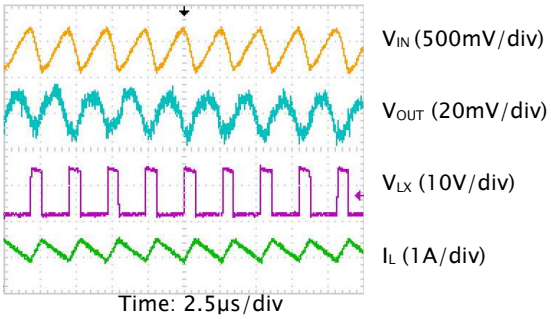


Figure 5. Medium Load (1A) Operation

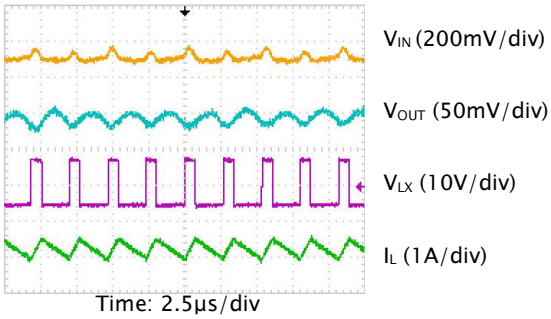


Figure 6. Light Load (no load) Operation

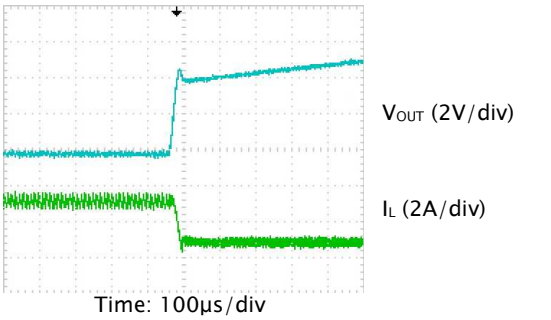


Figure 7. Heavy Load (2A) Short Circuit Recovery

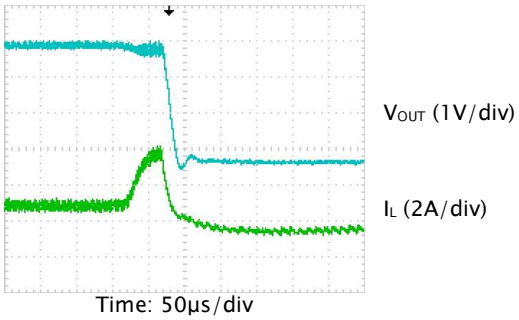


Figure 8. Heavy Load (2A) Short Circuit Protection

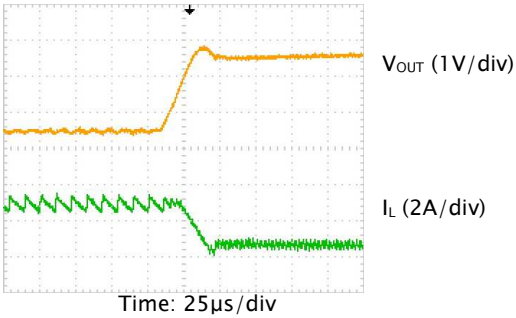


Figure 9. Light Load (no load) Short Circuit Recovery

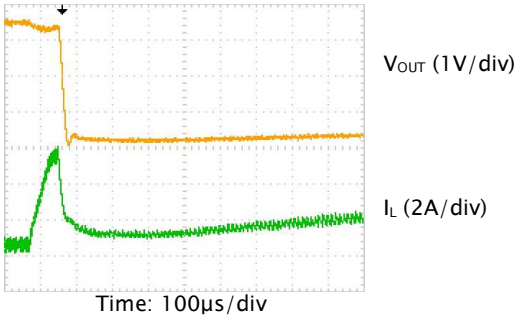


Figure 10. Light Load (no load) Short Circuit Protection

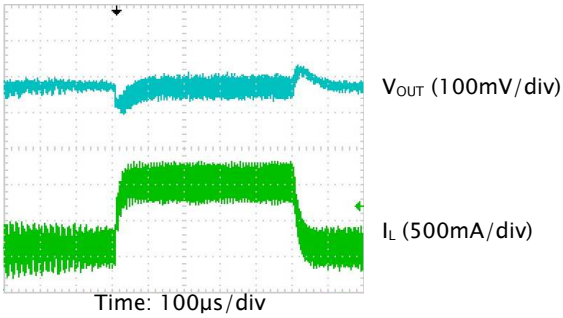


Figure 11. Load Transient

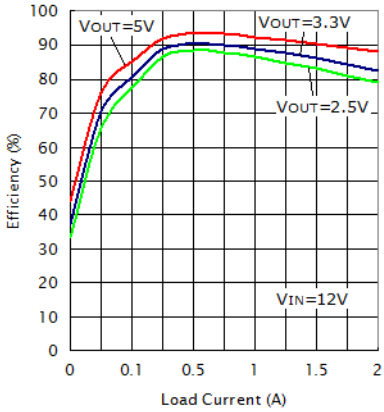


Figure 12. Efficiency

Application Information

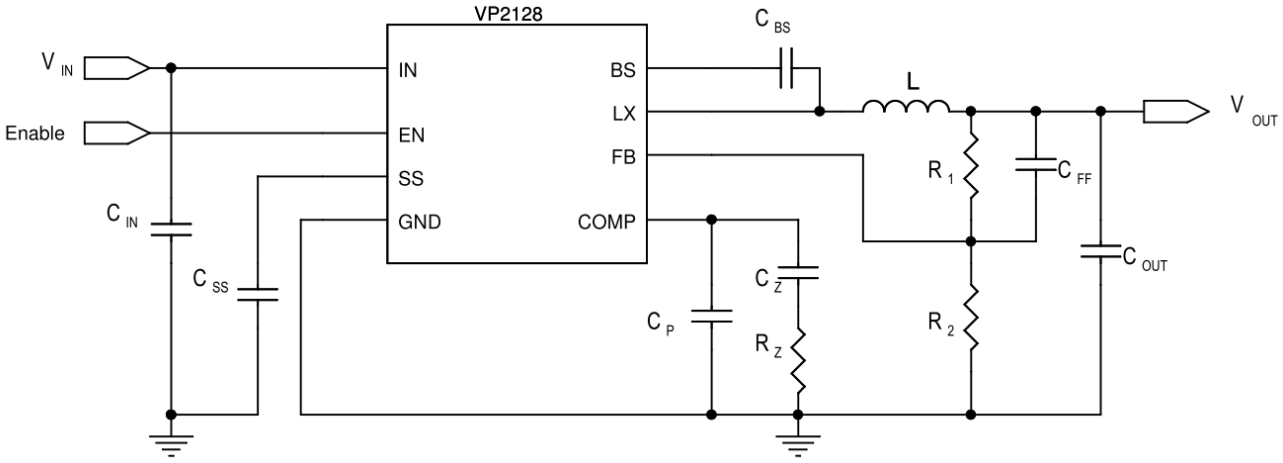


Figure 13. VP2128 typical application

Input Supply Voltage

V_{IN} supplies current to internal control circuits and output voltages. The supply voltage range is from 4.5V to 18V. A power on reset (POR) continuously monitors the input supply voltage. The buck converter draws pulsed current with sharp edges each time the upper switch turns on, resulting in voltage ripples and spikes at supply input. A minimum 22μF ceramic capacitor with shortest PCB trace is highly recommended for bypassing the supply input.

Output Voltage

The output voltage can be set by the resistor network connected to the output voltage terminal and FB pin. The resistor network divides the output voltage down to the feedback voltage by the follow ratio:

$$V_{FB} = V_{OUT} \frac{R_2}{R_1 + R_2}$$

where V_{FB} is the feedback voltage, V_{OUT} is the output voltage.

Thus the output voltage can be obtained by the following equation:

$$V_{OUT} = 0.922 \frac{R_1 + R_2}{R_2}$$

V_{IN} \ V_{OUT}	1.2V	1.8V	2.5V	3.3V	5V	9V
9V	L:3.3μH R_1:3kΩ R_2:10kΩ	L:3.3μH R_1:9.53kΩ R_2:10kΩ	L:6.8μH R_1:16.9kΩ R_2:10kΩ	L:10μH R_1:26.1kΩ R_2:10kΩ	L:15μH R_1:45.3kΩ R_2:10kΩ	
12V	L:3.3μH R_1:3kΩ R_2:10kΩ	L:3.3μH R_1:9.53kΩ R_2:10kΩ	L:6.8μH R_1:16.9kΩ R_2:10kΩ	L:10μH R_1:26.1kΩ R_2:10kΩ	L:15μH R_1:45.3kΩ R_2:10kΩ	L:15μH R_1:59kΩ R_2:6.8kΩ

Table 1. R1/R2 Ratio vs. Output voltage

Applying the feed-forward capacitor (C_{FF}) could improve the frequency jitter of the output PWM waveform caused by the improper layout criteria. With good layout the capacitor should not be added. If the value of C_{FF} is too large (>1nF), this capacitor will be almost transparent for lower frequency of spikes from output voltage and these noise could disturb the operation of the internal gate driver. The value of C_{FF} shall be lower than 1nF.

Soft-Start

The VP2128 features programmable soft-start function to avoid the in-rush current from supply input. Soft-start capacitor shall be connected to SS pin as capacitor C_{SS} shown in Figure 13. Once the converter exits UVLO state or shutdown mode, such scheme will ramp up the output voltage slowly. It can be used to program the output voltage ramp speed by changing the value of the capacitor. For one 100nF soft-start capacitor, the soft-start period is 15ms typically.

Input Under Voltage Lockout

When the VP2128 is powered on and EN pin is also held high, the internal circuit will remain inactive until V_{IN} exceeds the input UVLO threshold voltage. This function assures the converter works properly and protects the internal gate driver away from entering any unexpected state.

Short Circuit Protection

Once the output is shorted to ground, the protection circuit will be activated and the oscillation frequency will be reduced to lower frequency around 100kHz to prevent the inductor current increasing beyond the current limit. The PWM frequency will be back to its typical value 340kHz after the short condition is removed.

Over Temperature Protection

The VP2128 integrates the circuits to protect itself away from overheating. When junction temperature of the output driver reaches to threshold point like 160℃, the converter will enter the shutdown state and LX pin would be high impedance. The converter will resume only when the driver junction temperature drops more than 20℃ from overheating threshold temperature.

Loop Compensation

The VP2128 employs current mode control to simplify the compensation and improve transient response. The loop stability and transient response are controlled through the COMP pin. The COMP pin is the output of the internal transconductance error amplifier.

Select the appropriate compensation value by following procedure:

1. Calculate the R_Z value with the following equation:

$$R_Z < \frac{2\pi \times C_{OUT} \times 0.1 \times f}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}}$$

2. Calculate the C_Z value with the following equation:

$$C_Z < \frac{4}{2\pi \times R_Z \times 0.1 \times f}$$

3. Determine if the second compensation capacitor C_P is required. It is required if the ESR zero of the output capacitor is located at less than half of the switching frequency, or the following relationship holds:

$$\frac{1}{2\pi \times C_Z \times R_{ESR}} < \frac{f}{2}$$

Then, the value of C_P can be calculated with the following equation:

$$C_P = \frac{C_Z \times R_{ESR}}{R_Z}$$

Determining R_Z and C_Z could be tedious steps. To simplify the calculation, a quick reference table contains R_Z and C_Z is listed below on Table 2. Although the factor of layout style is not considered, this table could be general to approach the optimal compensation network.

V_{OUT}	1.2V	1.8V	2.5V	3.3V	5V	9V
R_Z	3kΩ	3kΩ	6.8kΩ	8.2kΩ	13kΩ	26.1kΩ
C_Z	3.9nF	3.9nF	3.9nF	3.9nF	3.9nF	3.9nF

Table 2. Recommended value of R_Z and C_Z

Inductor Selection

The value of the inductor affects the ripples of output voltage and must be carefully selected. In the same working condition, larger inductance value results in lower output ripple voltage but such inductor will be oversized, higher series resistance and lower saturation current. In most cases, it would be a good rule to keep peak-to-peak switching current ΔI_L to

be approximate 30% of the maximum switching current. And it is necessary to assure the peak inductor current is under maximum switch current limit. Thus, the inductance can be calculated by the following equation.

$$L = \frac{V_{OUT}}{f \times \Delta I_L}(1 - \frac{V_{OUT}}{V_{IN}})$$

where f is the switch frequency, L is the inductance.

Hence the maximum peak current limit of the inductor $I_{L(PEAK)}$ can be obtained.

$$I_{L(PEAK)} = I_{LOAD} + \Delta I_L = \frac{V_{OUT}}{2f \times L}(1 - \frac{V_{OUT}}{V_{IN}})$$

where I_{LOAD} is the maximum load current.

With the equations listed above, the inductance of inductor can be calculated easily. Actually, the selection of the inductor is the compromise of the cost, size and desired electro-magnetic compatibility.

Input Capacitor (C_{IN}) Selection

The VP2128 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor about 22μF is recommended for the decoupling capacitor. An additional 0.1μF speed-up capacitor near pin 2 to ground is good to provide additional high noise filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

Output Capacitor (C_{OUT}) Selection

The output capacitor is required to stabilize the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. If non-Low ESR electrolytic capacitors are used, limit the total value of the C_{OUT} lower than 470μF. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{I_{LOAD}}{f \times L}(1 - \frac{V_{OUT}}{V_{IN}})(R_{ESR} + \frac{1}{8 \times f \times C_{OUT}})$$

Where C_{OUT} is the output capacitance value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f^2 \times L \times C_{OUT}}(1 - \frac{V_{OUT}}{V_{IN}})$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f \times L}(1 - \frac{V_{OUT}}{V_{IN}})R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The VP2128 can be optimized for a wide range of capacitance and ESR values.

Boot-Strap Capacitor Selection

A 10nF ceramic capacitor must be connected between the BS pin to LX pin for proper operation. It is recommended to use a ceramic capacitor.

PCB Layout Guidelines

1. Keep the input switching current loop as small as possible.
2. Keep the LX pin as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions.
3. Keep analog and non-switching components away from switching components.
4. Do not allow switching current to flow under the device.
5. Output capacitor should be connected to a broad pattern of the GND.
6. Voltage feedback loop should be as short as possible, and preferably with ground shield.
7. Extra via is preferable for IN, LX and GND connection.
8. C_{IN} /C_{OUT} should be placed as near as possible to the device.

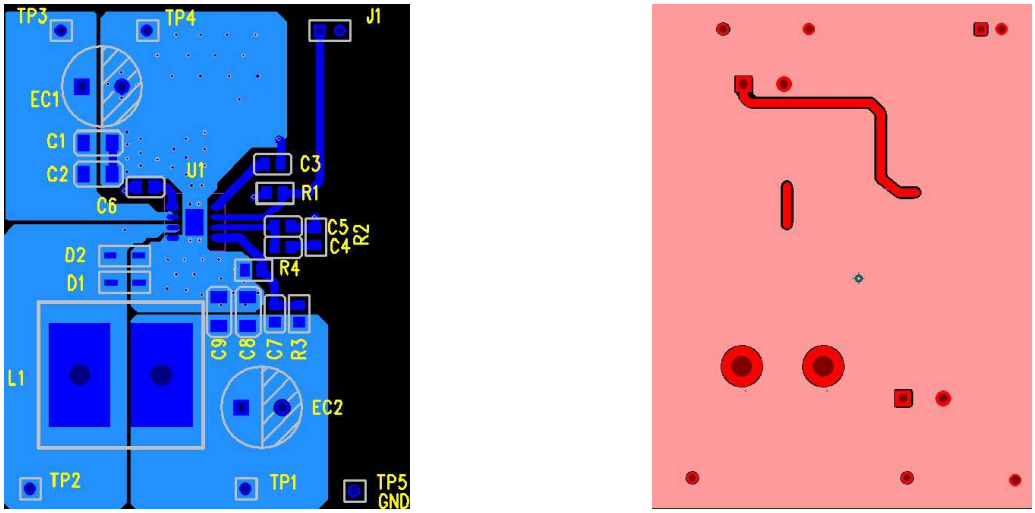


Figure 14. VP2128 reference evaluation board layout

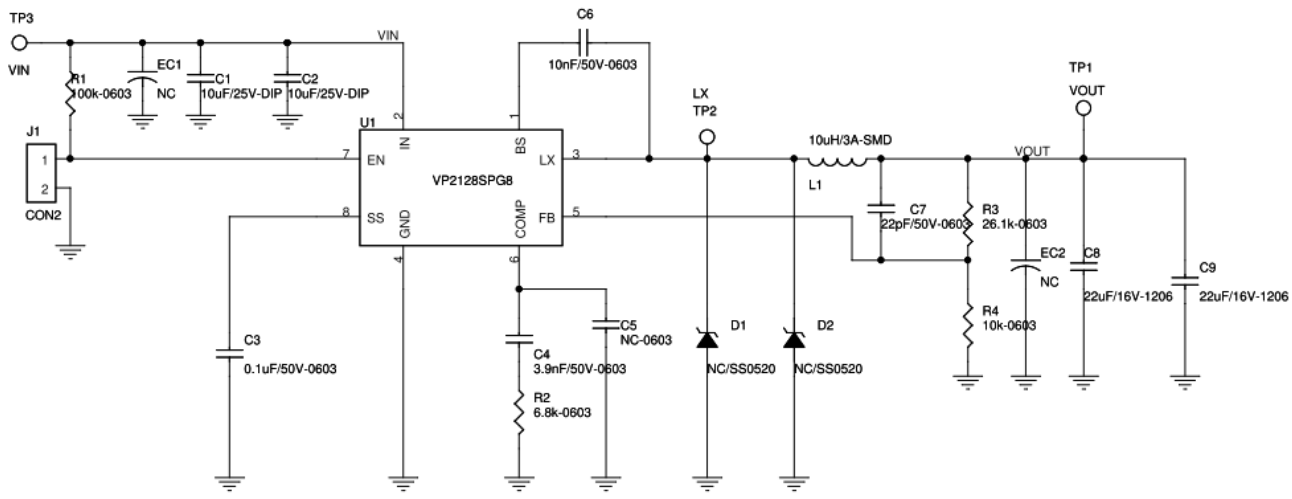
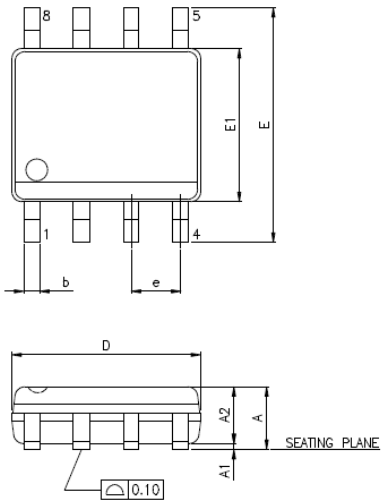
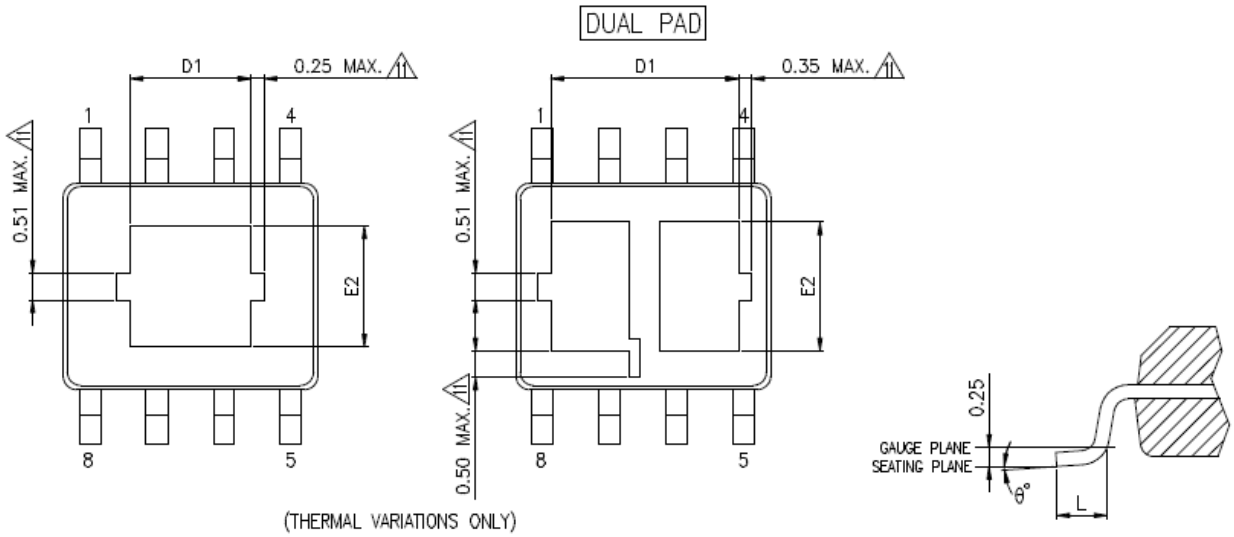


Figure 15. VP2128 reference evaluation board schematic

Package Information

- SO-8P





(THERMAL VARIATIONS ONLY)

SYMBOLS	STANDARD MIN.	STANDARD MAX.	THERMAL MIN.	THERMAL MAX.
A	—	1.75	—	1.70
A1	0.10	0.25	0.00	0.15
A2	1.25	—	1.25	—
b	0.31	0.51	0.31	0.51
c	0.10	0.25	0.10	0.25
D	4.90 BSC		4.90 BSC	
E	6.00 BSC		6.00 BSC	
E1	3.90 BSC		3.90 BSC	
e	1.27 BSC		1.27 BSC	
L	0.40	1.27	0.40	1.27
h	0.25	0.50	0.25	0.50
θ°	0	8	0	8

UNIT : mm

THERMALLY ENHANCED DIMENSIONS

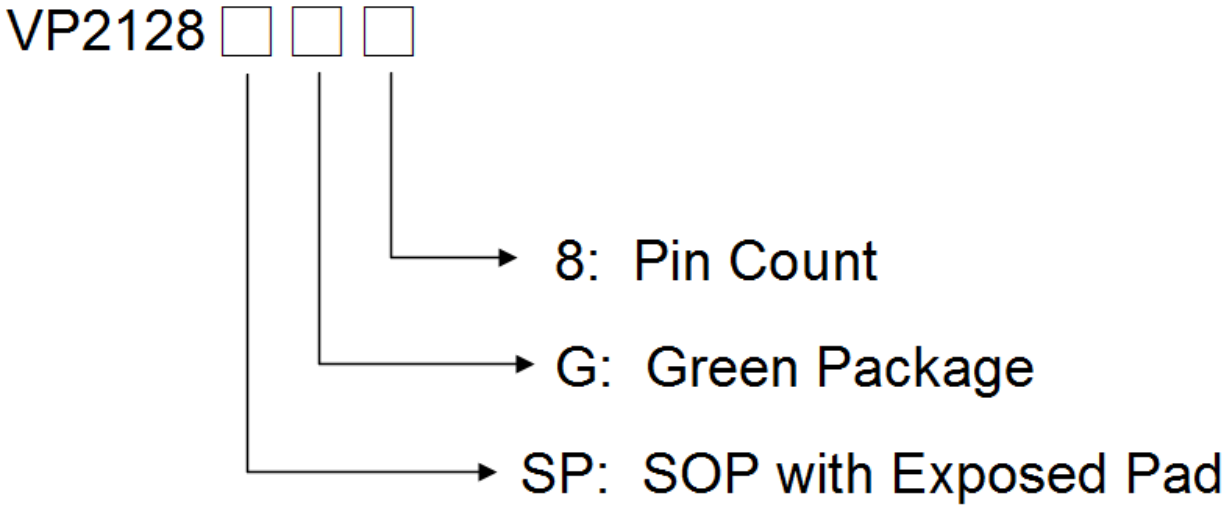
PAD SIZE	E2 MIN.	E2 MAX.	D1 MIN.	D1 MAX.
90X90E	1.94	2.29	1.94	2.29
95X13E	2.05	2.41	2.81	3.30
96X65E(DUAL PAD)	1.78	2.44	2.90	3.56

UNIT : mm

NOTES:

1. JEDEC OUTLINE : MS-012 AA REV.F (STANDARD)
   MS-012 BA REV.F (THERMAL)
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm. PER SIDE.
3. DIMENSIONS "E1" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE.

Ordering Information



Part No.	Q`ty/Reel
VP2128SPG8	2,500

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