



P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

$BV_{DSS} /$ BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package
			Die†
-60V	8.0Ω	-0.5A	VP1506NW
-90V	8.0Ω	-0.5A	VP1509NW

† MIL visual screening available.

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor controls
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

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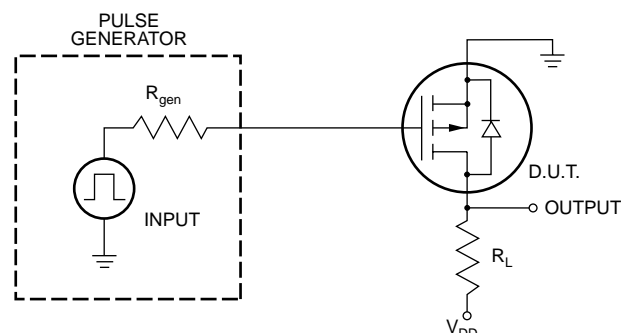
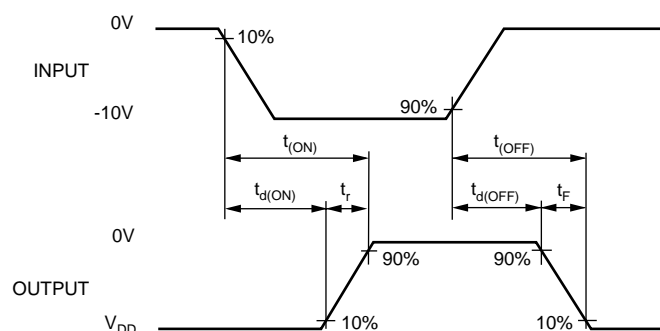
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	VP1509	-90			V	I _D = -1.0mA, V _{GS} = 0V
		VP1506	-60				
V _{GS(th)}	Gate Threshold Voltage		-1.5		-3.5	V	V _{GS} = V _{DS} , I _D = -1.0mA
ΔV _{GS(th)}	Change in V _{GS(th)} with Temperature			5.8	6.5	mV/°C	I _D = -1.0mA, V _{GS} = V _{DS}
I _{GSS}	Gate Body Leakage			-1.0	-100	nA	V _{GS} = ±20V, V _{DS} = 0V
I _{DSS}	Zero Gate Voltage Drain Current				-10	μA	V _{GS} = 0V, V _{DS} = Max Rating
					-1	mA	V _{GS} = 0V, V _{DS} = 0.8 Max Rating T _A = 125°C
I _{D(ON)}	ON-State Drain Current		-0.15	-0.25		A	V _{GS} = -5V, V _{DS} = -25V
			-0.50	-1.2			V _{GS} = -10V, V _{DS} = -25V
R _{DS(ON)}	Static Drain-to-Source ON-State Resistance			11	15	Ω	V _{GS} = -5V, I _D = -0.1A
				6.0	8.0		V _{GS} = -10V, I _D = -0.5A
ΔR _{DS(ON)}	Change in R _{DS(ON)} with Temperature			0.55	1.0	%/°C	V _{GS} = -10V, I _D = -0.5A
G _{FS}	Forward Transconductance		150	190		mS	V _{DS} = -25V, I _D = -0.5A
C _{ISS}	Input Capacitance			45	60	pF	V _{GS} = 0V, V _{DS} = -25V f = 1 MHz
C _{OSS}	Common Source Output Capacitance			22	30		
C _{RSS}	Reverse Transfer Capacitance			3	8		
t _{d(ON)}	Turn-ON Delay Time			4	6	ns	V _{DD} = -25V I _D = -0.5A R _{GEN} = 25Ω
t _r	Rise Time			3	10		
t _{d(OFF)}	Turn-OFF Delay Time			8	12		
t _f	Fall Time			4	10		
V _{SD}	Diode Forward Voltage Drop			-1.2	-2.0	V	I _{SD} = -1.0A, V _{GS} = 0V
t _{rr}	Reverse Recovery Time			400		ns	I _{SD} = -1.0A, V _{GS} = 0V

Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit



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