



P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV _{DSS} / BV _{DGS}	R _{DS(ON)} (max)	I _{D(ON)} (min)	Order Number / Package	
			TO-39	TO-92
-160V	100Ω	-100mA	VP1316N2	VP1316N3
-200V	100Ω	-100mA	VP1320N2	VP1320N3

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{iss} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV _{DSS}
Drain-to-Gate Voltage	BV _{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

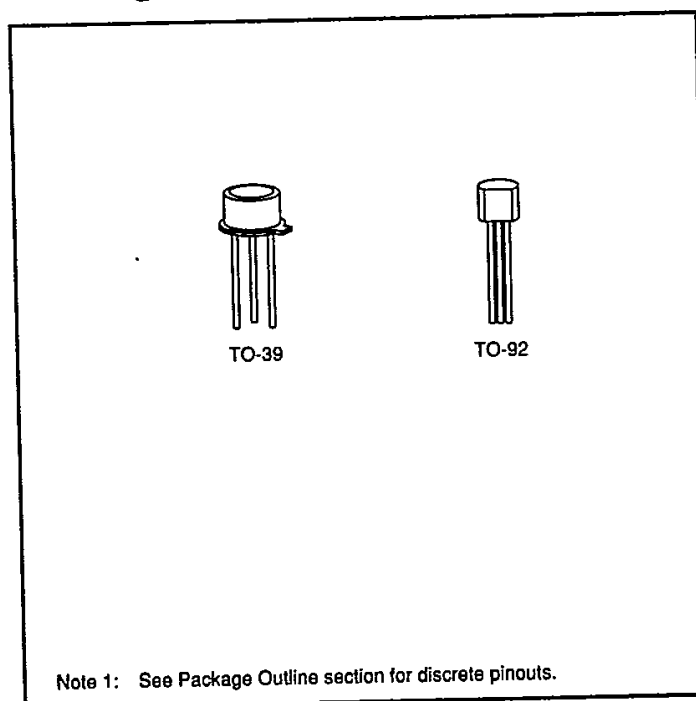
Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options

(Note 1)



Note 1: See Package Outline section for discrete pinouts.

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ $T_C = 25^\circ\text{C}$	θ_{JA} $^\circ\text{C/W}$	θ_{JC} $^\circ\text{C/W}$	I_{DR}	I_{DRM}^*
TO-39	-0.10A	-0.40A	3.0W	125	41	-0.1A	-0.4A
TO-92	-0.06A	-0.30A	0.8W	170	155	-0.06A	-0.3A

* I_D (continuous) is limited by max rated T_J .

Electrical Characteristics (@ 25°C unless otherwise specified)

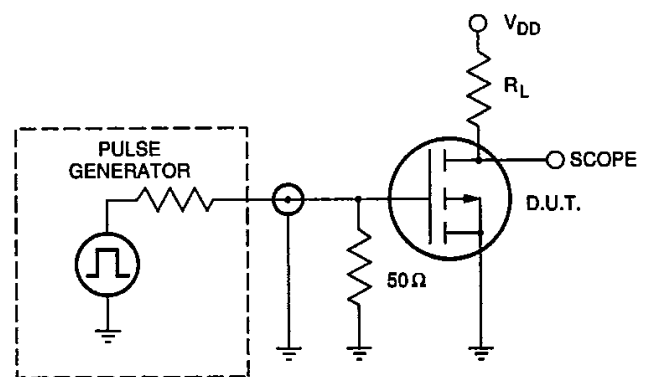
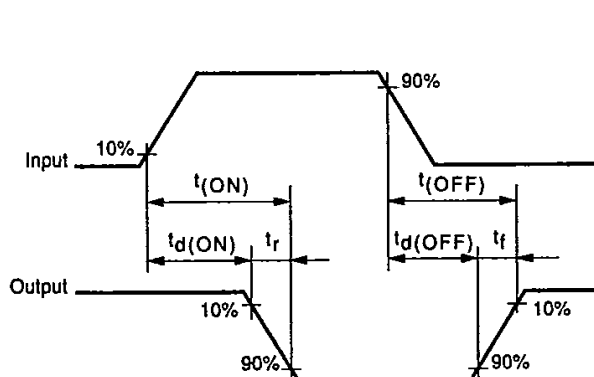
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP1320 VP1316	-200 -160			V	$I_D = -1\text{mA}$, $V_{GS} = 0$
$V_{GS(th)}$	Gate Threshold Voltage		-1.5		-3.5	V	$V_{GS} = V_{DS}$, $I_D = -1\text{mA}$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.0	-5.0	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}$, $I_D = -1\text{mA}$
I_{GSS}	Gate Body Leakage			0.1	100	nA	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				-10 -500	μA	$V_{GS} = 0$, $V_{DS} = \text{Max Rating}$ $V_{GS} = 0$, $V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current		-50 -100	-100 -400		mA	$V_{GS} = -5\text{V}$, $V_{DS} = -25\text{V}$ $V_{GS} = -10\text{V}$, $V_{DS} = -25\text{V}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			65 60	100 100	Ω	$V_{GS} = -5\text{V}$, $I_D = -40\text{mA}$ $V_{GS} = -10\text{V}$, $I_D = -150\text{mA}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.6	1.0	%/ $^\circ\text{C}$	$I_D = -50\text{mA}$, $V_{GS} = -10\text{V}$
G_{FS}	Forward Transconductance		20	30		mS	$V_{DS} = -25\text{V}$, $I_D = -150\text{A}$
C_{ISS}	Input Capacitance			35	40	pF	$V_{GS} = 0$, $V_{DS} = -25\text{V}$ $f = 1 \text{ MHz}$
C_{OSS}	Common Source Output Capacitance			10	15		
C_{RSS}	Reverse Transfer Capacitance			2	5		
$t_{d(ON)}$	Turn-ON Delay Time			1.5	5	ns	$V_{DD} = -25\text{V}$ $I_D = -200\text{mA}$ $R_S = 50\Omega$
t_r	Rise Time			2.5	5		
$t_{d(OFF)}$	Turn-OFF Delay Time			1.5	5		
t_f	Fall Time			2.5	5		
V_{SD}	Diode Forward Voltage Drop			1.6	2.0	V	$I_{SD} = -1\text{A}$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time			350		ns	$I_{SD} = -1\text{A}$, $V_{GS} = 0$

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

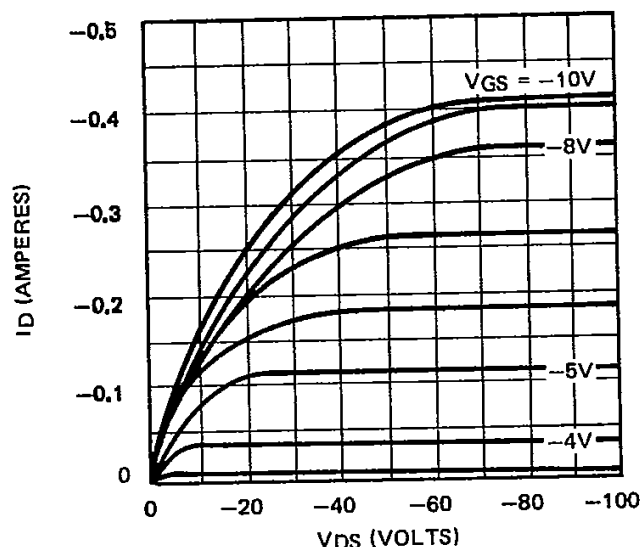
Switching Waveforms and Test Circuit



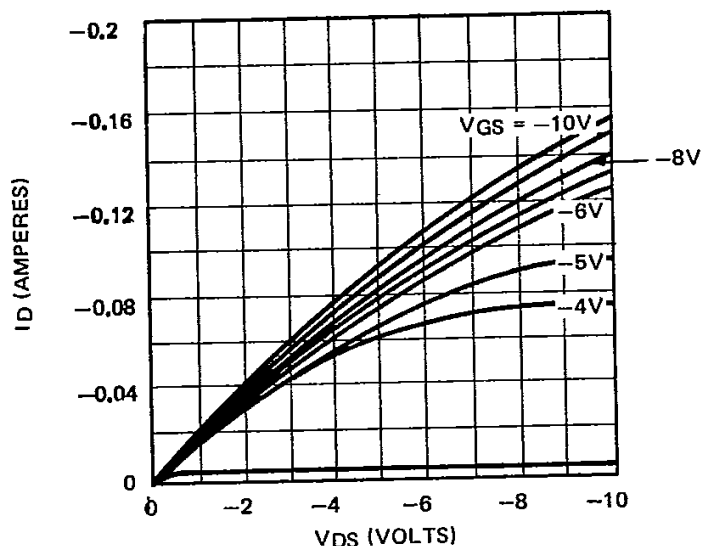
Typical Performance Curves

7-37-25

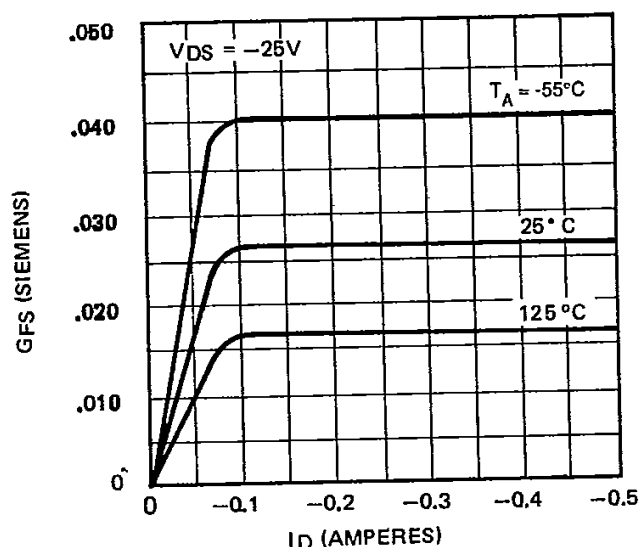
Output Characteristics



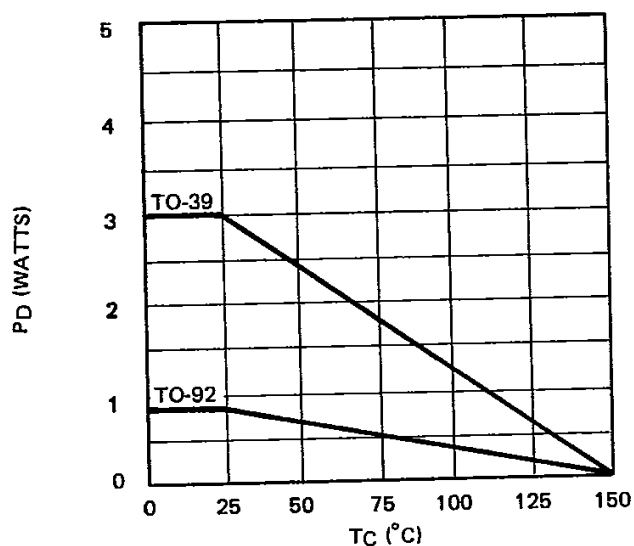
Saturation Characteristics



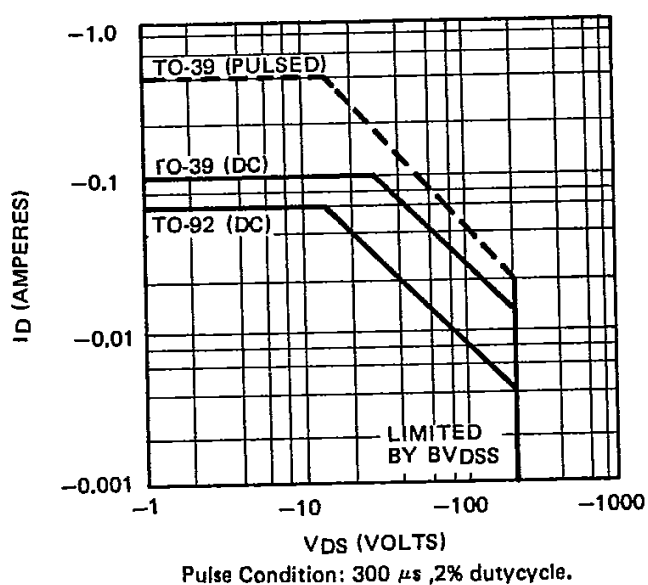
Transconductance Vs. Drain Current



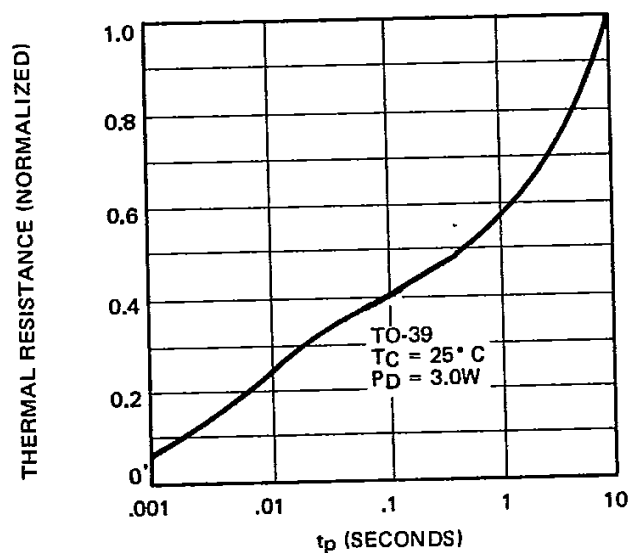
Power Dissipation Vs. Case Temperature



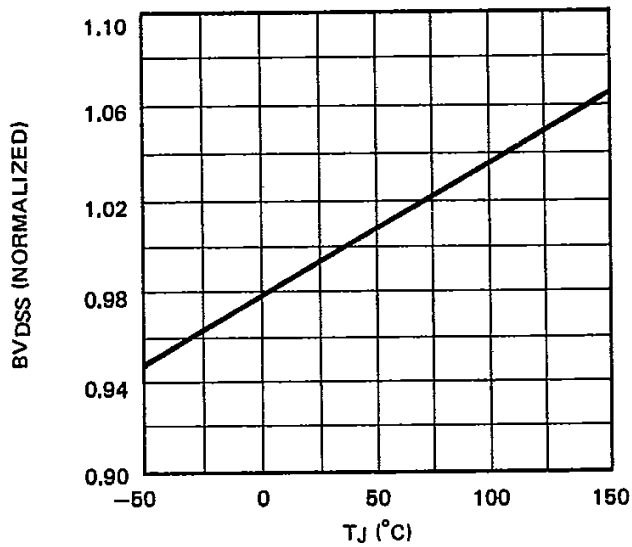
Maximum Rated Safe Operating Area



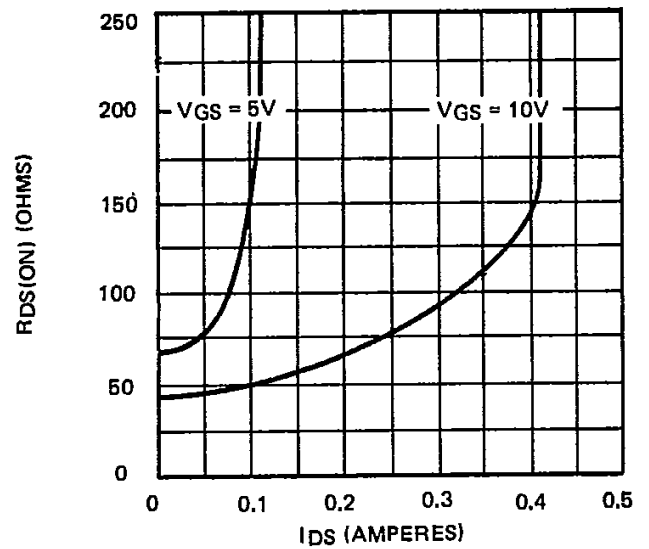
Thermal Response Characteristics



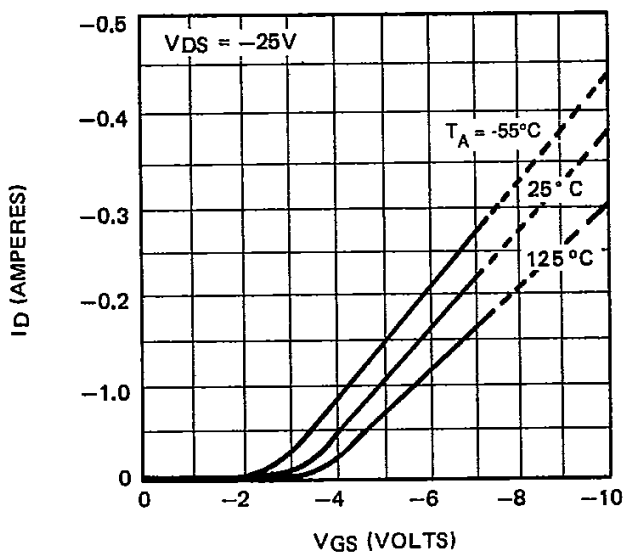
BVDSS Variation with Temperature



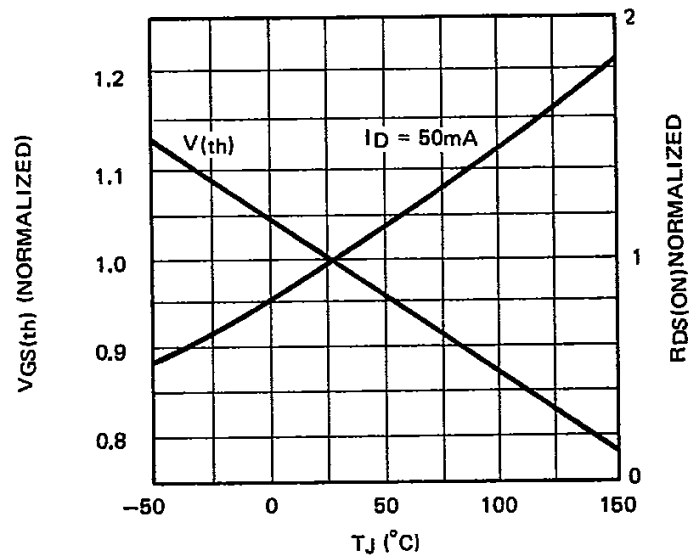
ON- Resistance Vs .Drain Current



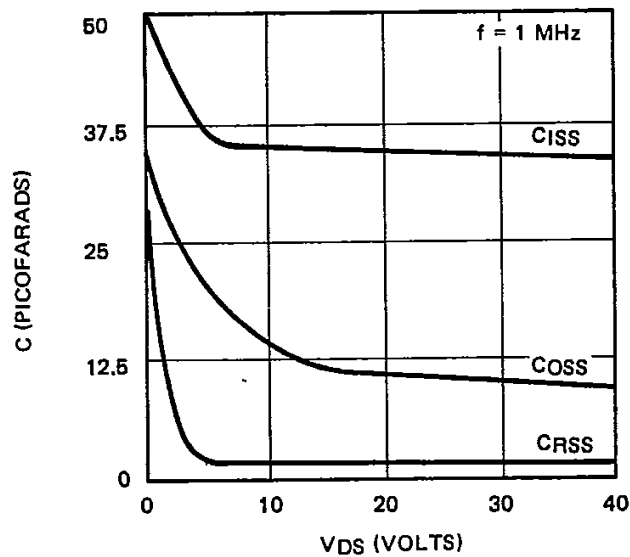
Transfer Characteristics



V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics

