



VP12A

T-39-19



P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package			
			TO-3	TO-39	TO-220	DICE
-40V	0.8Ω	-6A	VP1204N1	VP1204N2	VP1204N5	VP1204ND
-60V	0.8Ω	-6A	VP1206N1	VP1206N2	VP1206N5	VP1206ND
-100V	0.8Ω	-6A	VP1210N1	VP1210N2	VP1210N5	VP1210ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway, and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

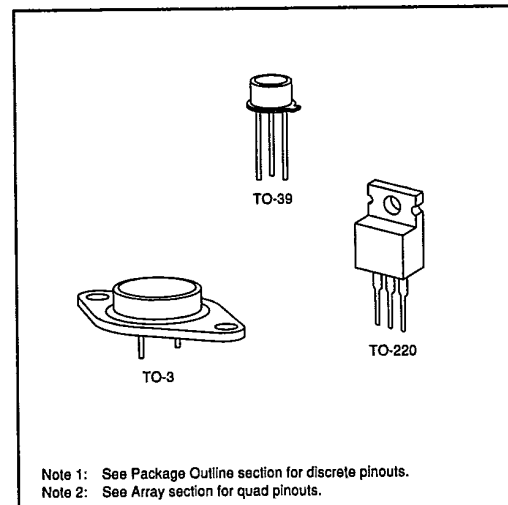
Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	$\pm 20V$
Operating and Storage Temperature	$-55^{\circ}C$ to $+150^{\circ}C$
Soldering Temperature*	$300^{\circ}C$

*Distance of 1.6 mm from case for 10 seconds.

Package Options

(Notes 1 and 2)



Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Thermal Characteristics

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Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ $T_C = 25^\circ\text{C}$	θ_{JA} $^\circ\text{C/W}$	θ_{JC} $^\circ\text{C/W}$	I_{DR}	I_{DRM}^*
TO-3	-7.0A	-14A	100W	30	1.25	-7A	-14A
TO-39	-2.5A	-11A	6.5W	125	20	-2.5A	-11A
TO-220	-5.0A	-14A	45W	70	2.75	-5A	-14A

* I_D (continuous) is limited by max rated T_J .

Electrical Characteristics (@ 25°C unless otherwise specified)

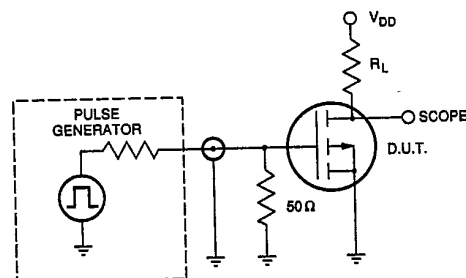
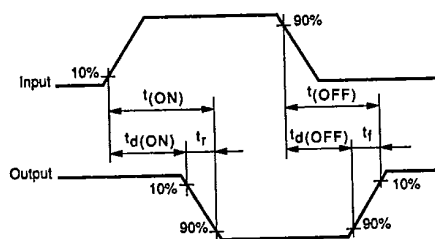
(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP1210	-100		V	$I_D = -10\text{mA}$, $V_{GS} = 0$
		VP1206	-60			
		VP1204	-40			
$V_{GS(th)}$	Gate Threshold Voltage	-1.5		-3.5	V	$V_{GS} = V_{DS}$, $I_D = -10\text{mA}$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature		-4.7	-5.5	mV/ $^\circ\text{C}$	$I_D = -10\text{mA}$, $V_{GS} = V_{DS}$
I_{GSS}	Gate Body Leakage		-1.0	-100	nA	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current			-100	μA	$V_{GS} = 0$, $V_{DS} = \text{Max Rating}$
				-10	mA	$V_{GS} = 0$, $V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current	-1.5	-2.0		A	$V_{GS} = -5\text{V}$, $V_{DS} = -25\text{V}$
		-6.0	-12.0			$V_{GS} = -10\text{V}$, $V_{DS} = -25\text{V}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		1.0	1.4	Ω	$V_{GS} = -5\text{V}$, $I_D = -1\text{A}$
			0.5	0.8		$V_{GS} = -10\text{V}$, $I_D = -3\text{A}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature		1.0	1.5	%/ $^\circ\text{C}$	$I_D = -10\text{A}$, $V_{GS} = -10\text{V}$
G_{FS}	Forward Transconductance	1	2		S	$V_{DS} = -25\text{V}$, $I_D = -3\text{A}$
C_{ISS}	Input Capacitance		550	650	pF	$V_{GS} = 0$, $V_{DS} = -25\text{V}$ $f = 1 \text{ MHz}$
C_{OSS}	Common Source Output Capacitance		250	275		
C_{RSS}	Reverse Transfer Capacitance		25	40		
$t_{d(ON)}$	Turn-ON Delay Time		10	30	ns	$V_{DD} = -25\text{V}$ $I_D = -4\text{A}$ $R_S = 50\Omega$
t_r	Rise Time		17	40		
$t_{d(OFF)}$	Turn-OFF Delay Time		70	105		
t_f	Fall Time		35	60		
V_{SD}	Diode Forward Voltage Drop		-1.2	-1.6	V	$I_{SD} = -5\text{A}$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time		500		ns	$I_{SD} = -1\text{A}$, $V_{GS} = 0$

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)

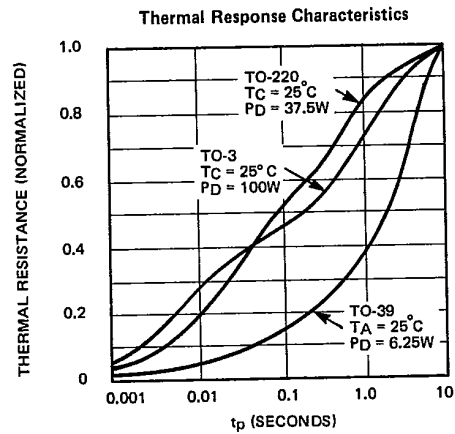
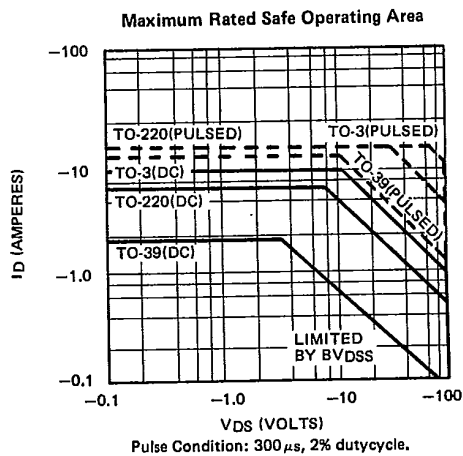
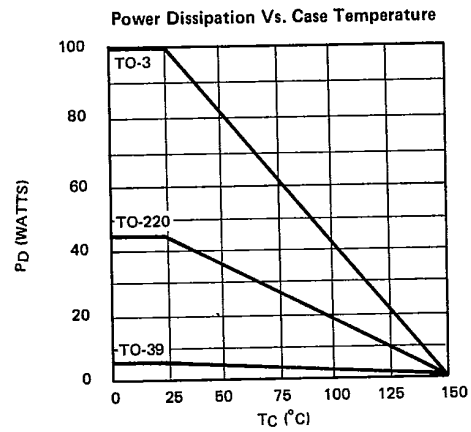
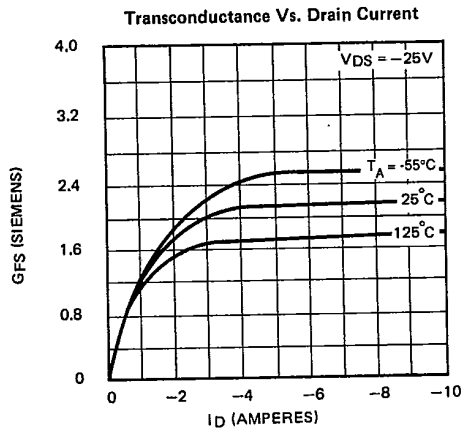
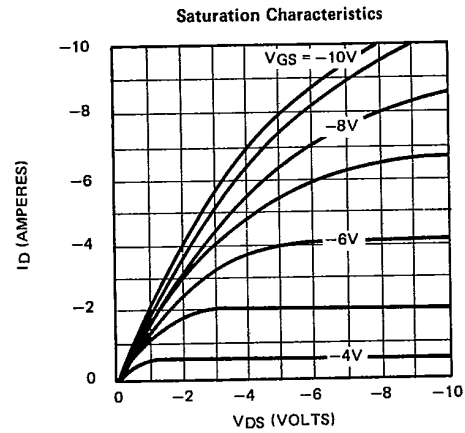
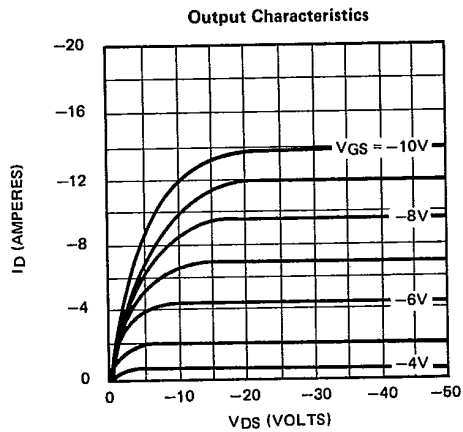
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit



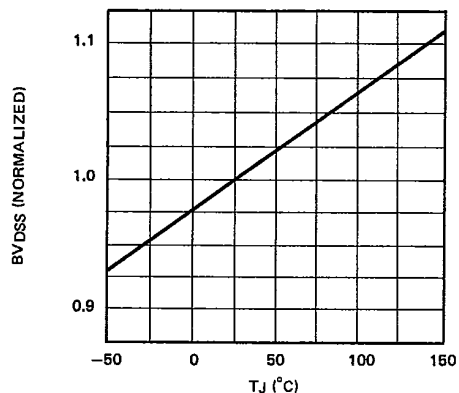
Typical Performance Curves

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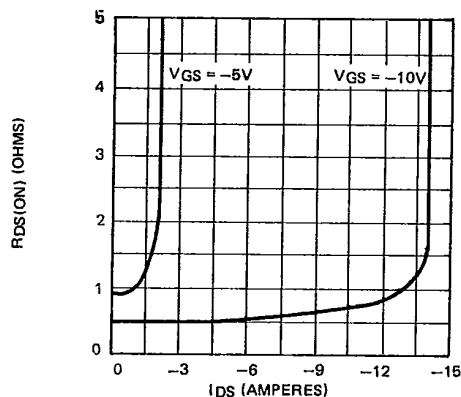


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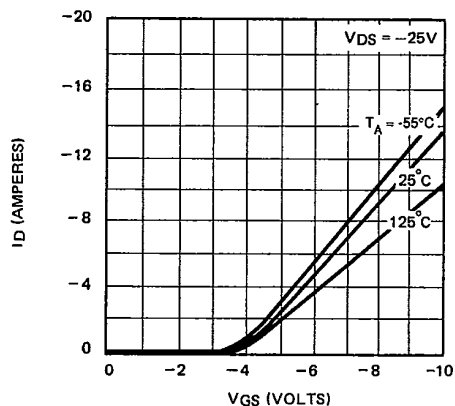
BVDSS Variation with Temperature



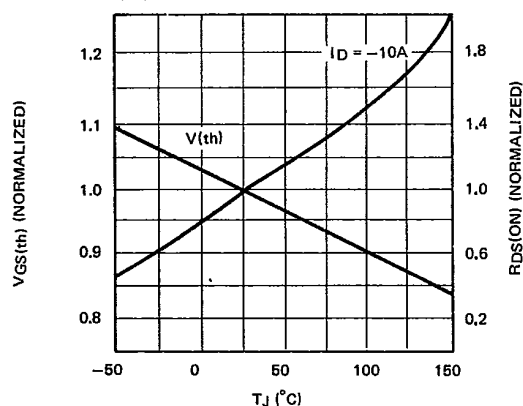
ON-Resistance Vs. Drain Current



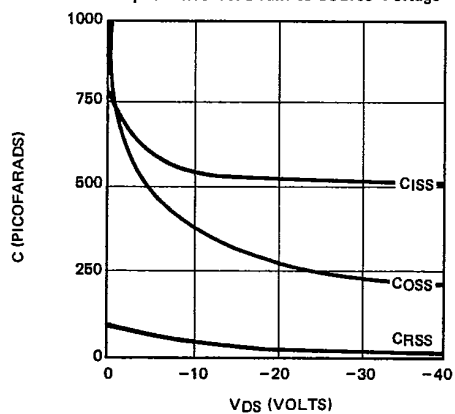
Transfer Characteristics



V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics

