P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-39	TO-92	DICE
-350V	75Ω	-200mA	VP0535N2	VP0535N3	VP0535ND
-400V	75Ω	-200mA	VP0540N2	VP0540N3	VP0540ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

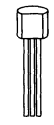
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

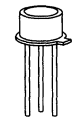
Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Notes 1 and 2)



TO-92



TO-39

Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO - 39	−0.2A	−0.5A	3.5W	35	125	−0.2A	−0.5A
TO - 92	−0.1A	−0.5A	1.0W	125	170	−0.1A	−0.5A

* I_D (continuous) is limited by max rated T_j.

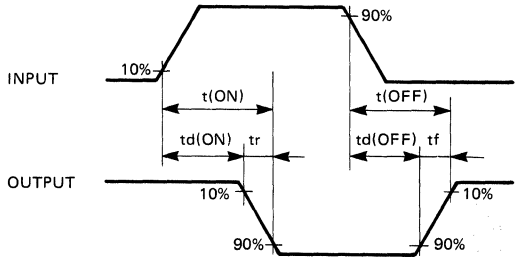
Electrical Characteristics (@ 25°C unless otherwise specified)

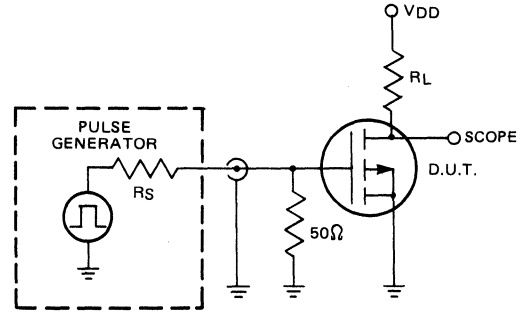
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BVDSS	Drain-to-Source Breakdown Voltage	VP0540	−400			V	VGS = 0, ID = −1mA
		VP0535	−350				
VGS(th)	Gate Threshold Voltage		−2.5		−4.5	V	VGS = VDS, ID = −1mA
ΔVGS(th)	Change in VGS(th) with Temperature			−3.5	−6.0	mV/°C	VGS = VDS, ID = −1mA
IGSS	Gate Body Leakage				−100	nA	VGS = ±20V, VDS = 0
IDSS	Zero Gate Voltage Drain Current				−10	μA	VGS = 0, VDS = Max Rating
					−500		VGS = 0, VDS = 0.8 Max Rating, TA = 125°C
ID(ON)	ON-State Drain Current			−80		mA	VGS = −5V, VDS = −25V
			200	−250			VGS = −10V, VDS = −25V
RDS(ON)	Static Drain-to-Source ON-State Resistance			60		Ω	VGS = −5V, ID = −10mA
				45	75		VGS = −10V, ID = −50mA
ΔRDS(ON)	Change in RDS(ON) with Temperature			0.8	1.5	%/°C	VGS = −10V, ID = −50mA
GFS	Forward Transconductance		50	70		m℧	VDS = −25V, ID = −50mA
CISS	Input Capacitance			40	60	pF	VGS = 0, VDS = −25V, f = 1 MHz
COSS	Common Source Output Capacitance			11	20		
CRSS	Reverse Transfer Capacitance			3	5		
td(ON)	Turn-ON Delay Time				10	ns	VDD = −25V, ID = −50mA, RS = 50Ω
tr	Rise Time				15		
td(OFF)	Turn-OFF Delay Time				15		
tf	Fall Time				10		
VSD	Diode Forward Voltage Drop			−0.8	−1.5	V	VGS = 0, ISD = −0.1A
trr	Reverse Recovery Time			200		ns	VGS = 0, ISD = −0.1A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

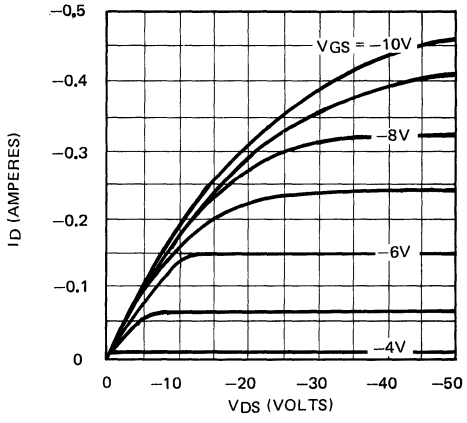
Switching Waveforms and Test Circuit



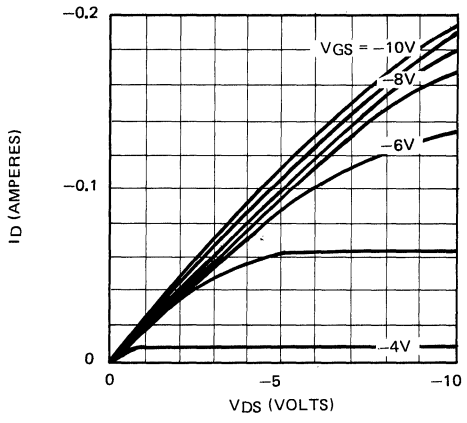


Typical Performance Curves

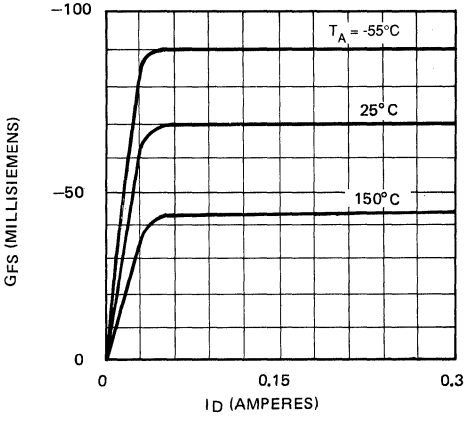
Output Characteristics



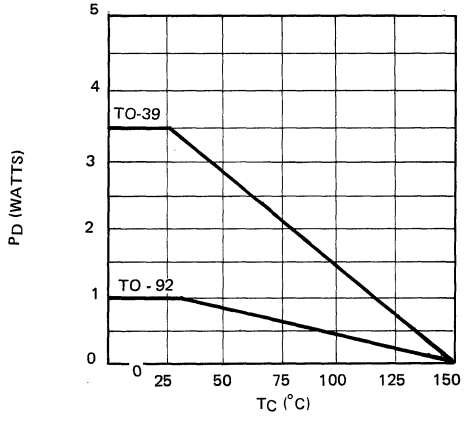
Saturation Characteristics



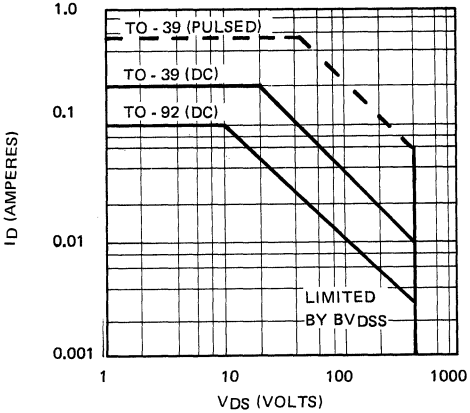
Transconductance Vs. Drain Current



Power Dissipation Vs. Case Temperature

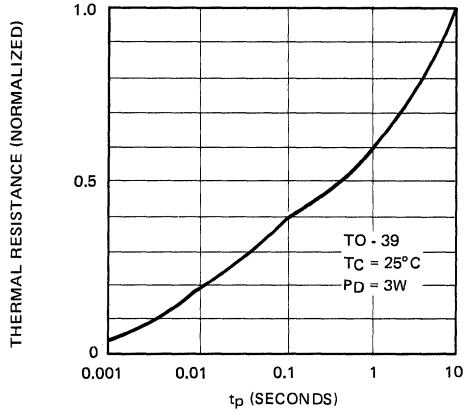


Maximum Rated Safe Operating Area

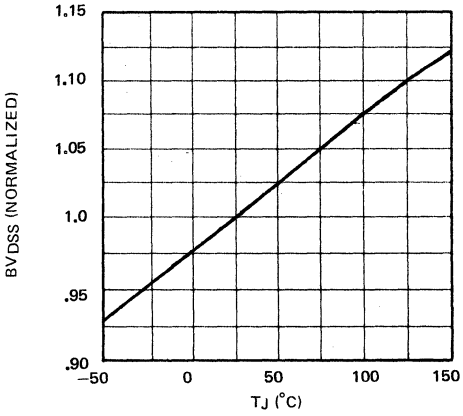


Pulsed Condition: 300μs, 2% Dutycycle

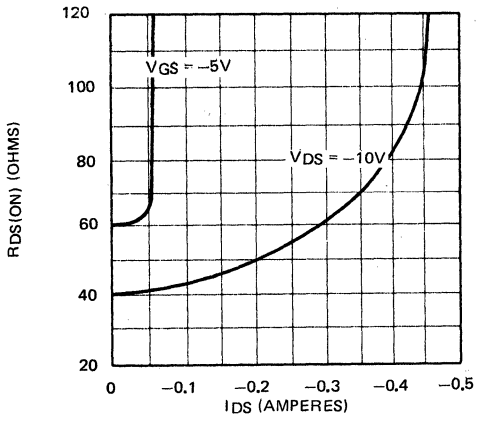
Thermal Response Characteristics



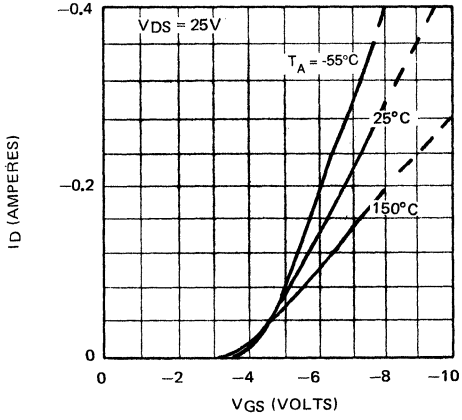
BVDSS Variation with Temperature



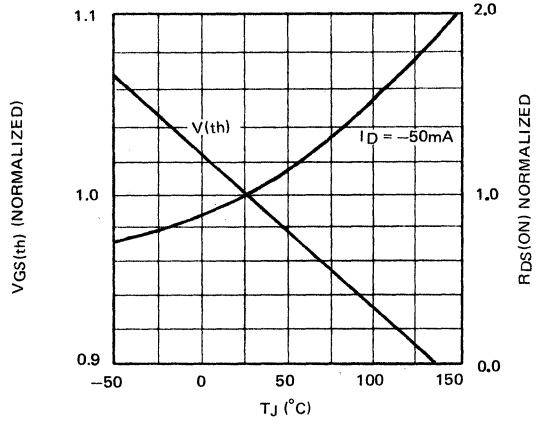
ON - Resistance Vs . Drain Current



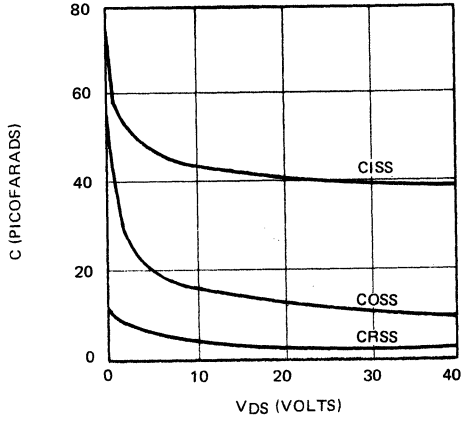
Transfer Characteristics



V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics