



P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)} (max)$	$I_{D(ON)} (min)$	Order Number / Package			
			TO-3	TO-39	TO-220	DICE
-450V	7.5Ω	-1A	VP0345N1	VP0345N2	VP0345N5	VP0345ND
-500V	7.5Ω	-1A	VP0350N1	VP0350N2	VP0350N5	VP0350ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Convertors
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

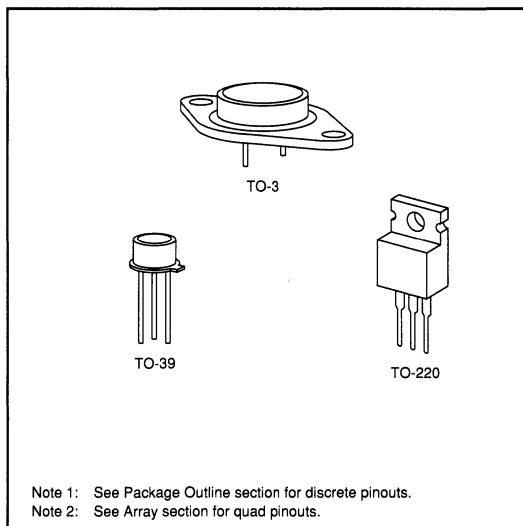
Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Package Options

(Notes 1 and 2)



Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ $T_C = 25^\circ\text{C}$	$\theta_{j\epsilon}$ $^\circ\text{C/W}$	θ_{ja} $^\circ\text{C/W}$	I_{DR}	I_{DRM}^*
TO-3	-1.5A	-3.0A	100W	1.25	30	-1.5A	-3.0A
TO-39	-0.4A	-3.0A	6W	20.8	125	-0.4A	-3.0A
TO-220	-1.0A	-3.0A	50W	2.5	40	-1.0A	-3.0A

* I_D (continuous) is limited by max rated T_J .

Electrical Characteristics (@ 25°C unless otherwise specified)

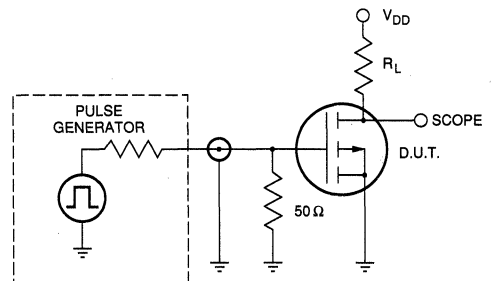
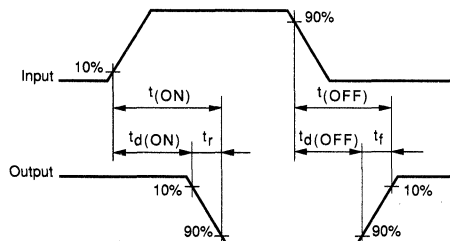
(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP0350 -500			V	$V_{GS} = 0, I_D = -10\text{mA}$
		VP0345 -450				
$V_{GS(th)}$	Gate Threshold Voltage	-2.5		-4.5	V	$V_{GS} = V_{DS}, I_D = -10\text{mA}$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature		-4.8	-6.0	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = -10\text{mA}$
I_{GSS}	Gate Body Leakage			-100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current			-200	μA	$V_{GS} = 0, V_{DS} = \text{Max Rating}$
				-2	mA	$V_{GS} = 0, V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current		-0.75		A	$V_{GS} = -5\text{V}, V_{DS} = -25\text{V}$
		-1.0	-2.5			$V_{GS} = -10\text{V}, V_{DS} = -25\text{V}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		6.0		Ω	$V_{GS} = -5\text{V}, I_D = -0.25\text{A}$
			5.5	7.5		$V_{GS} = -10\text{V}, I_D = -0.25\text{A}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature		0.7	1.2	%/ $^\circ\text{C}$	$V_{GS} = -10\text{V}, I_D = -0.25\text{A}$
G_{FS}	Forward Transconductance	0.25	0.75		S	$V_{DS} = -25\text{V}, I_D = -0.5\text{A}$
C_{ISS}	Input Capacitance		550	700	pF	$V_{GS} = 0, V_{DS} = -25\text{V}$ $f = 1 \text{ MHz}$
C_{OSS}	Common Source Output Capacitance		90	120		
C_{RSS}	Reverse Transfer Capacitance		20	50		
$t_{d(ON)}$	Turn-ON Delay Time		11	30	ns	$V_{DD} = -25\text{V}$ $I_D = -0.5\text{A}$ $R_S = 50\Omega$
t_r	Rise Time		11	30		
$t_{d(OFF)}$	Turn-OFF Delay Time		70	100		
t_f	Fall Time		22	30		
V_{SD}	Diode Forward Voltage Drop		-1.0	-1.3	V	$V_{GS} = 0, I_{SD} = -0.25\text{A}$
t_{rr}	Reverse Recovery Time		550		ns	$V_{GS} = 0, I_{SD} = -0.25\text{A}$

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

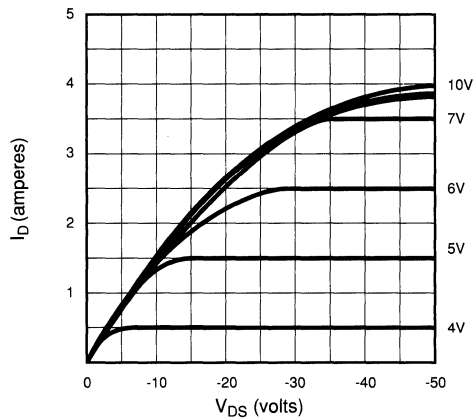
Switching Waveforms and Test Circuit



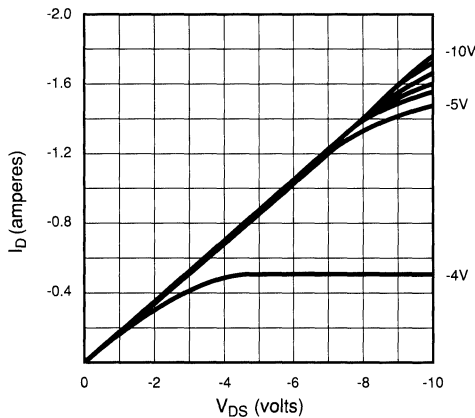
Typical Performance Curves

VP03E

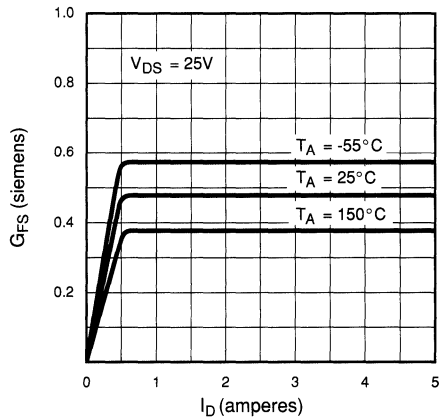
Output Characteristics



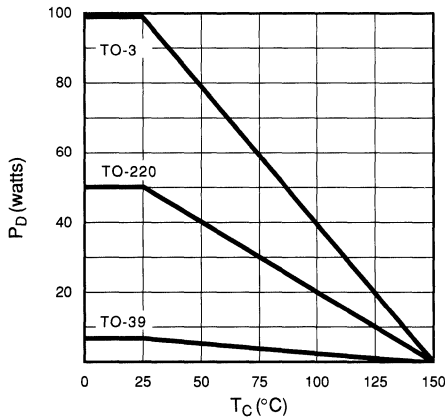
Saturation Characteristics



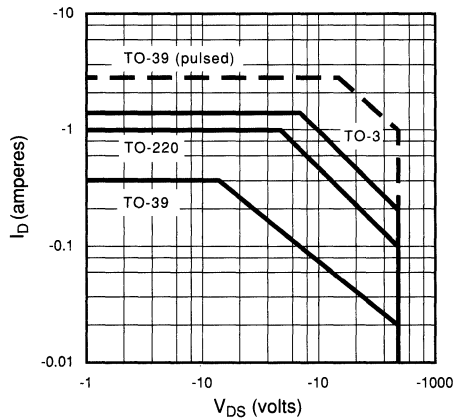
Transconductance vs. Drain Current



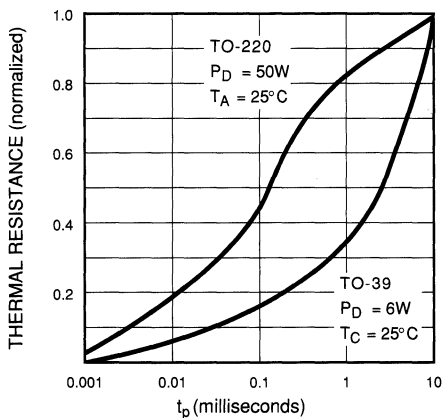
Power Dissipation vs. Case Temperature



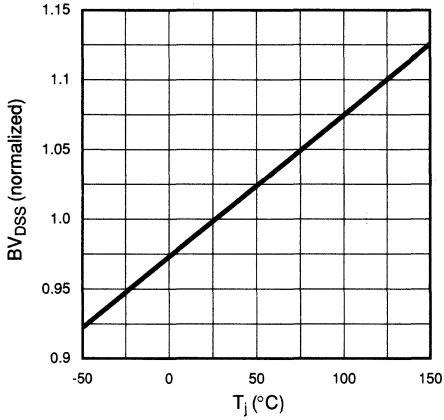
Maximum Rated Safe Operating Area



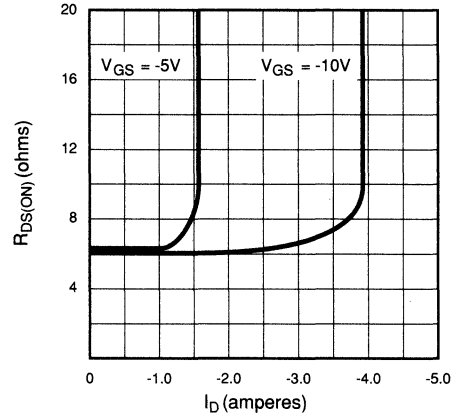
Thermal Response Characteristics



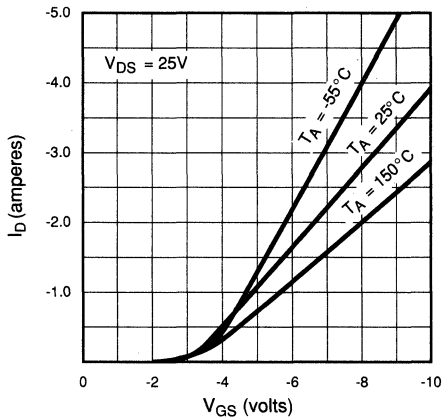
BV_{DSS} Variation with Temperature



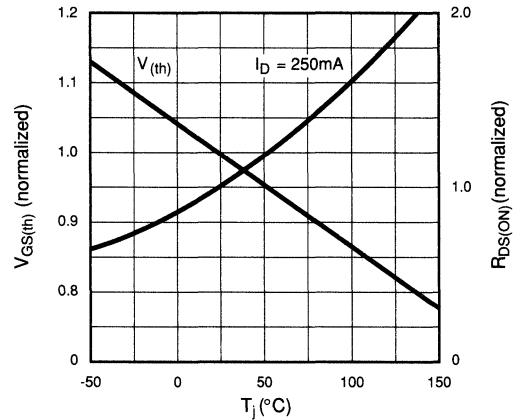
On-Resistance vs. Drain Current



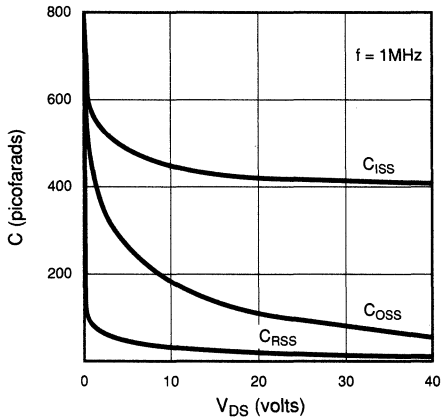
Transfer Characteristics



V_{th} and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics

