VND5N07/VND5N07-1
VNP5N07FI/K5N07FM

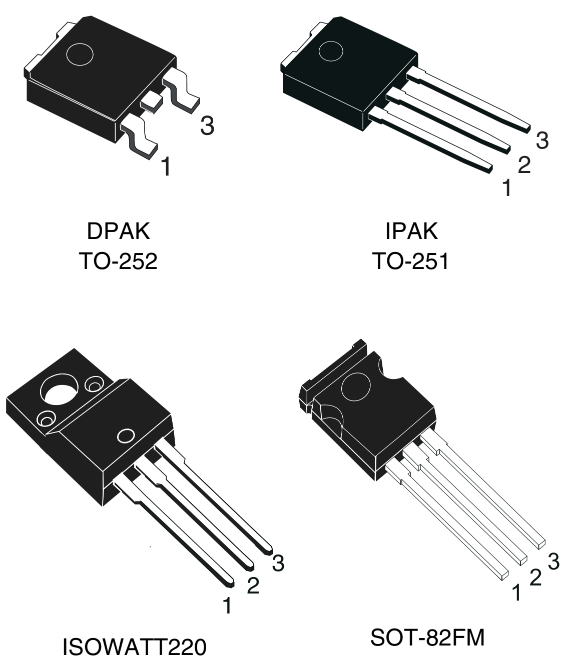
"OMNIFET": FULLY AUTOPROTECTED POWER MOSFET

Table 1. General Features

Type	V_{clamp}	$R_{DS(on)}$	I_{lim}
VND5N07 VND5N07-1 VND5N07FI VND5N07FM	70 V	0.2 Ω	5 A

- LINEAR CURRENT LIMITATION
- THERMAL SHUT DOWN
- SHORT CIRCUIT PROTECTION
- INTEGRATED CLAMP
- LOW CURRENT DRAWN FROM INPUT PIN
- DIAGNOSTIC FEEDBACK THROUGH INPUT PIN
- ESD PROTECTION
- DIRECT ACCESS TO THE GATE OF THE POWER MOSFET (ANALOG DRIVING)
- COMPATIBLE WITH STANDARD POWER MOSFET

Figure 1. Package



DESCRIPTION

The VND5N07, VND5N07-1, VNP5N07FI and VNK5N07FM are monolithic devices made using STMicroelectronics VIPower M0 Technology, intended for replacement of standard power MOSFETS in DC to 50 KHz applications. Built-in thermal shut-down, linear current limitation and overvoltage clamp protect the chip in harsh enviroments.

Fault feedback can be detected by monitoring the voltage at the input pin.

Table 2. Order Codes

Package	Tube	Tape and Reel
DPAK	VND5N07	VND5N0713TR
IPAK	VND5N07-1	–
ISOWATT220	VND5N07FI	–
SOT-82FM	VND5N07FM	–

Figure 2. Block Diagram

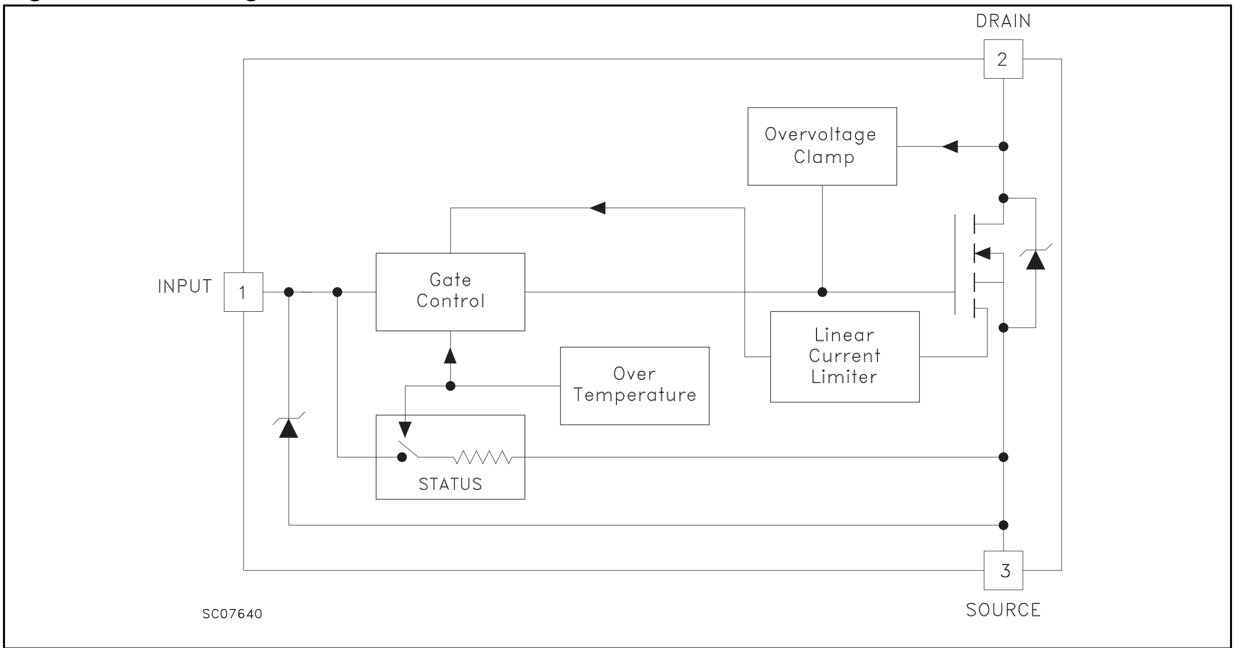


Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value			Unit
		DPAK IPAK	ISOWATT220	SOT-82FM	
V_{DS}	Drain-Source Voltage (V_{in} = 0)	Internally Clamped			V
V_{in}	Input Voltage	18			V
I_D	Drain Current	Internally Limited			A
I_R	Reverse DC Output Current	–7			A
V_{esd}	Electrostatic Discharge (C = 100 pF, R =1.5 KΩ)	2000			V
P_{tot}	Total Dissipation at T_c = 25 °C	60	24	9	W
T_j	Operating Junction Temperature	Internally Limited			°C
T_c	Case Operating Temperature	Internally Limited			°C
T_{stg}	Storage Temperature	-55 to 150			°C

Table 4. Thermal Data

Symbol	Parameter		DPAK/IPAK	ISOWATT220	SOT-82FM	Unit
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	3.75	5.2	14	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100	62.5	100	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Table 5. Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CLAMP}	Drain-source Clamp Voltage	I_D = 200 mA; V_{in} = 0	60	70	80	V
V_{CLTH}	Drain-source Threshold Voltage	I_D = 2 mA; V_{in} = 0	55			V
V_{INCL}	Input-Source Reverse Clamp Voltage	I_{in} = –1 mA	–1		–0.3	V
I_{DSS}	Zero Input Voltage Drain Current (V_{in} = 0)	V_{DS} = 13 V; V_{in} = 0 V_{DS} = 25 V; V_{in} = 0			50 200	µA µA
I_{ISS}	Supply Current from Input Pin	V_{DS} = 0 V; V_{in} = 10 V		250	500	µA

Table 6. On (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{IN(th)}$	Input Threshold Voltage	V_{DS} = V_{in}; I_D + I_{in} = 1 mA	0.8		3	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{in} = 10 V; I_D = 2.5 A V_{in} = 5 V; I_D = 2.5 A			0.200 0.280	Ω Ω

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

Table 7. Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (2)	Forward Transconductance	V_{DS} = 13 V; I_D = 2.5 A	3	4		S
C_{oss}	Output Capacitance	V_{DS} = 13 V; f = 1 MHz; V_{in} = 0		200	300	pF

Note: 2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%.

Table 8. Switching (3)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	V_{DD} = 15 V; I_d = 2.5 A; V_{gen} = 10V; R_{gen} = 10 Ω (see Figure 28)		50 60 150 40	100 100 300 80	ns ns ns ns
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	V_{DD} = 15 V; I_d = 2.5 A; V_{gen} = 10V; R_{gen} = 1000 Ω (see Figure 28)		150 400 3900 1100	250 600 5000 1600	ns ns ns ns
$(di/dt)_{on}$	Turn-on Current Slope	V_{DD} = 15 V; I_D = 2.5 A V_{in} = 10 V; R_{gen} = 10 Ω		80		A/µS
Q_i	Total Input Charge	V_{DD} = 12 V; I_D = 2.5 A; V_{in} = 10 V		18		nC

Note: 3. Parameters guaranteed by design/characterization.

ELECTRICAL CHARACTERISTICS (cont'd)

Table 9. Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{SD}(4)	Forward On Voltage	I_{SD} = 2.5 A; V_{in} = 0			1.6	V
t_{rr}(5)	Reverse Recovery Time	I_{SD} = 2.5 A; di/dt = 100 A/μs V_{DD} = 30 V; T_j = 25 °C (see test circuit, Figure 30)		150		ns
Q_{rr}(5)	Reverse Recovery Charge			0.3		μC
I_{RRM}(5)	Reverse Recovery Current			5.7		A

Note: 4. Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
5. Parameters guaranteed by design/characterization.

Table 10. Protection

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{lim}	Drain Current Limit	V_{in} = 10 V; V_{DS} = 13 V V_{in} = 5 V; V_{DS} = 13 V	3.5 3.5	5 5	7 7	A A
t_{dlim}(6)	Step Response Current Limit	V_{in} = 10 V V_{in} = 5 V		15 40	20 60	μs μs
T_{jsh}(6)	Overtemperature Shutdown		150			°C
T_{jrs}(6)	Overtemperature Reset		135			°C
I_{gf}(6)	Fault Sink Current	V_{in} = 10 V; V_{DS} = 13 V V_{in} = 5 V; V_{DS} = 13 V		50 20		mA mA
E_{as}(6)	Single Pulse Avalanche Energy	starting T_j = 25 °C; V_{DD} = 20 V V_{in} = 10 V; R_{gen} = 1 KΩ; L = 10 mH	0.2			J

Note: 6. Parameters guaranteed by design/characterization.

PROTECTION FEATURES

During normal operation, the Input pin is electrically connected to the gate of the internal power MOSFET. The device then behaves like a standard power MOSFET and can be used as a switch from DC to 50 KHz. The only difference from the user's standpoint is that a small DC current (I_{iss}) flows into the Input pin in order to supply the internal circuitry.

The device integrates:

– OVERVOLTAGE CLAMP PROTECTION: internally set at 70V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.

– LINEAR CURRENT LIMITER CIRCUIT: limits the drain current Id to Ilim whatever the Input pin voltage. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the overtemperature threshold T_{jsh}.

– OVERTEMPERATURE AND SHORT CIRCUIT PROTECTION: these are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cutout occurs at minimum 150°C. The device is automatically restarted when the chip temperature falls below 135°C.

– STATUS FEEDBACK: In the case of an overtemperature fault condition, a Status Feedback is provided through the Input pin. The internal protection circuit disconnects the input from the gate and connects it instead to ground via an equivalent resistance of 100 Ω. The failure can be detected by monitoring the voltage at the Input pin, which will be close to ground potential.

Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL Logic circuit (with a small increase in $R_{DS(on)}$).

Figure 3. Thermal Impedance for DPAK/IPAK

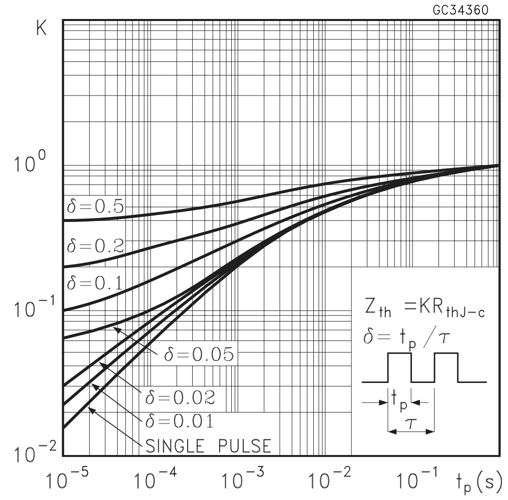


Figure 4. Thermal Impedance for ISOWATT220

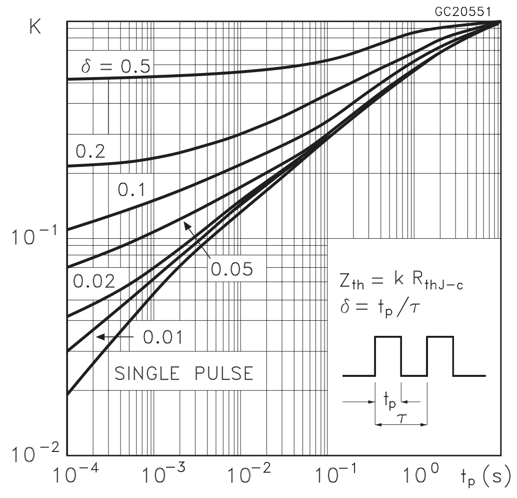


Figure 5. Derating Curve

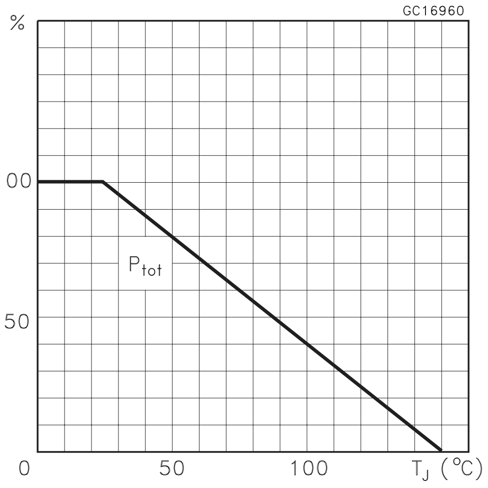


Figure 6. Output Characteristics

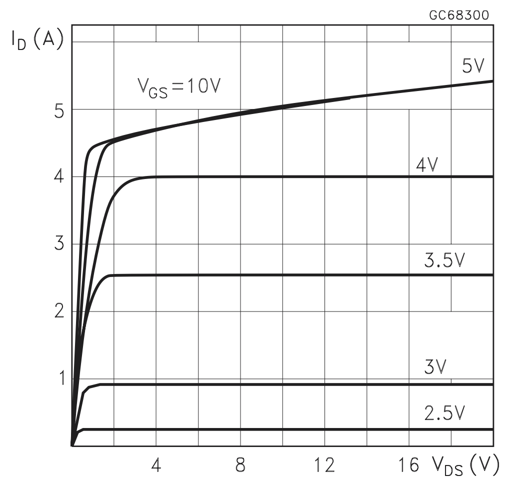


Figure 7. Transconductance

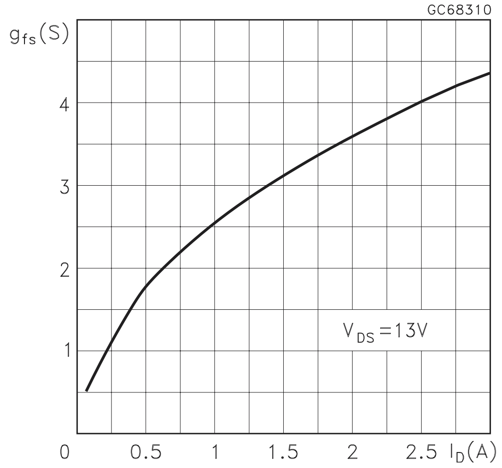


Figure 8. Static Drain-source On Resistance vs Input Voltage

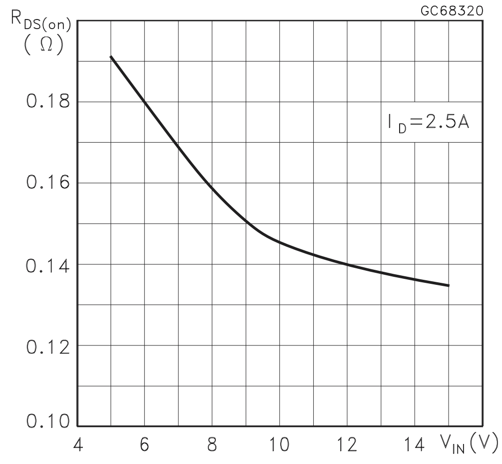


Figure 9. Static Drain-Source On Resistance

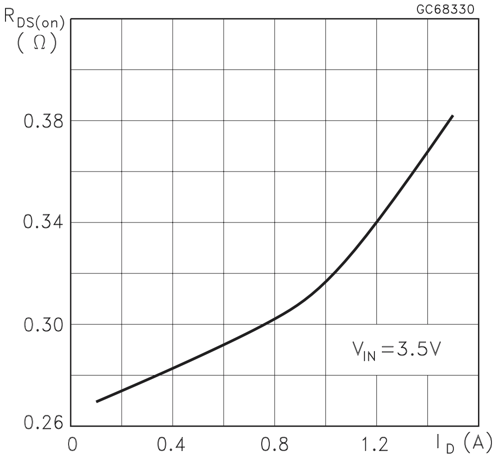


Figure 10. Static Drain-Source On Resistance

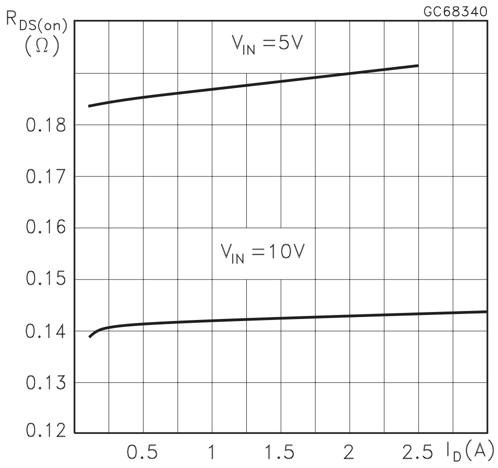


Figure 11. Input Charge vs Input Voltage

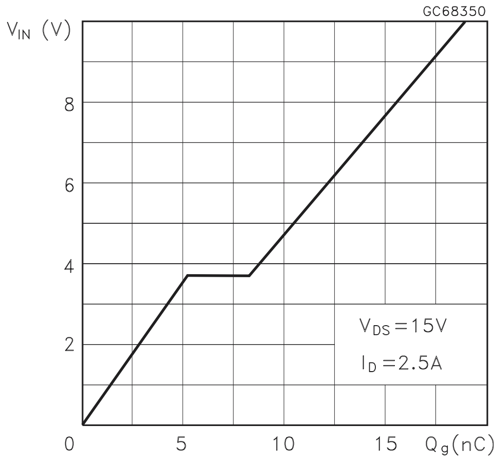


Figure 12. Capacitance Variations

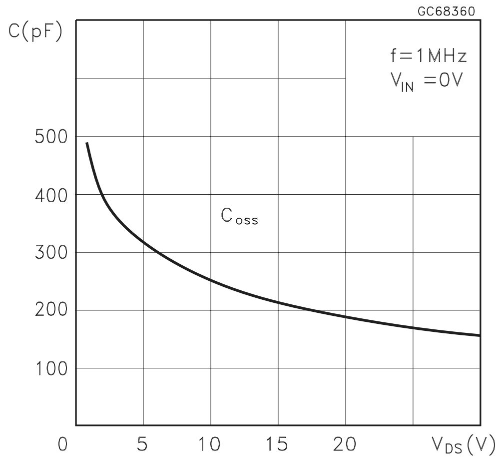


Figure 13. Normalized Input Threshold Voltage vs Temperature

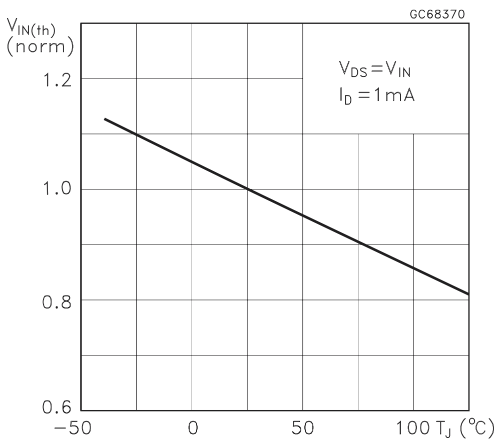


Figure 14. Normalized On Resistance vs Temperature

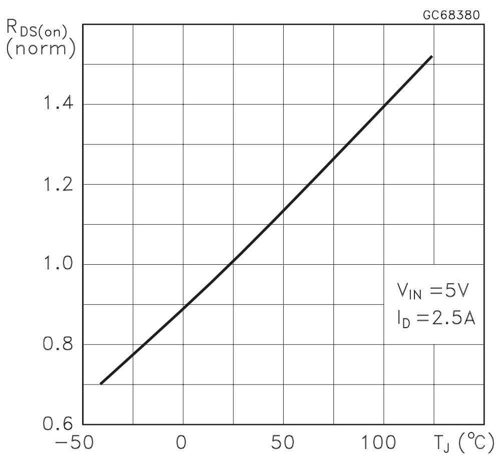


Figure 15. Normalized On Resistance vs Temperature

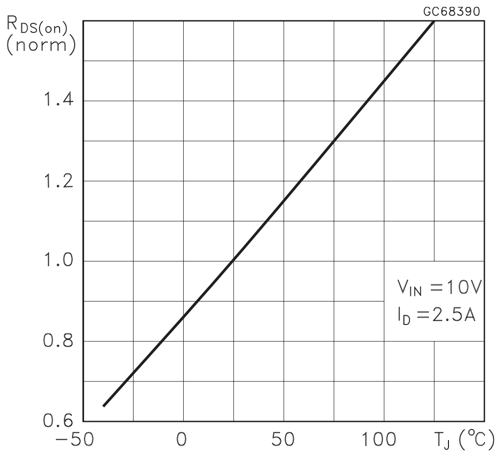


Figure 16. Turn-on Current Slope

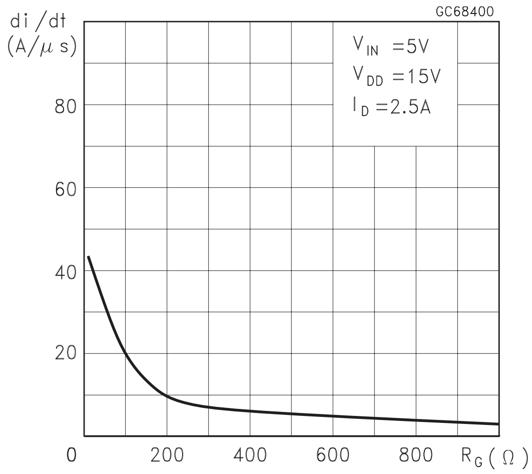


Figure 17. Turn-on Current Slope

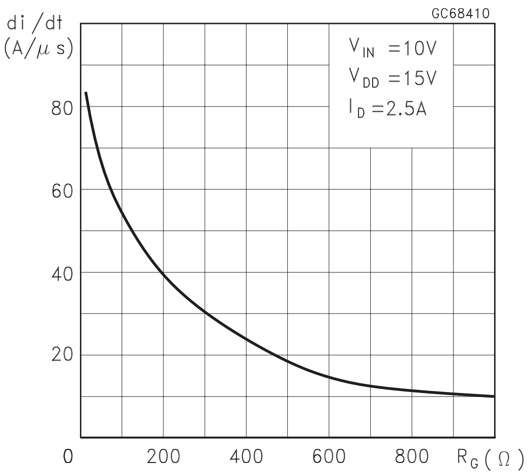


Figure 18. Turn-off Drain-Source Voltage Slope

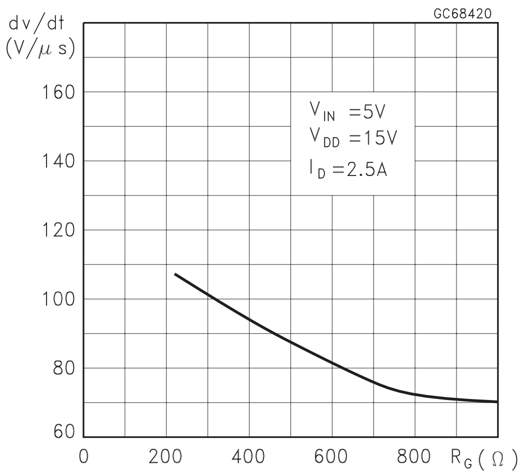


Figure 19. Turn-off Drain-Source Voltage Slope

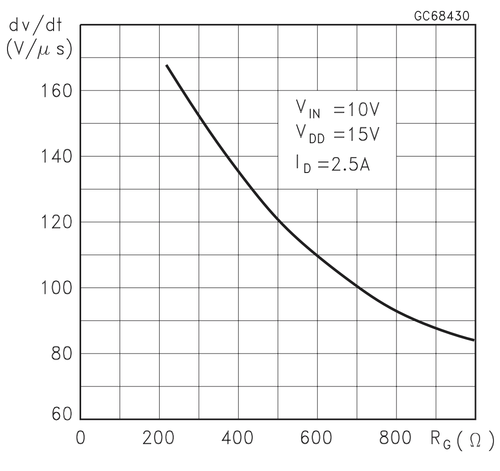


Figure 20. Switching Time Resistive Load

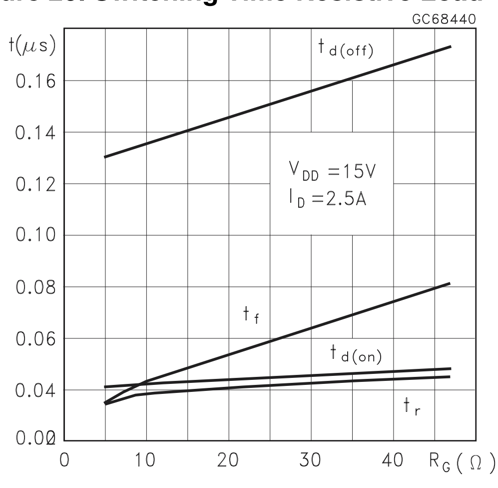


Figure 21. Switching Time Resistive Load

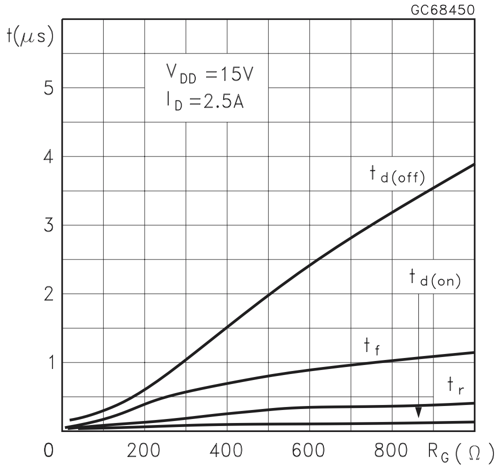


Figure 22. Switching Time Resistive Load

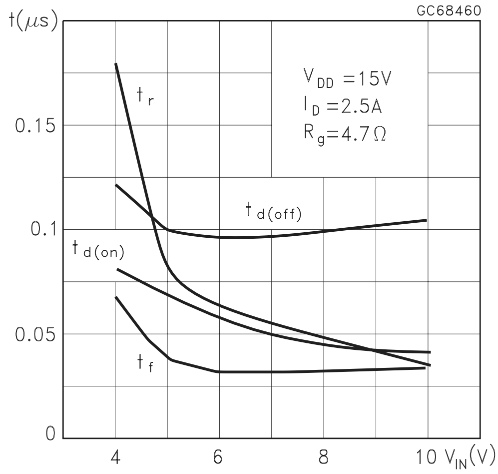


Figure 23. Current Limit vs Junction Temperature

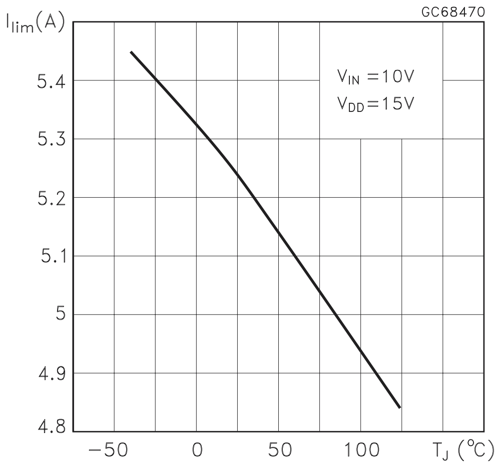


Figure 24. Step Response Current Limit

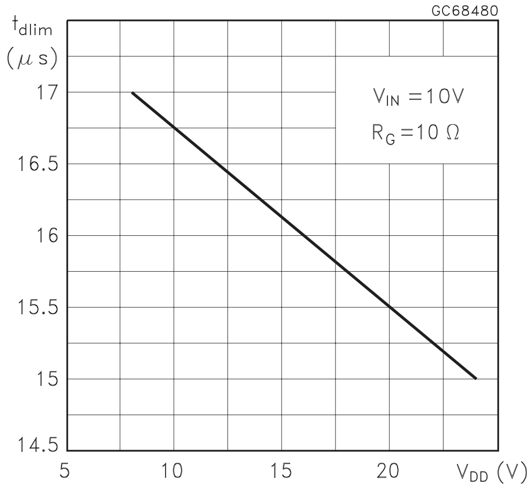


Figure 25. Source Drain Diode Forward Characteristics

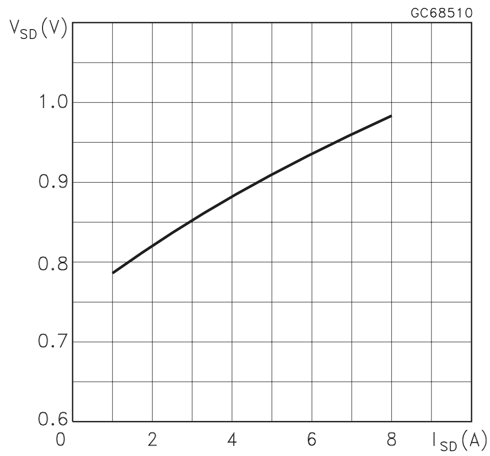


Figure 26. Unclamped Inductive Load Test Circuit

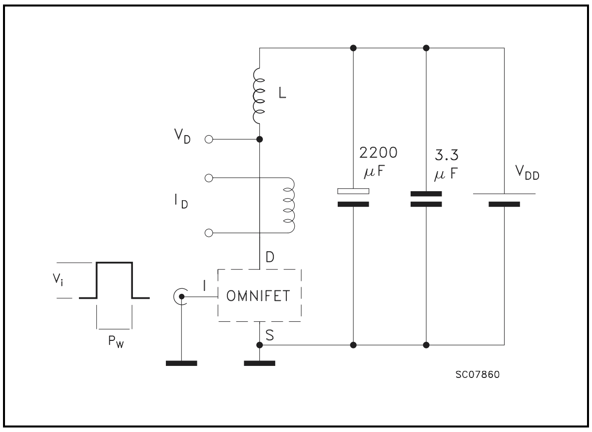


Figure 27. Unclamped Inductive Waveforms

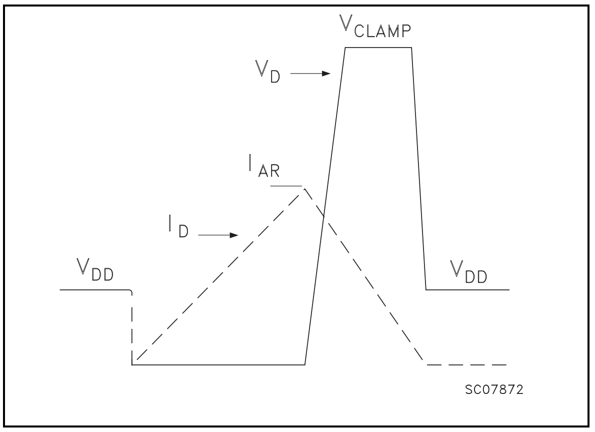


Figure 28. Switching Times Test Circuits For Resistive Load

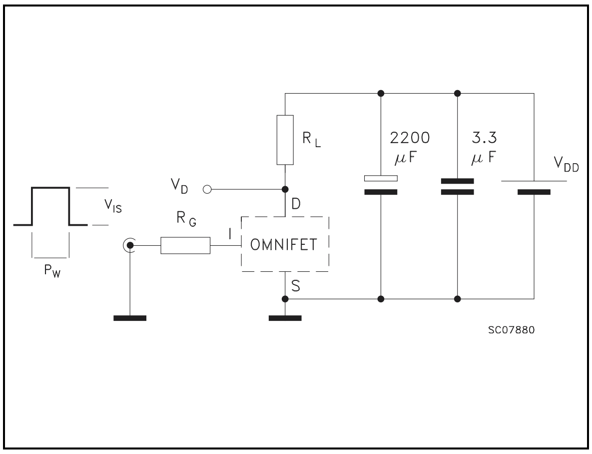


Figure 29. Input Charge Test Circuit

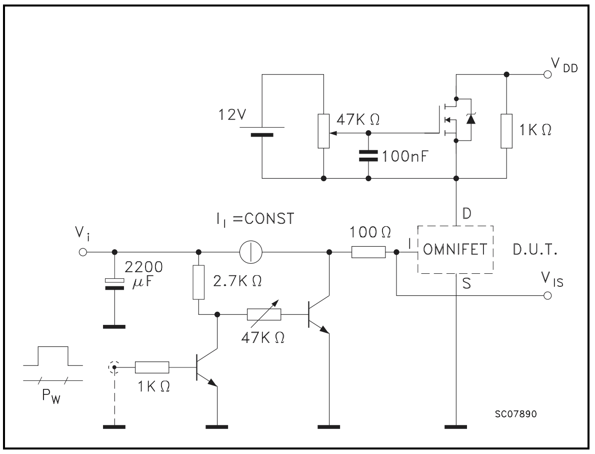


Figure 30. Test Circuit For Inductive Load Switching And Diode Recovery Times

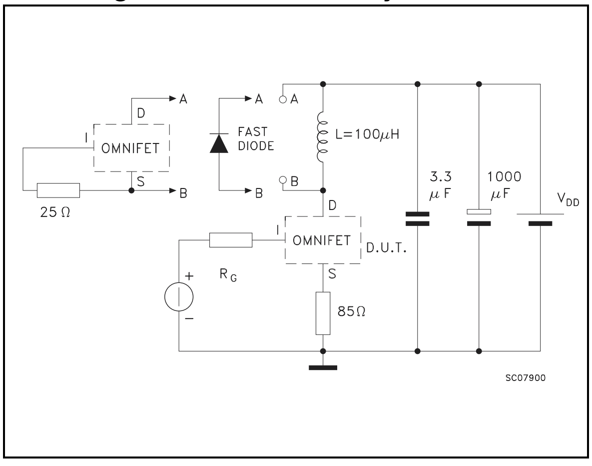
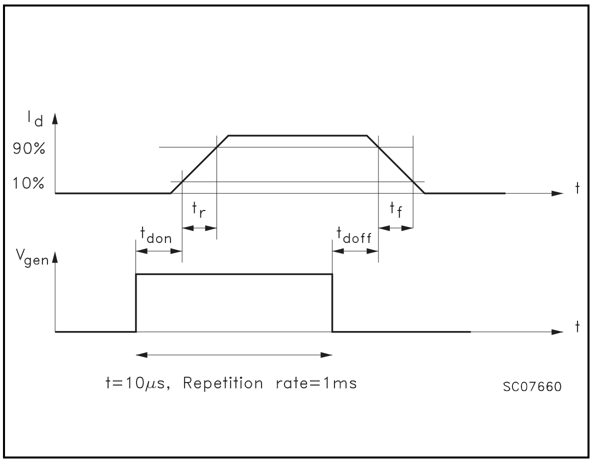


Figure 31. Waveforms

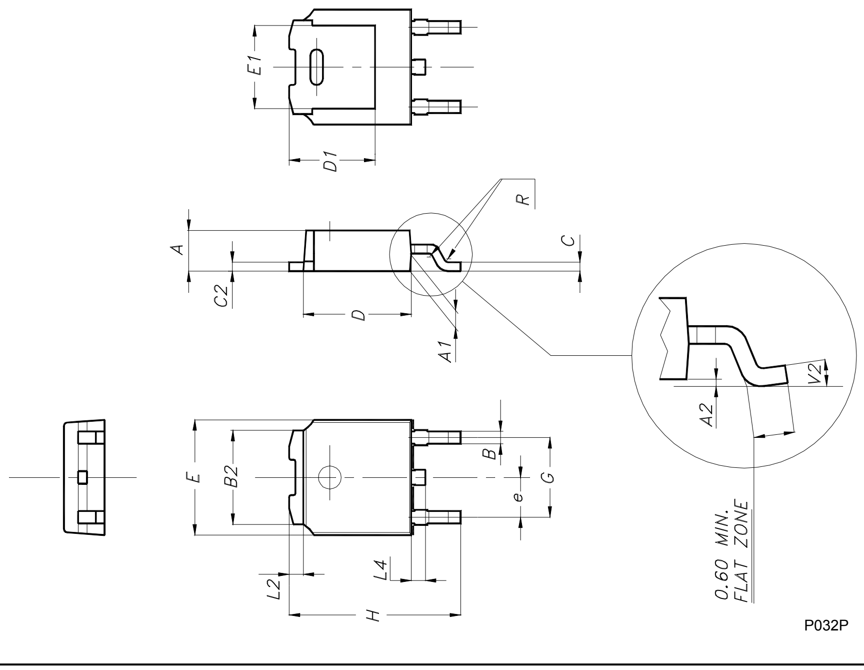


PACKAGE MECHANICAL

Table 11. DPAK Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
B	0.64		0.90
B2	5.20		5.40
C	0.45		0.60
C2	0.48		0.60
D	6.00		6.20
D1		5.1	
E	6.40		6.60
E1		4.7	
e		2.28	
G	4.40		4.60
H	9.35		10.10
L2		0.8	
L4	0.60		1.00
R		0.2	
V2	0°	8°	
Package Weight	Gr. 0.29		

Figure 32. DPAK Package Dimensions

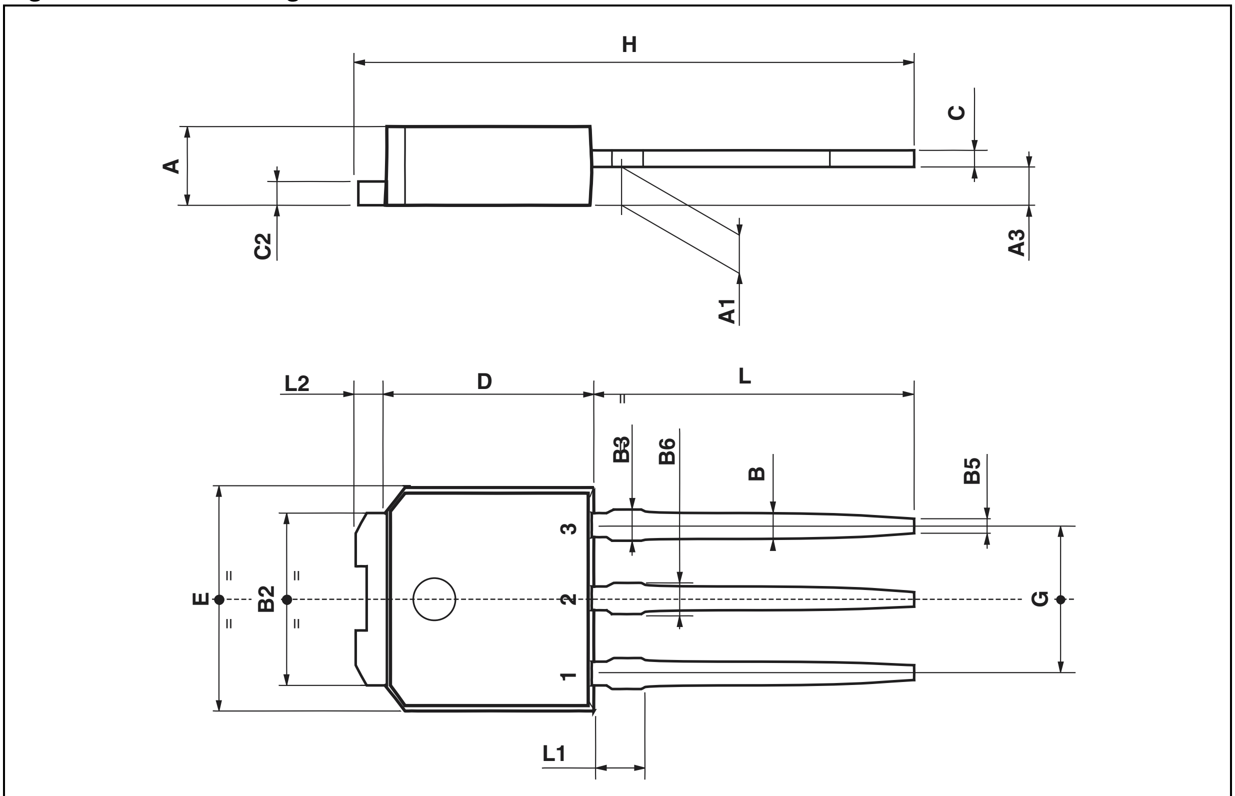


Note: Drawing is not to scale.

Table 12. IPAK Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A	2.2		2.4
A1	0.9		1.1
A3	0.7		1.3
B	0.64		0.9
B2	5.2		5.4
B3			0.85
B5		0.3	
B6			0.95
C	0.45		0.6
C2	0.48		0.6
D	6		6.2
E	6.4		6.6
G	4.4		4.6
H	15.9		16.3
L	9		9.4
L1	0.8		1.2
L2		0.8	1

Figure 33. IPAK Package Dimensions

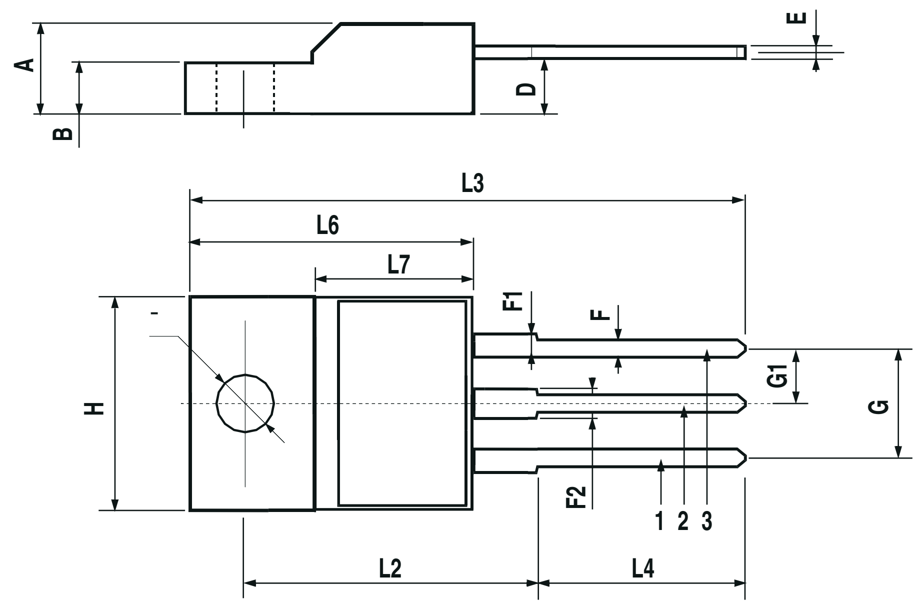


Note: Drawing is not to scale.

Table 13. ISOWATT220 Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.4		0.7
F	0.75		1
F1	1.15		1.7
F2	1.15		1.7
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L6	15.9		16.4
L7	9		9.3
	3		3.2

Figure 34. ISOWATT220 Package Dimensions

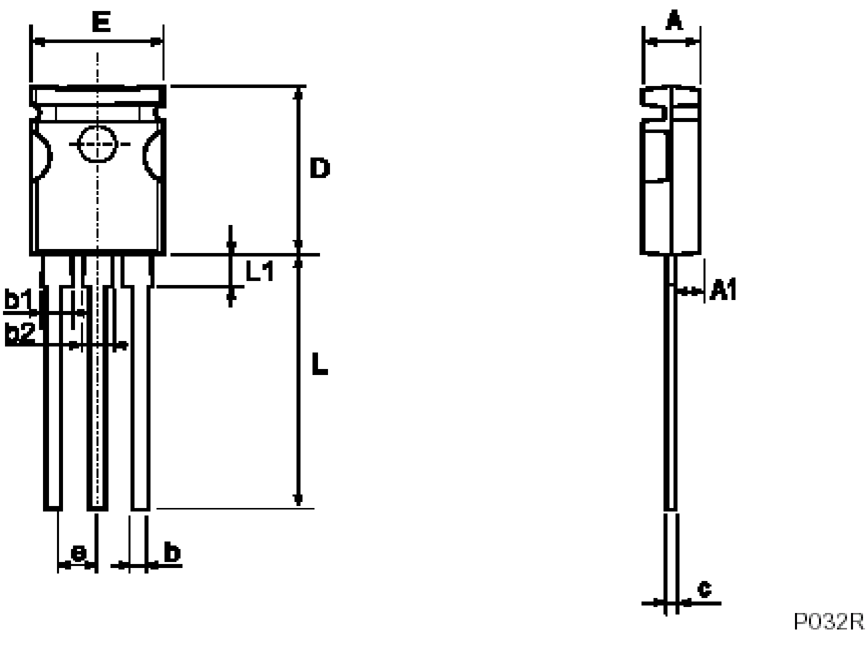


Note: Drawing is not to scale.

Table 14. SOT-82FM Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A	2.85		3.05
A1	1.47		1.67
b	0.40		0.60
b1	1.4		1.6
b2	1.3		1.5
c	0.45		0.6
D	10.5		10.9
e	2.2		2.8
E	7.45		7.75
L	15.5		15.9
L	1 1.95		2.35

Figure 35. SOT-82FM Package Dimensions



Note: Drawing is not to scale.

REVISION HISTORY

Table 15. Revision History

Date	Revision	Description of Changes
June-1996	1	First Issue
18-June-2004	2	Stylesheet update. No content change.