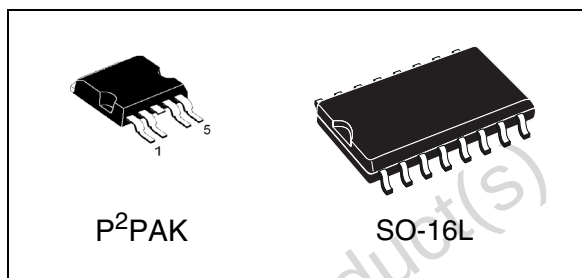


Features

Type	$R_{DS(on)}$	I_{OUT}	V_{CC}
VN920D-B5 VN920DSO	18 mΩ	30 A	36 V

- CMOS-compatible input
- On-state open load detection
- Off-state open load detection
- Shorted load protection
- Under-voltage and over-voltage shutdown
- Protection against loss of ground
- Very low standby current
- Reverse battery protected (see [Application schematic](#))



Description

The VN920D-B5 and VN920DSO are monolithic devices designed in STMicroelectronics VIPower M0-3 technology. The VN920D-B5 and VN920DSO are intended for driving any type of load with one side connected to ground. The active V_{CC} pin voltage clamp protects the devices against low energy spikes (see ISO7637 transient compatibility table).

Active current limitation combined with thermal shutdown and automatic restart protects the devices against overload. The devices detect the open load condition in both the on and off-state. In the off-state the devices detect if the output is shorted to V_{CC} . The devices automatically turn-off in the case where the ground pin becomes disconnected.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
P ² PAK	VN920D-B5	VN920D-B513TR
SO-16L	VN920DSO	VN920DSO13TR

Contents

1	Block diagram and pin description	5
2	Electrical specifications	6
2.1	Absolute maximum ratings	6
2.2	Thermal data	7
2.3	Electrical characteristics	8
2.4	Electrical characteristics curves	13
3	Application information	16
3.1	GND protection network against reverse battery	16
3.1.1	Solution 1: resistor in the ground line (RGND only)	16
3.1.2	Solution 2: diode (DGND) in the ground line	17
3.2	Load dump protection	17
3.3	MCU I/Os protection	17
3.4	P ² PAK maximum demagnetization energy (VCC = 13.5V)	18
3.5	SO-16L maximum demagnetization energy (VCC = 13.5V)	19
4	Package and PCB thermal data	20
4.1	SO-16L thermal data	20
4.2	P ² PAK thermal data	22
5	Package and packing information	25
5.1	ECOPACK [®] packages	25
5.2	P ² PAK mechanical data	27
5.3	SO-16L packing information	29
5.4	P ² PAK packing information	30
6	Revision history	31

List of tables

Table 1.	Device summary	1
Table 2.	Suggested connections for unused and not connected pins	5
Table 3.	Absolute maximum ratings	6
Table 4.	Thermal data.	7
Table 5.	Power	8
Table 6.	Switching ($V_{CC}=13V$)	8
Table 7.	Input pin	9
Table 8.	V_{CC} output diode.	9
Table 9.	Status pin	9
Table 10.	Protections	9
Table 11.	Open load detection	10
Table 12.	Truth table.	11
Table 13.	Electrical transient requirements	11
Table 14.	SO-16L thermal parameters	22
Table 15.	P ² PAK thermal parameters	24
Table 16.	SO-16L mechanical data	25
Table 17.	P ² PAK mechanical data	28
Table 18.	Document revision history	31

List of figures

Figure 1.	Block diagram	5
Figure 2.	Configuration diagram (top view)	5
Figure 3.	Current and voltage conventions	6
Figure 4.	Status timings	10
Figure 5.	Switching time waveforms	10
Figure 6.	Waveforms	12
Figure 7.	Off-state output current.	13
Figure 8.	High-level input current.	13
Figure 9.	Input clamp voltage.	13
Figure 10.	Status leakage current	13
Figure 11.	Status low output voltage	13
Figure 12.	Status clamp voltage	13
Figure 13.	On-state resistance Vs T_{case}	14
Figure 14.	On-state resistance Vs V_{CC}	14
Figure 15.	Over-voltage shutdown.	14
Figure 16.	Input high-level	14
Figure 17.	Input low-level.	14
Figure 18.	Input hysteresis voltage	14
Figure 19.	I_{lim} Vs T_{case}	15
Figure 20.	Turn-on voltage slope	15
Figure 21.	Turn-off voltage slope	15
Figure 22.	Application schematic	16
Figure 23.	P ² PAK maximum turn-off current versus inductance	18
Figure 24.	SO-16L maximum turn-off current versus inductance	19
Figure 25.	SO-16L PC board	20
Figure 26.	SO-16L $R_{thj-amb}$ Vs PCB copper area in open box free air condition	20
Figure 27.	SO-16L thermal impedance junction ambient single pulse	21
Figure 28.	Thermal fitting model of a single channel HSD in SO-16L	21
Figure 29.	P ² PAK PC board	22
Figure 30.	P ² PAK $R_{thj-amb}$ Vs. PCB copper area in open box free air condition	23
Figure 31.	P ² PAK thermal impedance junction ambient single pulse	23
Figure 32.	Thermal fitting model of a single channel HSD in P ² PAK.	24
Figure 33.	SO-16L package dimensions	25
Figure 34.	P ² PAK package dimensions.	27
Figure 35.	SO-16L tube shipment (no suffix)	29
Figure 36.	SO-16L tape and reel shipment (suffix "TR")	29
Figure 37.	P ² PAK tube shipment (no suffix)	30
Figure 38.	P ² PAK tape and reel (suffix "13TR").	30

1 Block diagram and pin description

Figure 1. Block diagram

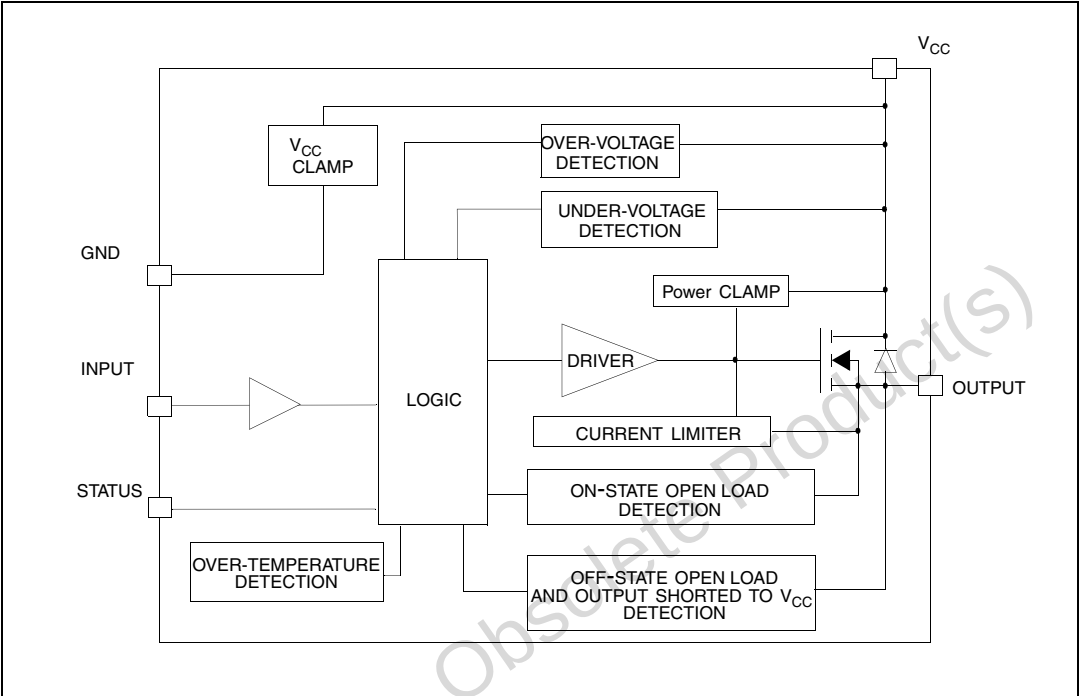


Figure 2. Configuration diagram (top view)

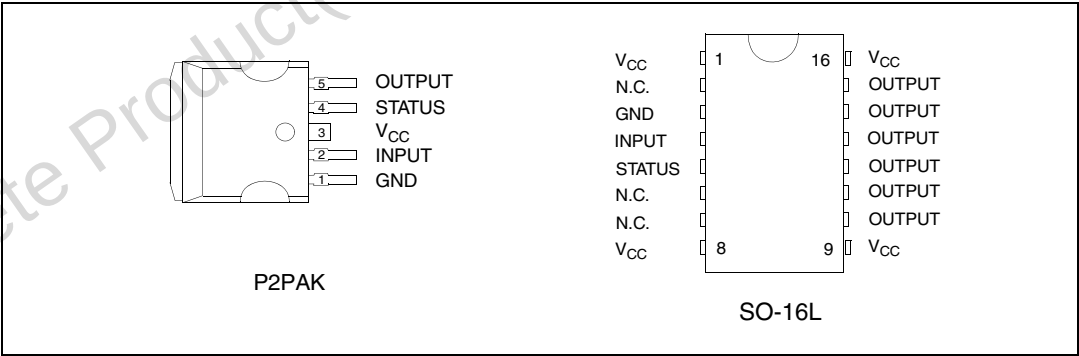
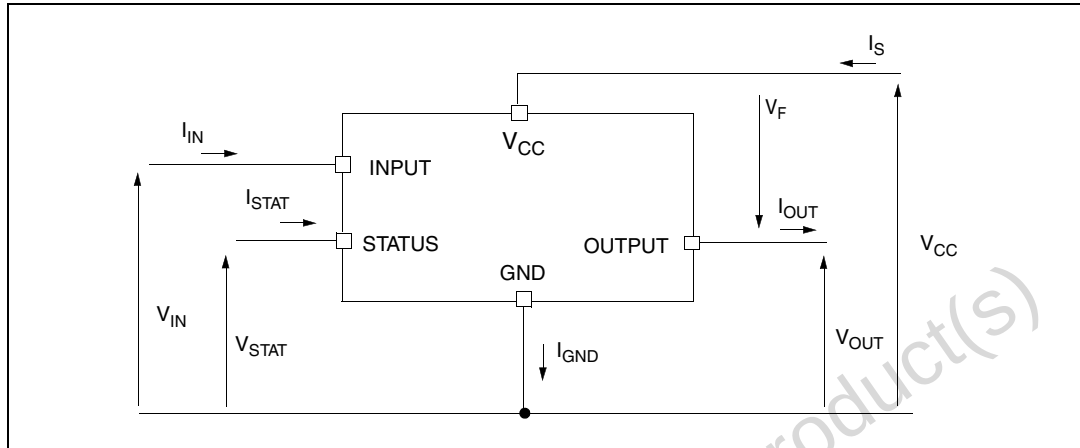


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Status	N.C.	Output	Input
Floating	X	X	X	X
To ground		X		Through 10KΩ resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to Absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics sure program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		SO-16L	P ² PAK	
V_{CC}	DC supply voltage	41		V
$-V_{CC}$	Reverse DC supply voltage	- 0.3		V
$-I_{gnd}$	DC reverse ground pin current	- 200		mA
I_{OUT}	DC output current	Internally limited		A
$-I_{OUT}$	Reverse DC output current	- 25		A
I_{IN}	DC input current	+/- 10		mA
I_{STAT}	DC Status current	+/- 10		mA
V_{ESD}	Electrostatic discharge (human body model: $R = 1.5K\Omega$, $C = 100pF$)			
	- INPUT	4000		V
	- STATUS	4000		V
	- OUTPUT	5000		V
	- V_{CC}	5000		V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value		Unit
		SO-16L	P ² PAK	
E _{MAX}	Maximum switching energy (L = 0.25mH; R _L = 0Ω; V _{bat} = 13.5V; T _{Jstart} = 150°C; I _L = 45A)	352	364	mJ
P _{tot}	Power dissipation T _C = 25°C	8.3	96.1	W
T _j	Junction operating temperature	Internally limited		°C
T _C	Case operating temperature	- 40 to 150		°C
T _{stg}	Storage temperature	- 55 to 150		°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max. value		Unit
		SO-16L	P ² PAK	
R _{thj-case}	Thermalresistance junction-case	-	1.3	°C/W
R _{thj-lead}	Thermalresistance junction-lead	15	-	°C/W
R _{thj-amb}	Thermalresistance junction-ambient	65 ⁽¹⁾	51.3 ⁽²⁾	°C/W

1. When mounted on FR4 printed circuit board with 0.5cm² of Cu (at least 35μm thick) connected to all V_{CC} pins.
2. When mounted on a standard single-sided FR-4 board with 0.5cm² of Cu (at least 35μm thick).

2.3 Electrical characteristics

Values specified in this section are for $8V < V_{CC} < 36V$; $-40^{\circ}C < T_j < 150^{\circ}C$, unless otherwise stated.

Table 5. Power

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		5.5	13	36	V
V_{USD}	Under-voltage shutdown		3	4	5.5	V
$V_{USDhyst}$	Under-voltage shutdown hysteresis			0.5		V
V_{OV}	Over-voltage shutdown		36			V
R_{ON}	On-state resistance	$I_{OUT} = 10A$; $T_j = 25^{\circ}C$; $I_{OUT} = 10A$; $I_{OUT} = 3A$; $V_{CC} = 6V$			18 36 50	mΩ mΩ mΩ
I_S	Supply current	Off-state; $V_{CC} = 13V$; $V_{IN} = V_{OUT} = 0V$ Off-state; $V_{CC} = 13V$; $V_{IN} = V_{OUT} = 0V$; $T_j = 25^{\circ}C$ On-state; $V_{CC} = 13V$; $V_{IN} = 5V$; $I_{OUT} = 0A$		10 10	25 20 3.5	μA μA mA
$I_{L(off1)}$	Off-state output current	$V_{IN} = V_{OUT} = 0V$	0		50	μA
$I_{L(off2)}$	Off-state output current	$V_{IN} = 0V$; $V_{OUT} = 3.5V$	-75		0	μA
$I_{L(off3)}$	Off-state output current	$V_{IN} = V_{OUT} = 0V$; $V_{CC} = 13V$; $T_j = 125^{\circ}C$			5	μA
$I_{L(off4)}$	Off-state output current	$V_{IN} = V_{OUT} = 0V$; $V_{CC} = 13V$; $T_j = 25^{\circ}C$			3	μA

Table 6. Switching ($V_{CC}=13V$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 1.3\Omega$		50		μs
$t_{d(off)}$	Turn-off delay time	$R_L = 1.3\Omega$		50		μs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	$R_L = 1.3\Omega$	See Figure 20 .			V/μs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	$R_L = 1.3\Omega$	See Figure 21 .			V/μs

Table 7. Input pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low-level				1.25	V
I_{IL}	Low-level input current	$V_{IN} = 1.25V$	1			μA
V_{IH}	Input high-level		3.25			V
I_{IH}	High-level input current	$V_{IN} = 3.25V$			10	μA
V_{hyst}	Input hysteresis voltage		0.5			V
V_{ICL}	Input clamp voltage	$I_{IN} = 1mA$ $I_{IN} = -1mA$	6	6.8 - 0.7	8	V V

Table 8. V_{CC} output diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_F	Forward on voltage	- $I_{OUT} = 5.5A$; $T_j = 150^\circ C$			0.7	V

Table 9. Status pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status low output voltage	$I_{STAT} = 1.6mA$			0.5	V
I_{LSTAT}	Status leakage current	Normal operation; $V_{STAT} = 5V$			10	μA
C_{STAT}	Status pin input capacitance	Normal operation; $V_{STAT} = 5V$			100	pF
V_{SCL}	Status clamp voltage	$I_{STAT} = 1mA$ $I_{STAT} = -1mA$	6	6.8 - 0.7	8	V V

Table 10. Protections⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{TSD}	Shutdown temperature		150	175	200	$^\circ C$
T_R	Reset temperature		135			$^\circ C$
T_{hyst}	Thermal hysteresis		7	15		$^\circ C$
t_{SDL}	Status delay in overload condition	$T_j > T_{jsh}$			20	ms
I_{lim}	Current limitation	$5.5V < V_{CC} < 36V$	30	45	75 75	A A
V_{demag}	Turn-off output clamp voltage	$I_{OUT} = 2A$; $V_{IN} = 0V$; $L = 6mH$	$V_{CC} - 41$	$V_{CC} - 48$	$V_{CC} - 55$	V

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device operates under abnormal conditions this software must limit the duration and number of activation cycles.

Table 11. Open load detection

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{OL}	Open load on-state detection threshold	$V_{IN} = 5V$	300	500	700	mA
$t_{DOL(on)}$	Open load on-state detection delay	$I_{OUT} = 0A$			250	μs
V_{OL}	Open load off-state voltage detection threshold	$V_{IN} = 0V$	1.5	2.5	3.5	V
$t_{DOL(off)}$	Open load detection delay at turn-off				1000	μs

Figure 4. Status timings

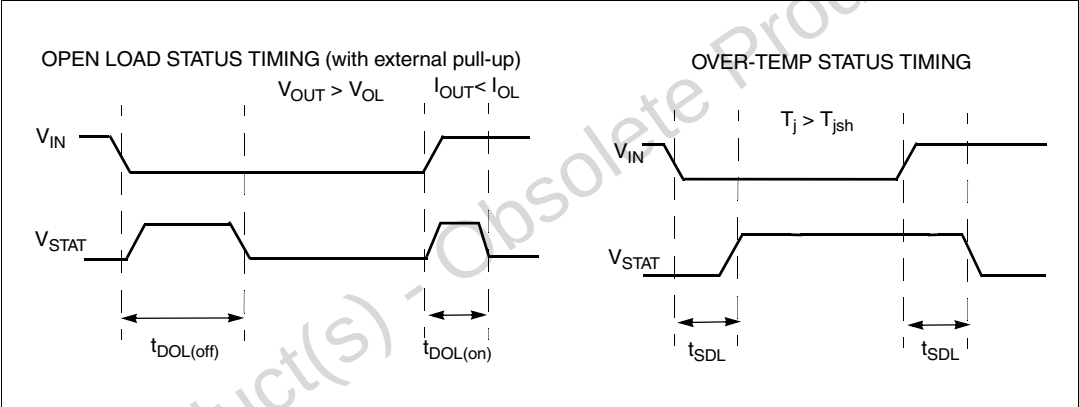


Figure 5. Switching time waveforms

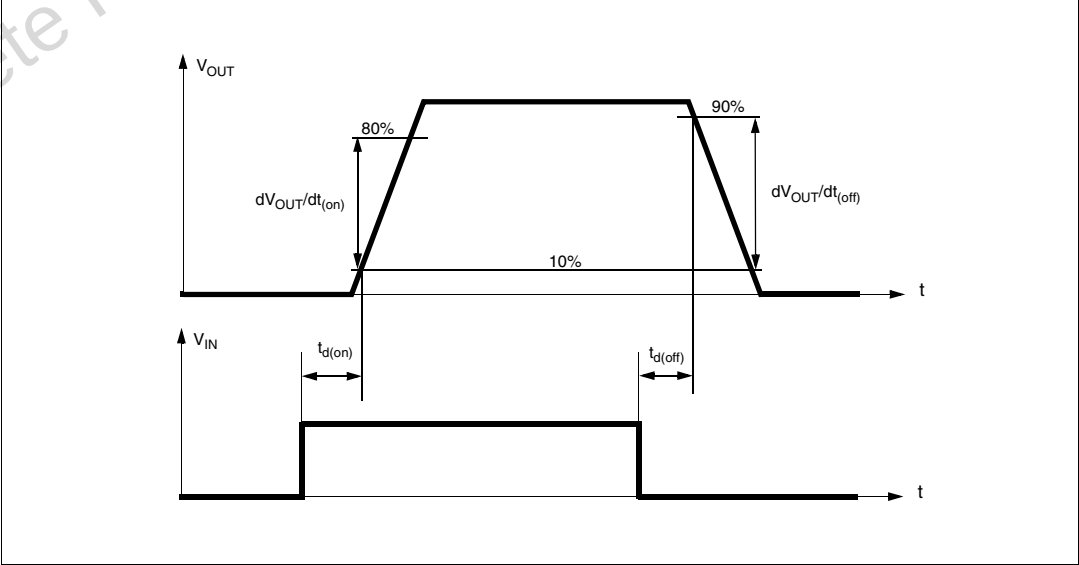


Table 12. Truth table

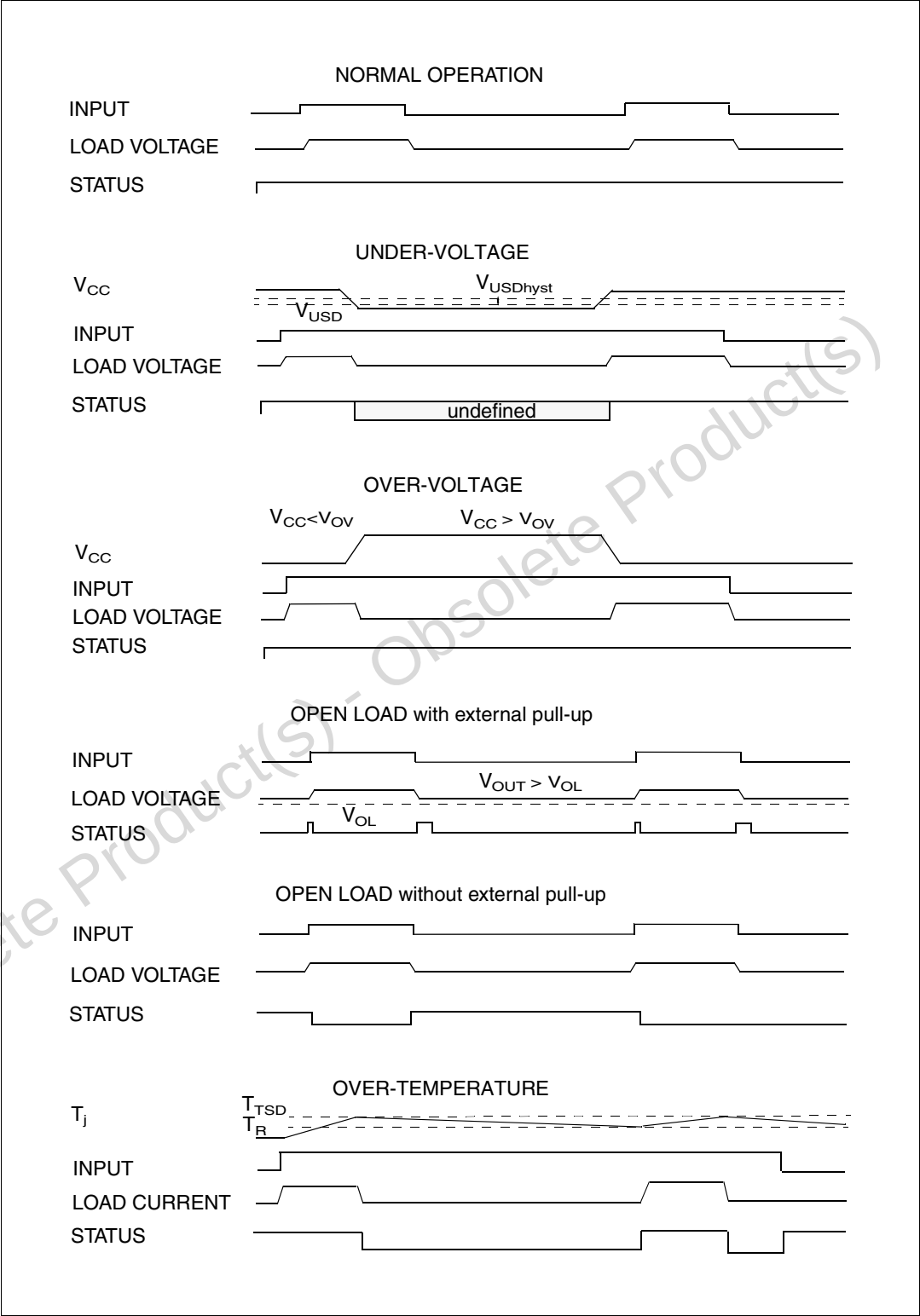
Conditions	Input	Output	Status
Normal operation	L	L	H
	H	H	H
Current limitation	L	L	H
	H	X	$(T_j < T_{TSD})$ H $(T_j > T_{TSD})$ L
Over-temperature	L	L	H
	H	L	L
Under-voltage	L	L	X
	H	L	X
Over-voltage	L	L	H
	H	L	H
Output voltage > V_{OL}	L	H	L
	H	H	H
Output current < I_{OL}	L	L	H
	H	H	L

Table 13. Electrical transient requirements

ISO T/R 7637/1 Test pulse	Test level				
	I	II	III	IV	Delays and impedance
1	- 25V ⁽¹⁾	- 50V ⁽¹⁾	- 75V ⁽¹⁾	- 100V ⁽¹⁾	2ms, 10Ω
2	+ 25V ⁽¹⁾	+ 50V ⁽¹⁾	+ 75V ⁽¹⁾	+ 100V ⁽¹⁾	0.2ms, 10Ω
3a	- 25V ⁽¹⁾	- 50V ⁽¹⁾	- 100V ⁽¹⁾	- 150V ⁽¹⁾	0.1μs, 50Ω
3b	+ 25V ⁽¹⁾	+ 50V ⁽¹⁾	+ 75V ⁽¹⁾	+ 100V ⁽¹⁾	0.1μs, 50Ω
4	- 4V ⁽¹⁾	- 5V ⁽¹⁾	- 6V ⁽¹⁾	- 7V ⁽¹⁾	100ms, 0.01Ω
5	+ 26.5V ⁽¹⁾	+ 46.5V ⁽²⁾	+ 66.5V ⁽²⁾	+ 86.5V ⁽²⁾	400ms, 2Ω

1. All functions of the device are performed as designed after exposure to disturbance.
2. One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

Figure 6. Waveforms



2.4 Electrical characteristics curves

Figure 7. Off-state output current

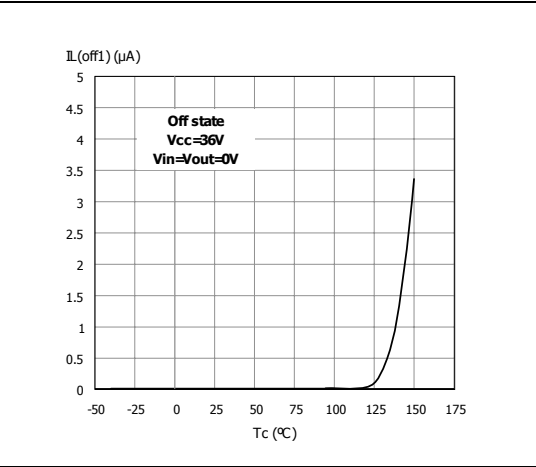


Figure 8. High-level input current

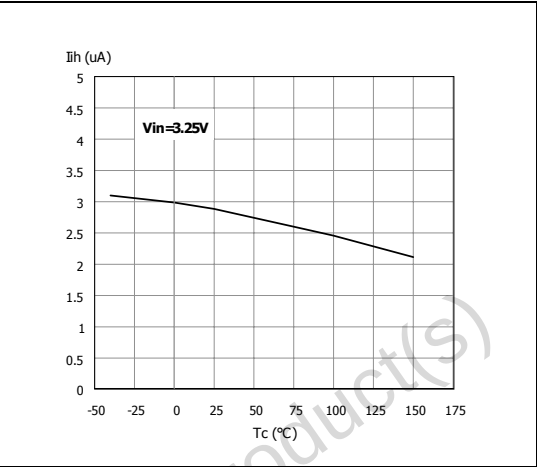


Figure 9. Input clamp voltage

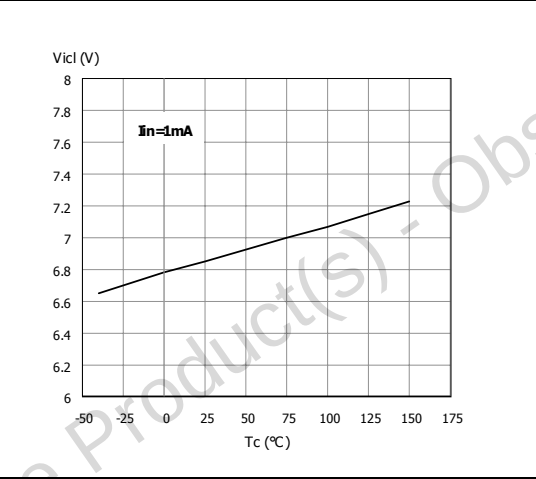


Figure 10. Status leakage current

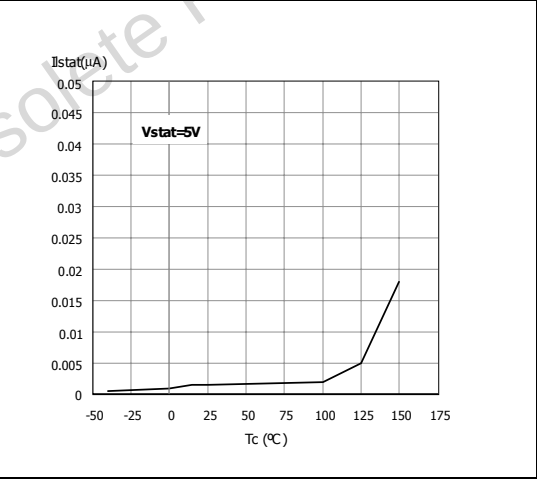


Figure 11. Status low output voltage

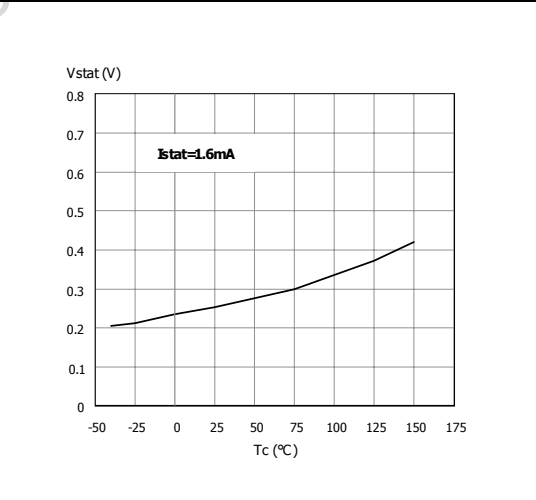


Figure 12. Status clamp voltage

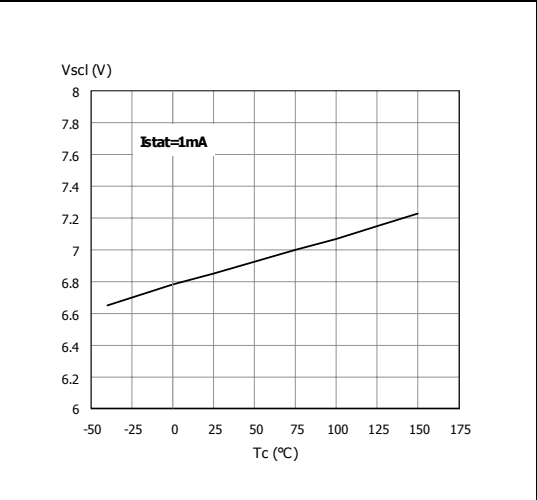


Figure 13. On-state resistance Vs T_{case}

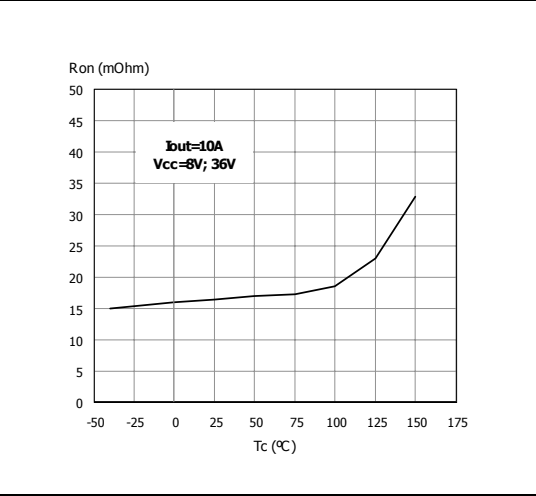


Figure 14. On-state resistance Vs V_{CC}

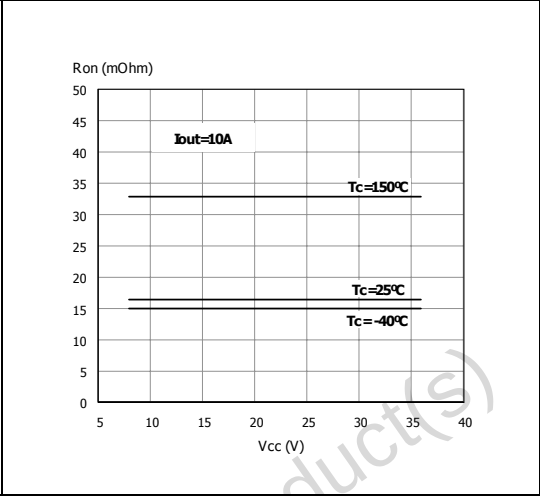


Figure 15. Over-voltage shutdown

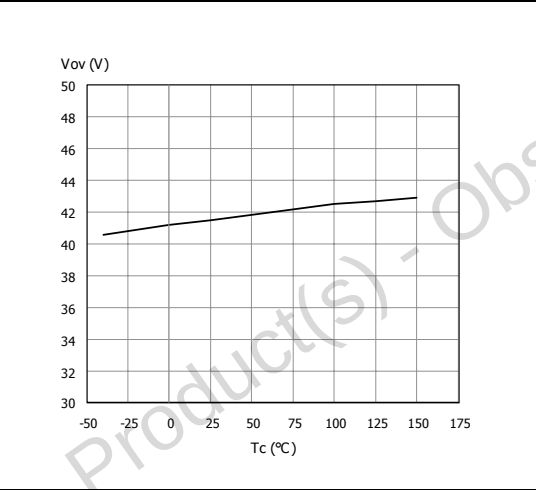


Figure 16. Input high-level

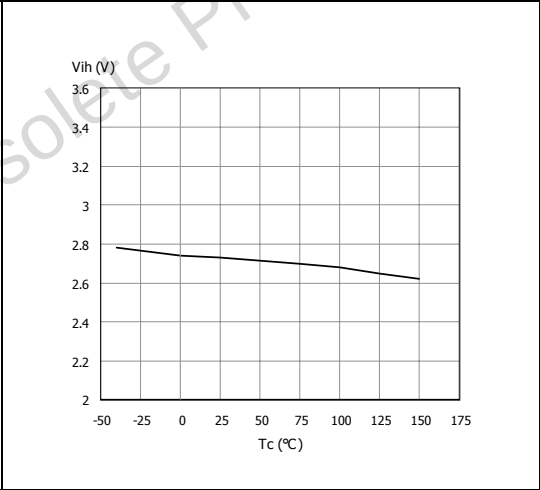


Figure 17. Input low-level

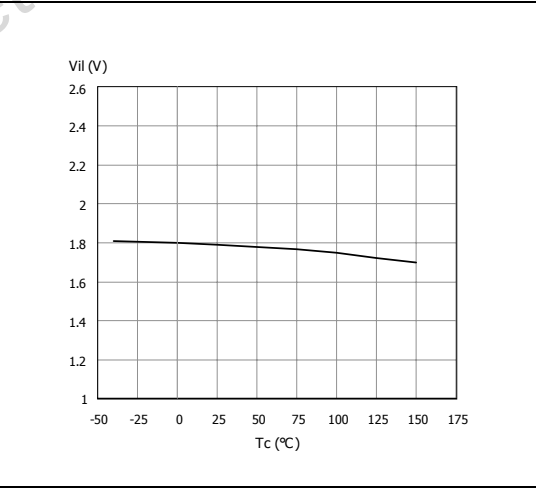


Figure 18. Input hysteresis voltage

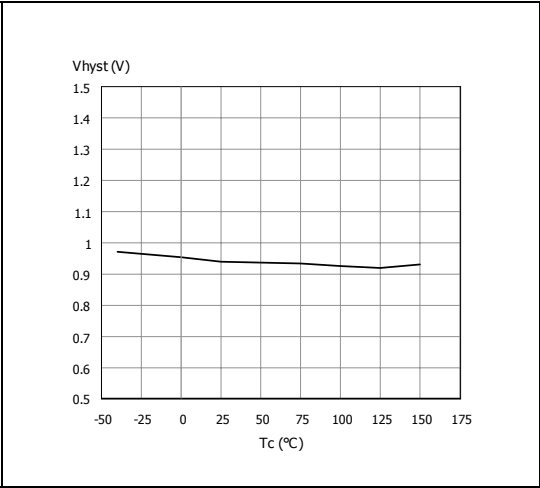


Figure 19. I_{lim} Vs T_{case}

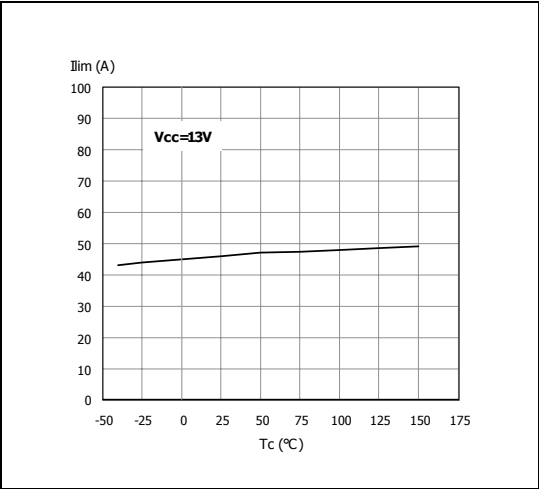


Figure 20. Turn-on voltage slope

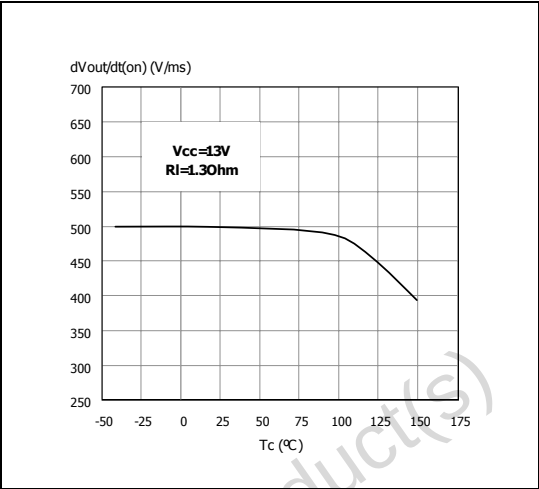
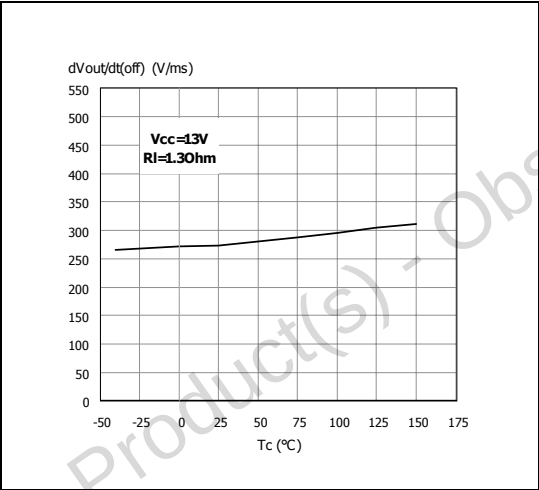


Figure 21. Turn-off voltage slope



3.1.2 Solution 2: diode (D_{GND}) in the ground line

A resistor ($R_{GND} = 1k\Omega$) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift ($\approx 600mV$) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the absolute maximum rating.

Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

3.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

3.3 MCU I/Os protection

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the μC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of μC I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

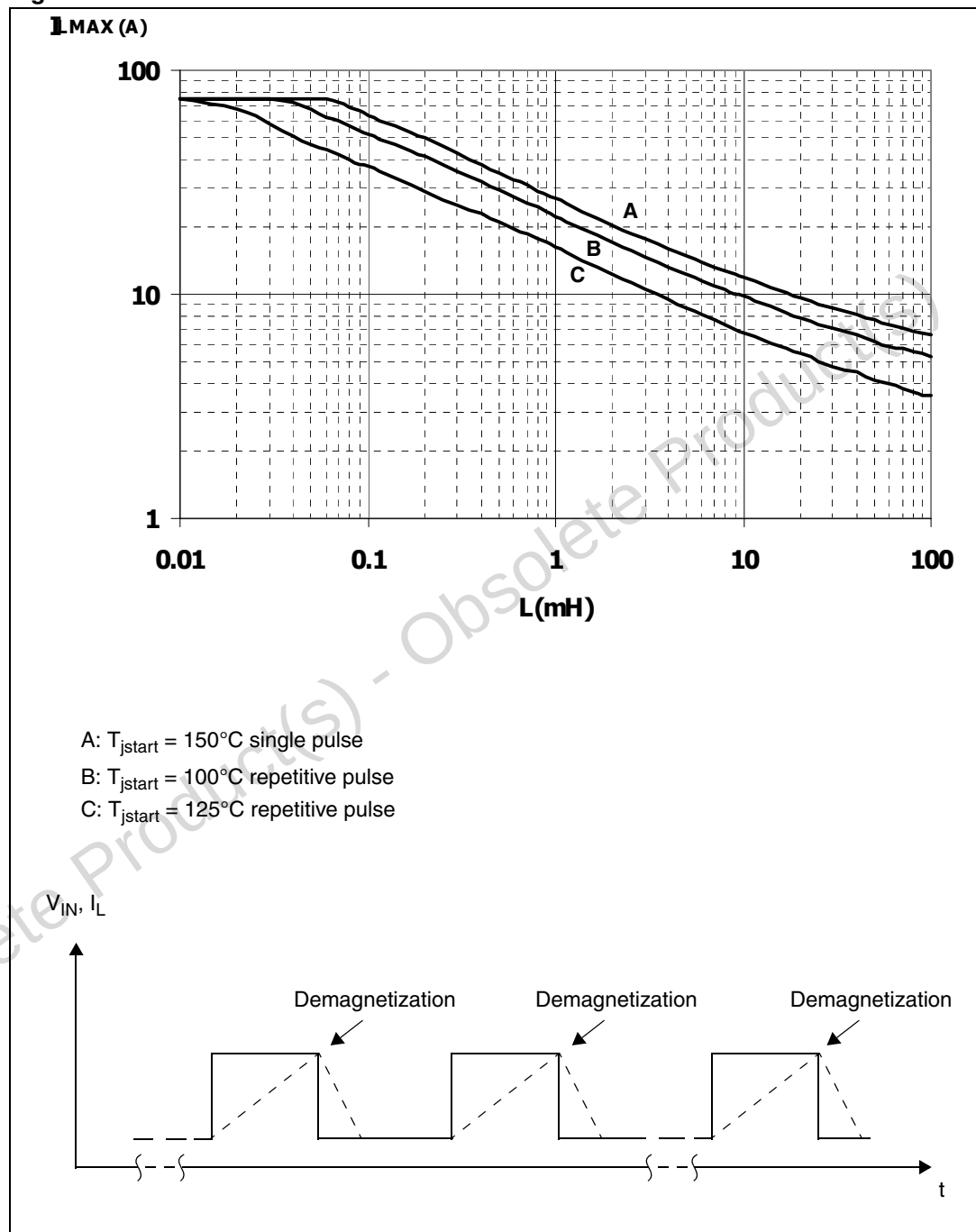
For $V_{CCpeak} = -100V$ and $I_{latchup} \geq 20mA$; $V_{OH\mu C} \geq 4.5V$

$$5k\Omega \leq R_{prot} \leq 65k\Omega$$

Recommended values: $R_{prot} = 10k\Omega$.

3.4 P²PAK maximum demagnetization energy ($V_{CC} = 13.5V$)

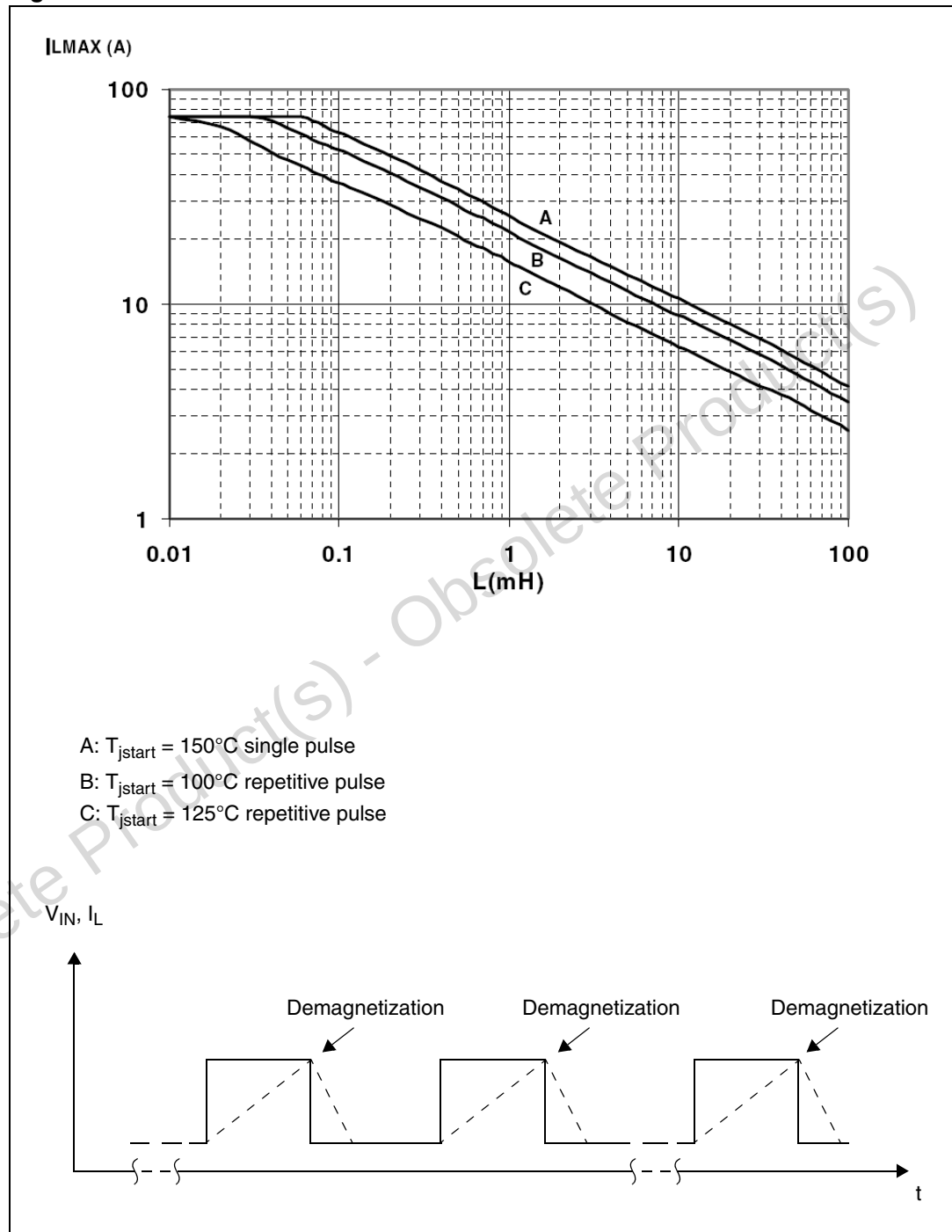
Figure 23. P²PAK maximum turn-off current versus inductance



Note: Values are generated with $R_L = 0 \Omega$. In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

3.5 SO-16L maximum demagnetization energy ($V_{CC} = 13.5V$)

Figure 24. SO-16L maximum turn-off current versus inductance

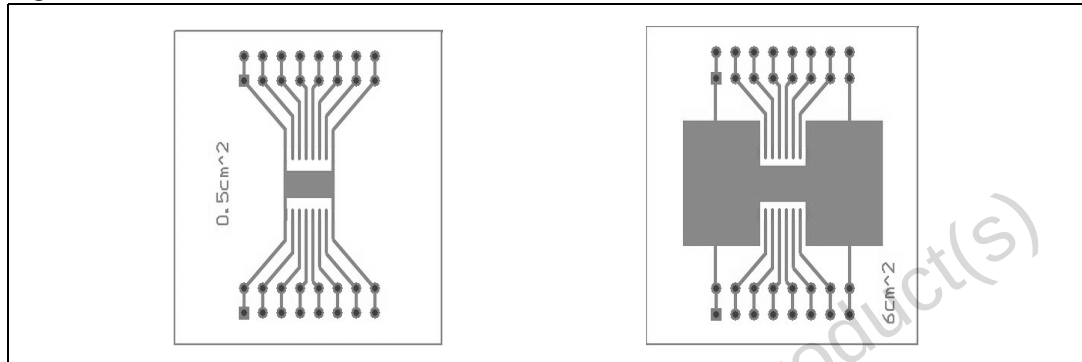


Note: Values are generated with $R_L = 0 \Omega$. In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PCB thermal data

4.1 SO-16L thermal data

Figure 25. SO-16L PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 41mm x 48mm, PCB thickness = 2mm, Cu thickness = 35 μ m, Copper areas: 0.5cm², 6cm²).

Figure 26. SO-16L $R_{thj-amb}$ Vs PCB copper area in open box free air condition

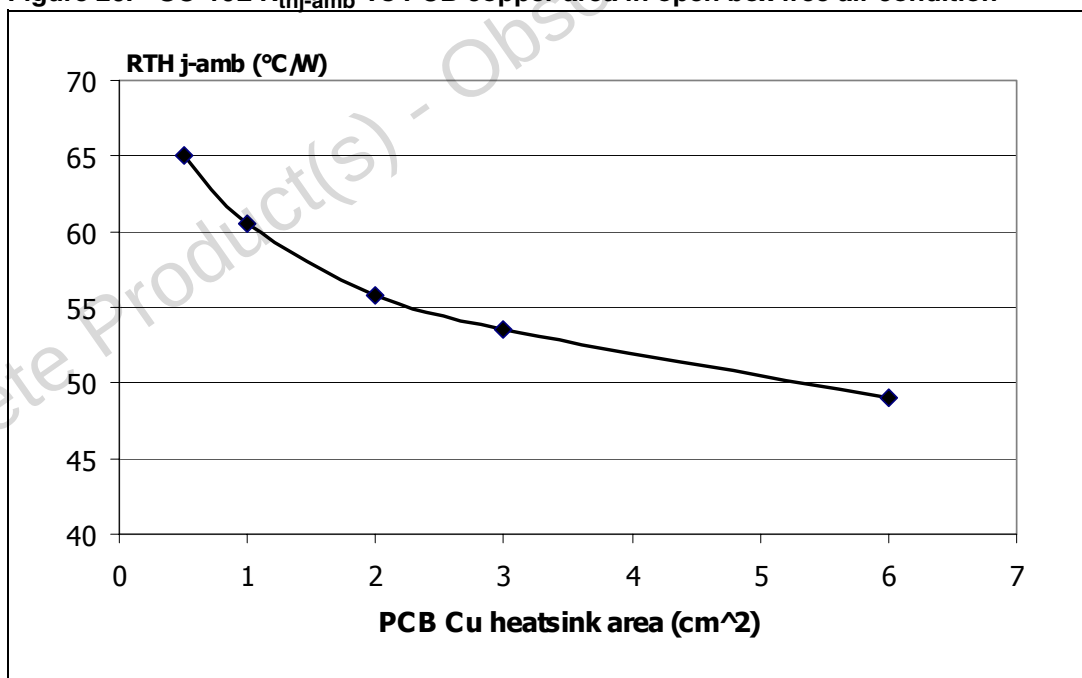
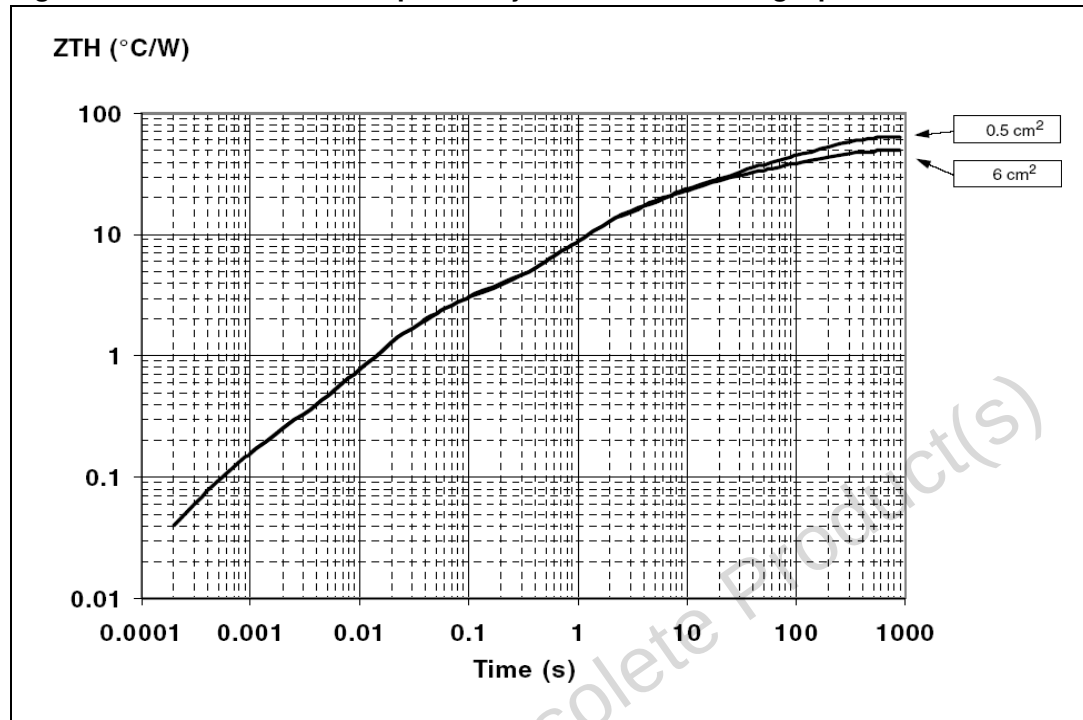


Figure 27. SO-16L thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

$$\text{where } \delta = t_p / T$$

Figure 28. Thermal fitting model of a single channel HSD in SO-16L

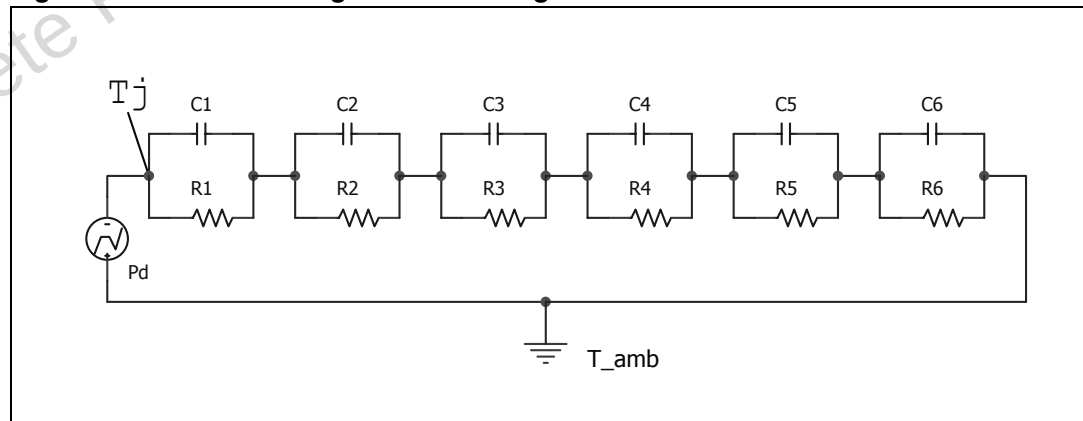


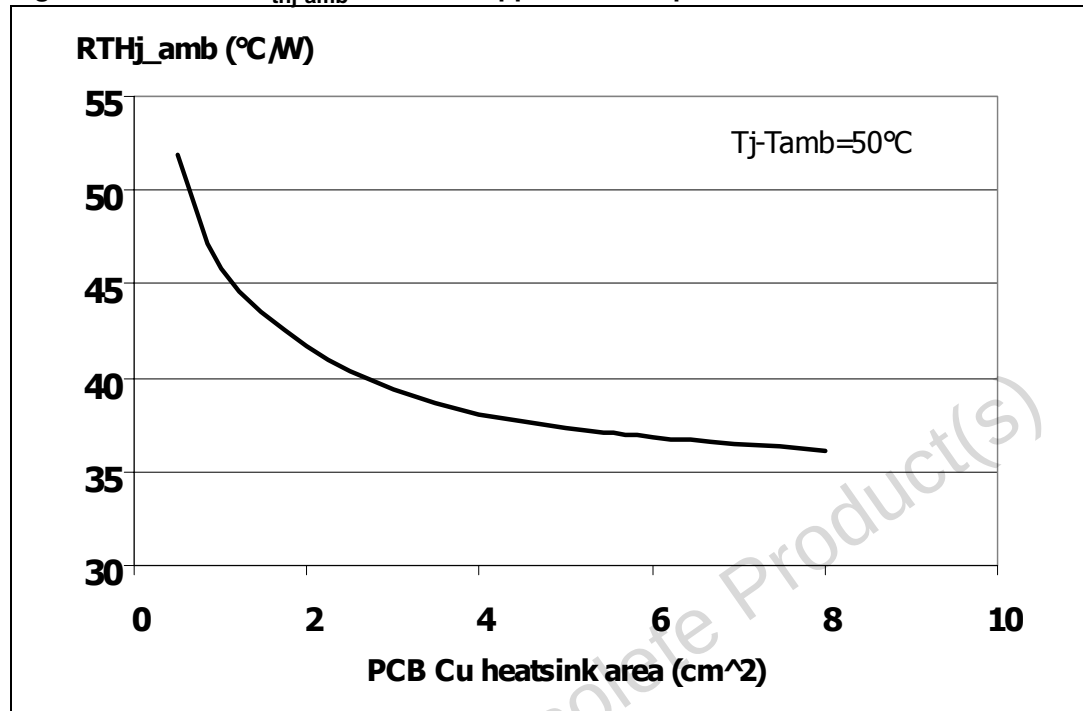
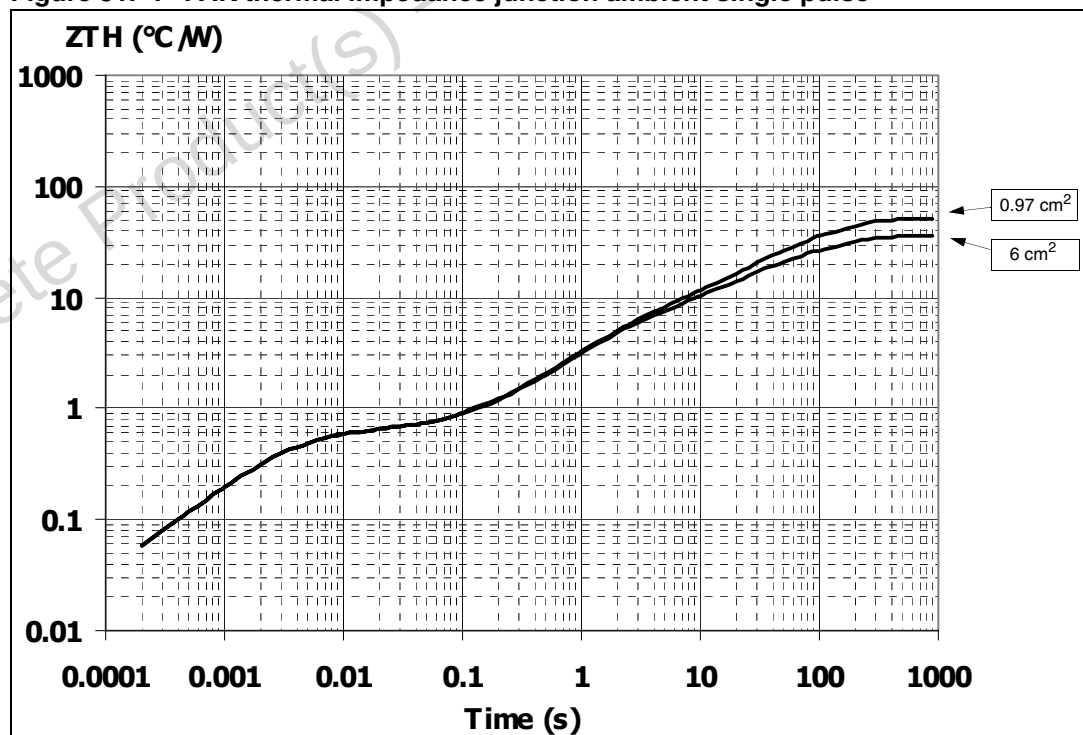
Table 14. SO-16L thermal parameters

Area / island (cm ²)	Footprint	6
R1 (°C/W)	0.02	
R2 (°C/W)	0.1	
R3 (°C/W)	2.2	
R4 (°C/W)	12	
R5 (°C/W)	15	
R6 (°C/W)	35	20
C1 (W.s/°C)	0.0015	
C2 (W.s/°C)	7E-03	
C3 (W.s/°C)	1.5E-02	
C4 (W.s/°C)	0.14	
C5 (W.s/°C)	1	
C6 (W.s/°C)	5	8

4.2 P²PAK thermal data

Figure 29. P²PAK PC board

Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 60mm x 60mm, PCB thickness = 2 mm, Cu thickness = 35μm, Copper areas: 0.97cm², 8cm²).

Figure 30. P²PAK $R_{thj-amb}$ Vs. PCB copper area in open box free air conditionFigure 31. P²PAK thermal impedance junction ambient single pulse

Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 32. Thermal fitting model of a single channel HSD in P²PAK

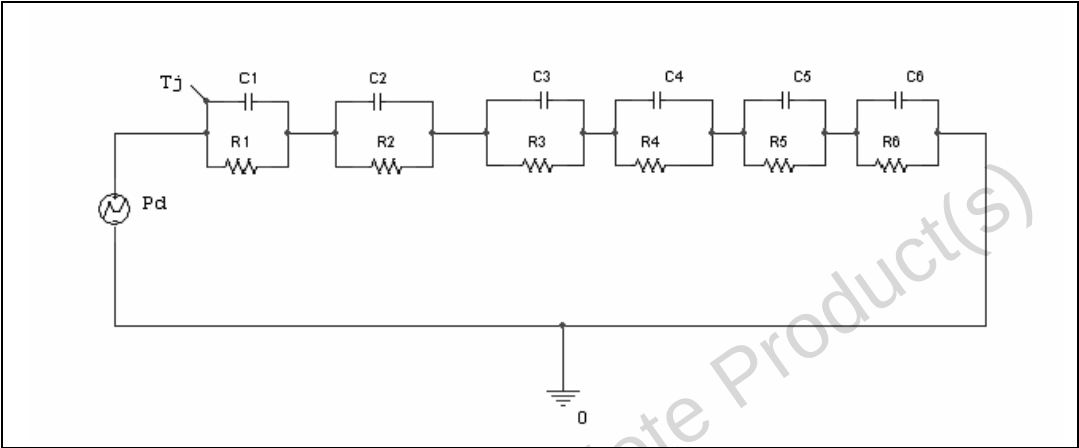


Table 15. P²PAK thermal parameters

Area/island (cm ²)	0.97	6
R1 (°C/W)	0.02	
R2 (°C/W)	0.1	
R3 (°C/W)	0.22	
R4 (°C/W)	4	
R5 (°C/W)	9	
R6 (°C/W)	37	22
C1 (W·s/°C)	0.0015	
C2 (W·s/°C)	0.007	
C3 (W·s/°C)	0.015	
C4 (W·s/°C)	0.4	
C5 (W·s/°C)	2	
C6 (W·s/°C)	3	5

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 33. SO-16L package dimensions

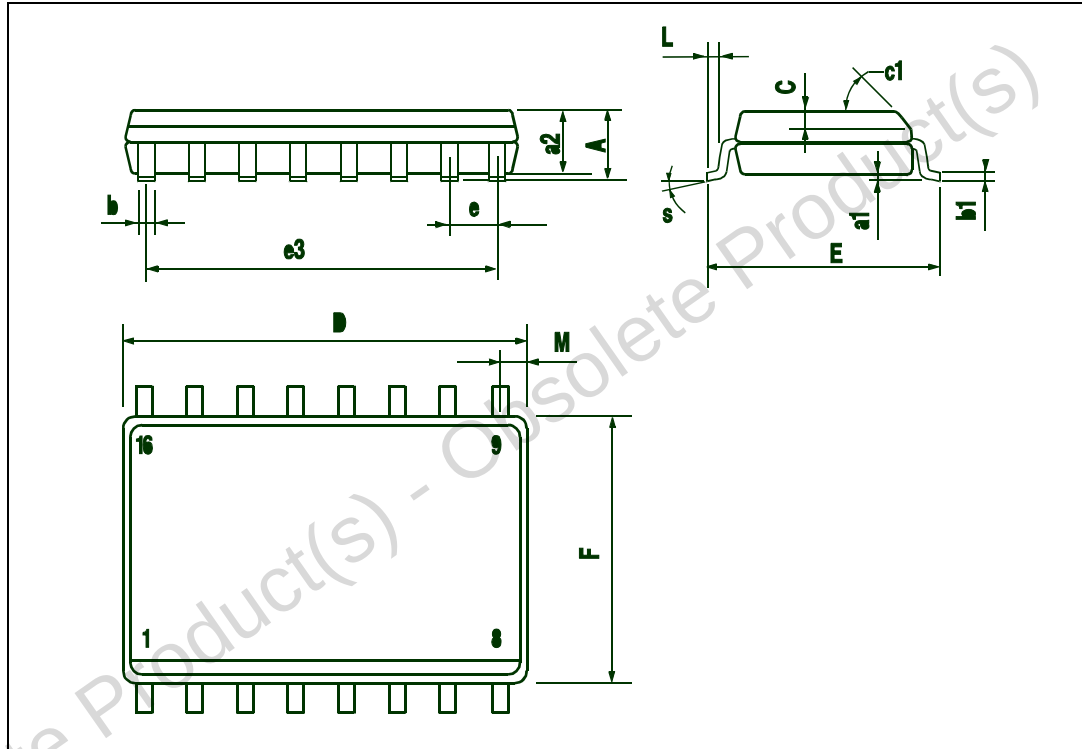


Table 16. SO-16L mechanical data

DIM.	mm.		
	Min.	Typ.	Max.
A			2.65
a1	0.1		0.2
a2			2.45
b	0.35		0.49
b1	0.23		0.32
C		0.5	
c1	45° (typ.)		

Table 16. SO-16L mechanical data (continued)

DIM.	mm.		
	Min.	Typ.	Max.
D	10.1		10.5
E	10.0		10.65
e		1.27	
e3		8.89	
F	7.4		7.6
L	0.5		1.27
M			0.75
S	8° (max.)		

5.2 P²PAK mechanical data

Figure 34. P²PAK package dimensions

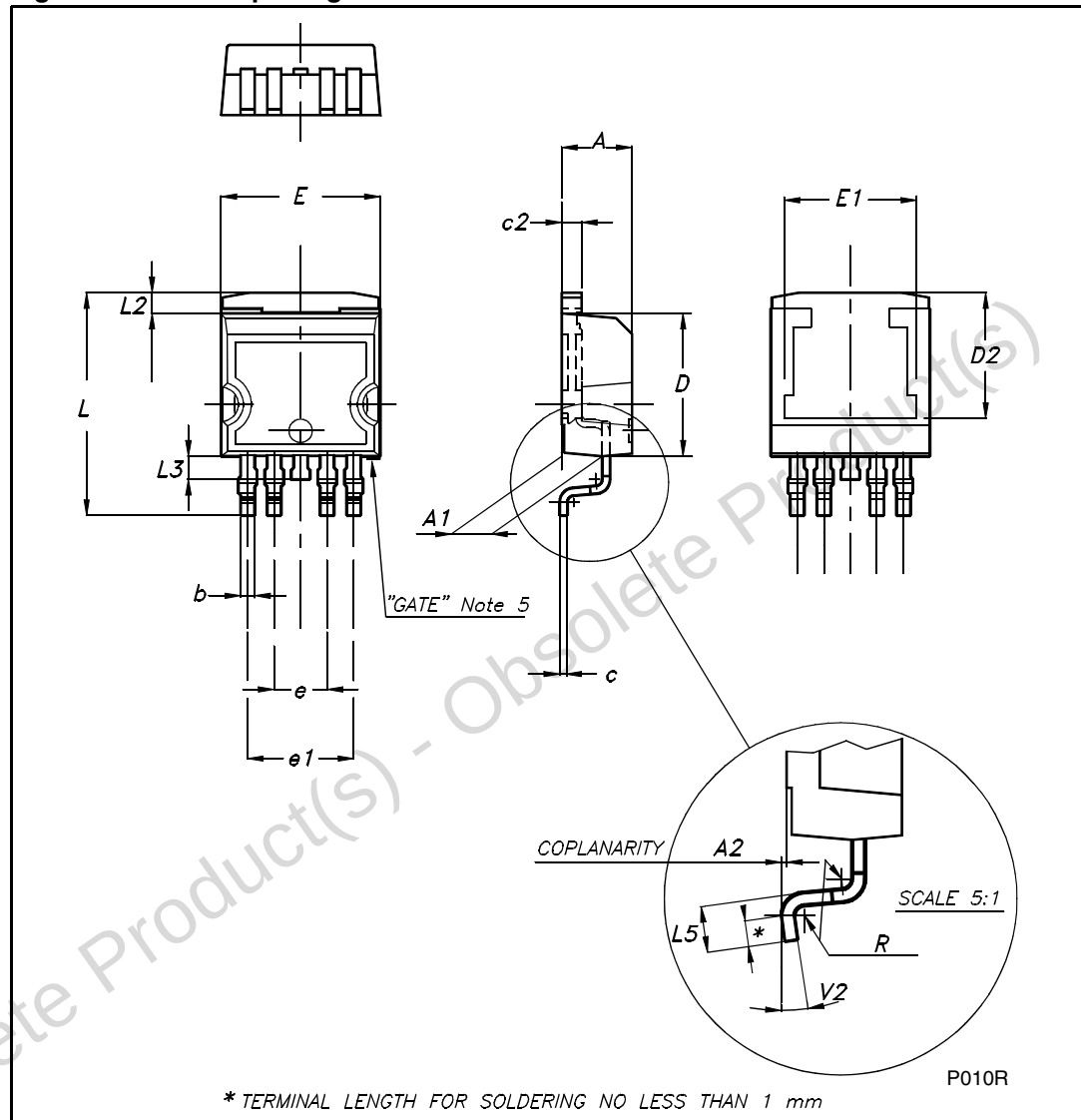


Table 17. P²PAK mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	2.40		2.80
A2	0.03		0.23
b	0.80		1.05
c	0.45		0.60
c2	1.17		1.37
D	8.95		9.35
D2		8.00	
E	10.00		10.40
E1		8.50	
e	3.20		3.60
e1	6.60		7.00
L	13.70		14.50
L2	1.25		1.40
L3	0.90		1.70
L5	1.55		2.40
R		0.40	
V2	0°		8°
Package weight	1.40 Gr (typ)		

5.3 SO-16L packing information

Figure 35. SO-16L tube shipment (no suffix)

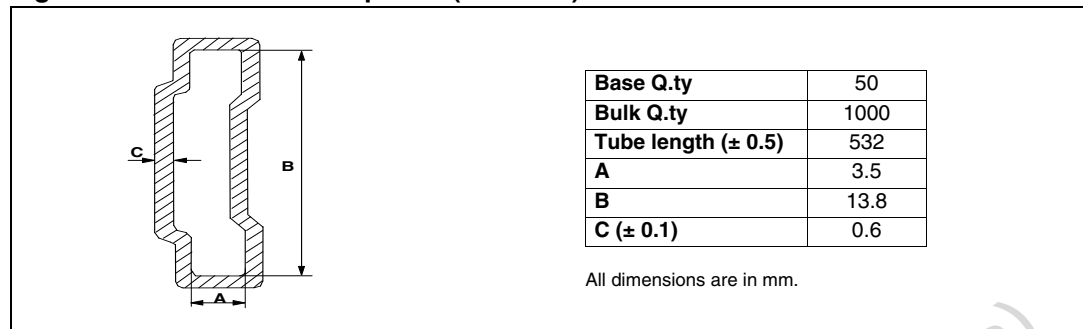
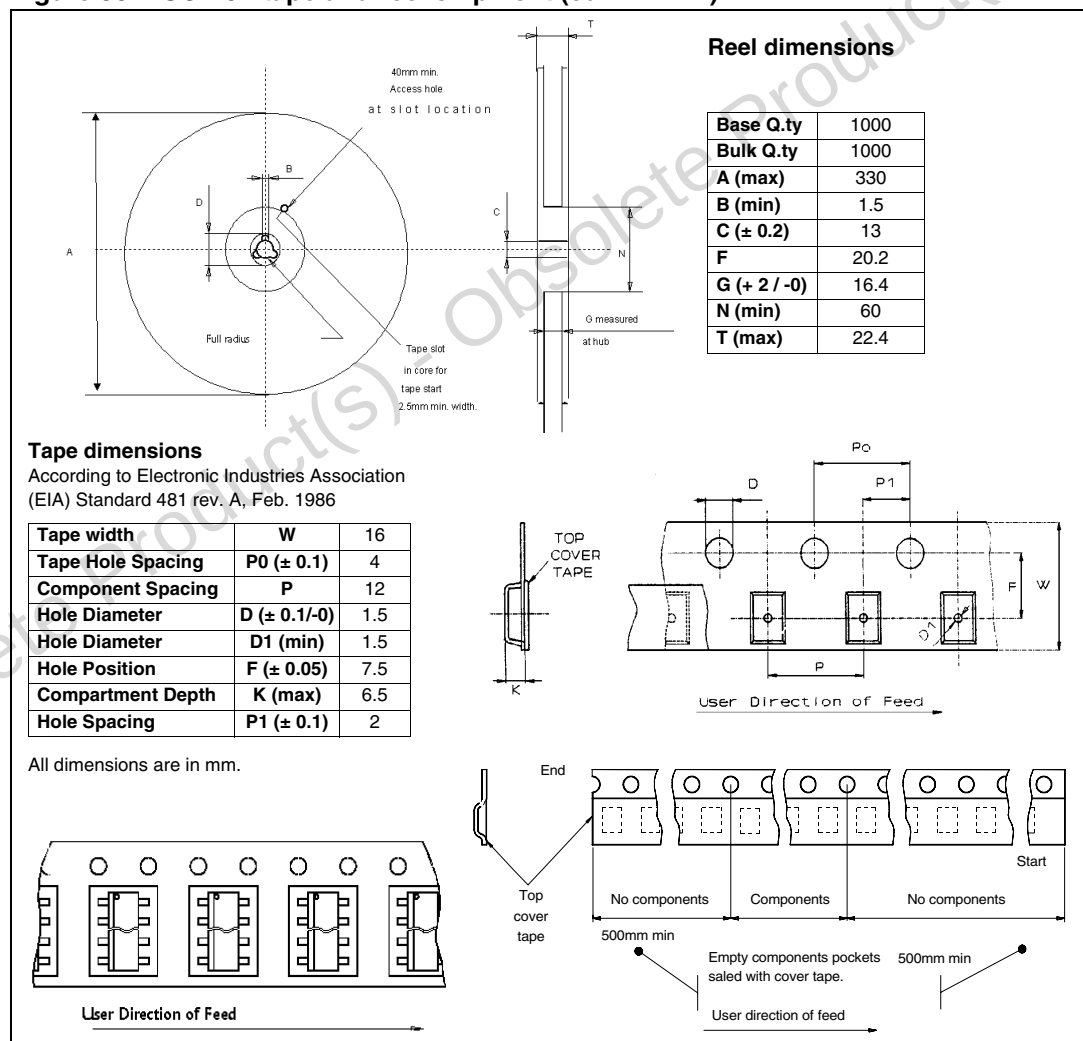


Figure 36. SO-16L tape and reel shipment (suffix "TR")



5.4 P²PAK packing information

Figure 37. P²PAK tube shipment (no suffix)

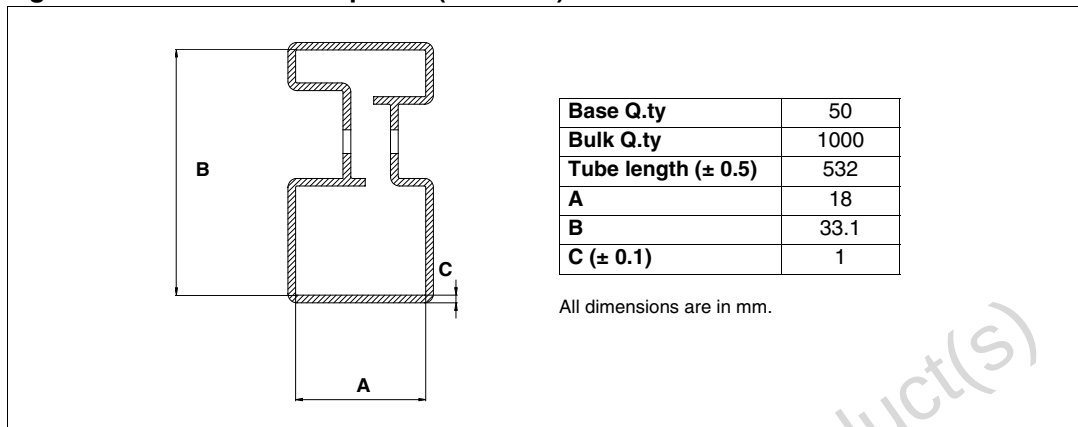
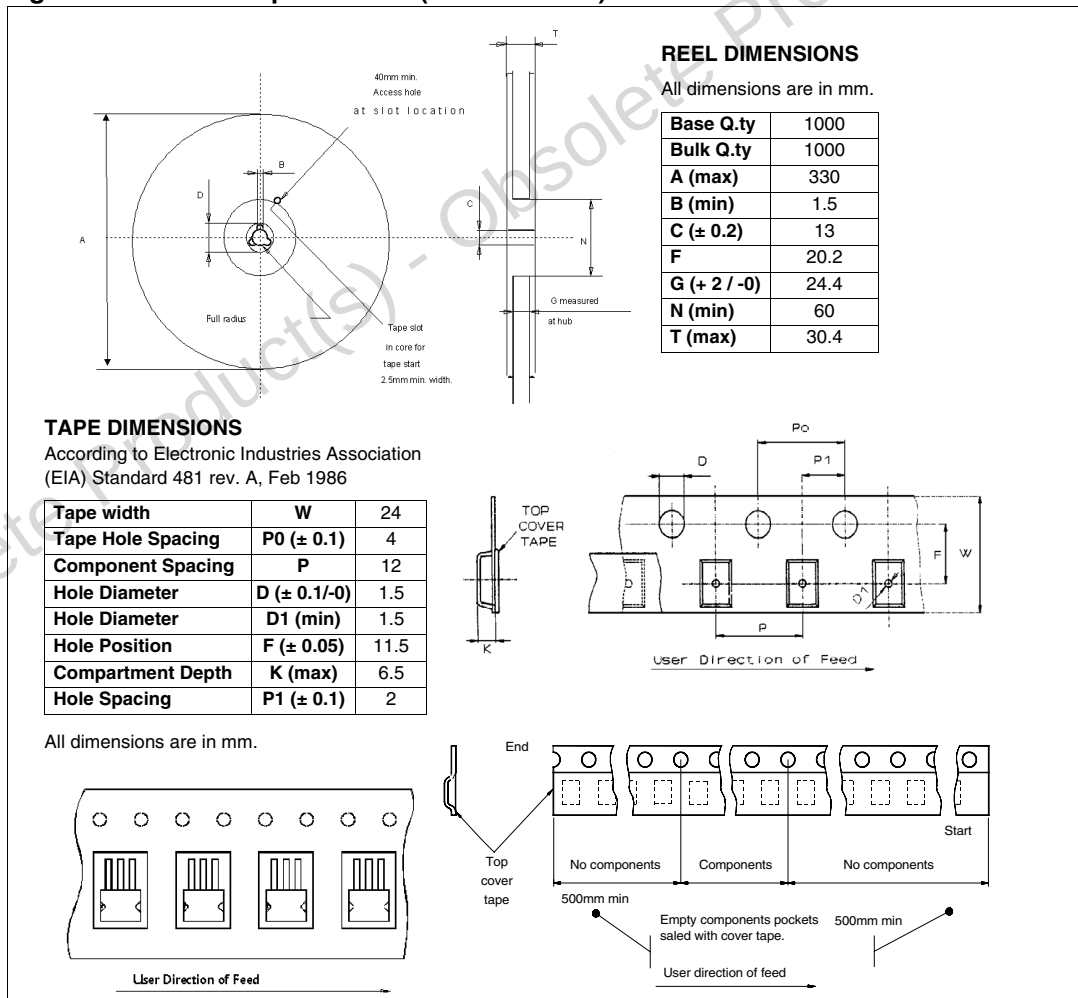


Figure 38. P²PAK tape and reel (suffix "13TR")



6 Revision history

Table 18. Document revision history

Date	Revision	Changes
09-Sep-2004	1	Initial release.
03-May-2006	2	Suggested connections for unused and n.c.pins correction (page 2).
19-Dec-2008	3	Document reformatted and restructured. Added content, list of figures and tables. Added <i>ECOPACK® packages</i> information. Updated <i>Figure 38.: P²PAK tape and reel (suffix "13TR")</i> : changed component spacing (P) in tape dimensions table from 16 mm to 12 mm.
24-Sep-2013	4	Updated Disclaimer.

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