



VN750SM

HIGH SIDE DRIVER

TYPE	$R_{DS(on)}$	I_{OUT}	V_{CC}
VN750SM	55 m Ω	6 A	36 V

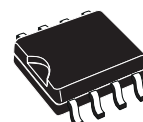
- CMOS COMPATIBLE INPUT
- ON STATE OPEN LOAD DETECTION
- OFF STATE OPEN LOAD DETECTION
- SHORTED LOAD PROTECTION
- UNDERVOLTAGE AND OVERVOLTAGE SHUTDOWN
- PROTECTION AGAINST LOSS OF GROUND
- VERY LOW STAND-BY CURRENT
- REVERSE BATTERY PROTECTION (*)

DESCRIPTION

The VN750SM is a monolithic device designed in STMicroelectronics VIPower M0-3 Technology, intended for driving any kind of load with one side connected to ground.

Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table). Active current limitation combined with thermal shutdown and automatic restart protect the device against overload.

The device detects open load condition both in on and off state. The openload threshold is aimed at



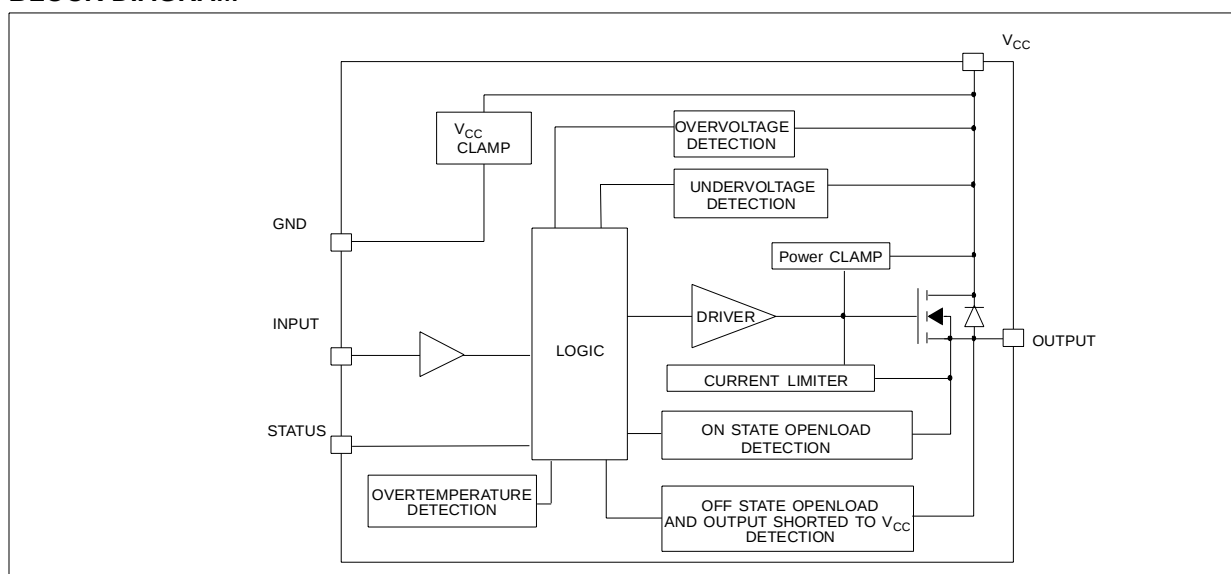
SO-8

ORDER CODES

PACKAGE	TUBE	T&R
SO-8	VN750SM	VN750SM13TR

detecting the 5W/12V standard bulb as an openload fault in the on state. Output shorted to V_{CC} is detected in the off state. Device automatically turns off in case of ground pin disconnection.

BLOCK DIAGRAM

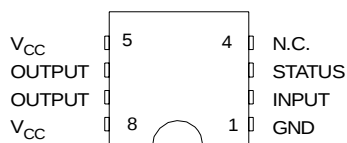


(*) See application schematic at page 8

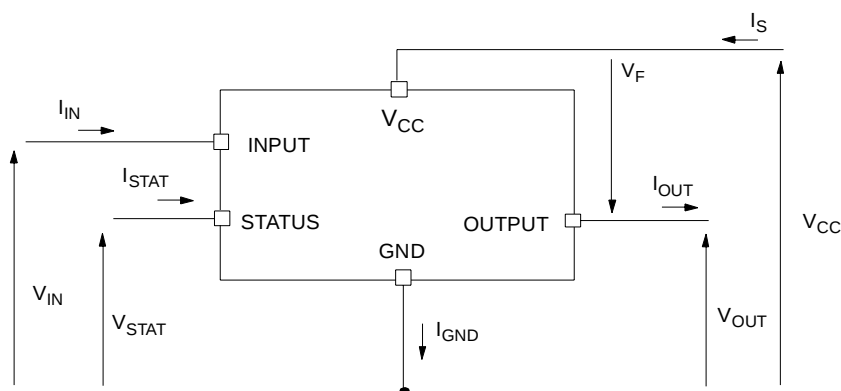
Rev. 1

VN750SM**ABSOLUTE MAXIMUM RATING**

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	41	V
$-V_{CC}$	Reverse DC Supply Voltage	- 0.3	V
$-I_{gnd}$	DC Reverse Ground Pin Current	- 200	mA
I_{OUT}	DC Output Current	Internally Limited	A
$-I_{OUT}$	Reverse DC Output Current	- 6	A
I_{IN}	DC Input Current	+/- 10	mA
I_{STAT}	DC Status Current	+/- 10	mA
V_{ESD}	Electrostatic Discharge (Human Body Model: $R=1.5K\Omega$; $C=100pF$)		
	- INPUT	4000	V
	- STATUS	4000	V
	- OUTPUT	5000	V
	- V_{CC}	5000	V
E_{MAX}	Maximum Switching Energy ($L=1.3mH$; $R_L=0\Omega$; $V_{bat}=13.5V$; $T_{jstart}=150^\circ C$; $I_L=10A$)	90	mJ
P_{tot}	Power Dissipation $T_C=25^\circ C$	4.2	W
T_j	Junction Operating Temperature	Internally Limited	$^\circ C$
T_{stg}	Storage Temperature	- 55 to 150	$^\circ C$

CONFIGURATION DIAGRAM (TOP VIEW) & SUGGESTED CONNECTIONS FOR UNUSED AND N.C. PINS

Connection / Pin	Status	N.C.	Output	Input
Floating	X	X	X	X
To Ground		X		Through 10K Ω resistor

CURRENT AND VOLTAGE CONVENTIONS

VN750SM

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{thj-lead}$	Thermal Resistance Junction-lead	30	°C/W
$R_{thj-amb}$	Thermal Resistance Junction-ambient	93 ⁽¹⁾ 82 ⁽²⁾	°C/W

⁽¹⁾ When mounted on a standard single-sided FR-4 board with 0.5 cm² of Cu (at least 35μm thick) connected to all V_{CC} pins. Horizontal mounting and no artificial air flow.

⁽²⁾ When mounted on a standard single-sided FR-4 board with 2 cm² of Cu (at least 35μm thick) connected to all V_{CC} pins. Horizontal mounting and no artificial air flow.

ELECTRICAL CHARACTERISTICS (8V<V_{CC}<36V; -40°C<T_j<150°C unless otherwise specified)

POWER

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V _{CC}	Operating Supply Voltage		5.5	13	36	V
V _{USD}	Undervoltage Shut-down		3	4	5.5	V
V _{USDhyst}	Undervoltage Shut-down Hysteresis			0.5		V
V _{OV}	Overvoltage Shut-down		36			V
R _{ON}	On State Resistance	I _{OUT} =2A; T _j =25°C; V _{CC} >8V I _{OUT} =2A; V _{CC} >8V			55 110	mΩ mΩ
I _S	Supply Current	Off State; V _{CC} =13V; V _{IN} =V _{OUT} =0V Off State; V _{CC} =13V; V _{IN} =V _{OUT} =0V; T _j =25°C On State; V _{CC} =13V; V _{IN} =5V; I _{OUT} =0A		10 10 2	25 20 3.5	μA μA mA
I _{L(off1)}	Off State Output Current	V _{IN} =V _{OUT} =0V	0		50	μA
I _{L(off2)}	Off State Output Current	V _{IN} =0V; V _{OUT} =3.5V	-75		0	μA
I _{L(off3)}	Off State Output Current	V _{IN} =V _{OUT} =0V; V _{CC} =13V; T _j =125°C			5	μA
I _{L(off4)}	Off State Output Current	V _{IN} =V _{OUT} =0V; V _{CC} =13V; T _j =25°C			3	μA

SWITCHING (V_{CC}=13V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t _{d(on)}	Turn-on Delay Time	R _L =6.5Ω from V _{IN} rising edge to V _{OUT} =1.3V		40		μs
t _{d(off)}	Turn-off Delay Time	R _L =6.5Ω from V _{IN} falling edge to V _{OUT} =11.7V		30		μs
dV _{OUT} /dt _(on)	Turn-on Voltage Slope	R _L =6.5Ω from V _{OUT} =1.3V to V _{OUT} =10.4V		See relative diagram		V/μs
dV _{OUT} /dt _(off)	Turn-off Voltage Slope	R _L =6.5Ω from V _{OUT} =11.7V to V _{OUT} =1.3V		See relative diagram		V/μs

INPUT PIN

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V _{IL}	Input Low Level				1.25	V
I _{IL}	Low Level Input Current	V _{IN} =1.25V	1			μA
V _{IH}	Input High Level		3.25			V
I _{IH}	High Level Input Current	V _{IN} =3.25V			10	μA
V _{I(hyst)}	Input Hysteresis Voltage		0.5			V
V _{ICL}	Input Clamp Voltage	I _{IN} =1mA I _{IN} =-1mA	6	6.8 -0.7	8	V V



VN750SM**ELECTRICAL CHARACTERISTICS** (continued)**VCC - OUTPUT DIODE**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_F	Forward on Voltage	$-I_{OUT}=1.4A$; $T_J=150^{\circ}C$			0.6	V

STATUS PIN

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{STAT}	Status Low Output Voltage	$I_{STAT}=1.6mA$			0.5	V
I_{LSTAT}	Status Leakage Current	Normal Operation; $V_{STAT}=5V$			10	μA
C_{STAT}	Status Pin Input Capacitance	Normal Operation; $V_{STAT}=5V$			100	pF
V_{SCL}	Status Clamp Voltage	$I_{STAT}=1mA$	6	6.8	8	V
		$I_{STAT}=-1mA$		-0.7		V

PROTECTIONS (see note 1)

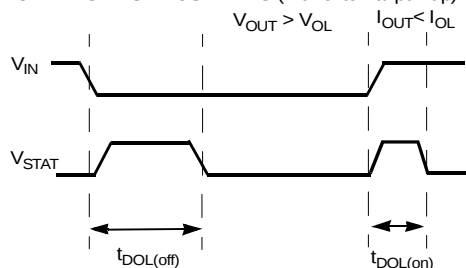
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
T_{TSD}	Shut-down Temperature		150	175	200	$^{\circ}C$
T_R	Reset Temperature		135			$^{\circ}C$
T_{hyst}	Thermal Hysteresis		7	15		$^{\circ}C$
t_{SDL}	Status delay in overload condition	$T_J > T_{TSD}$			20	μs
I_{lim}	Current limitation	$5.5V < V_{CC} < 36V$	6	10	12	A
					12	A
V_{demag}	Turn-off Output Clamp Voltage	$I_{OUT}=2A$; $V_{IN}=0V$; $L=6mH$	$V_{CC}-41$	$V_{CC}-48$	$V_{CC}-55$	V

Note 1: To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles

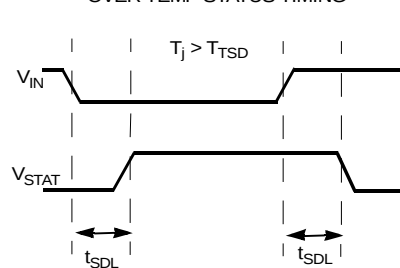
OPENLOAD DETECTION

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{OL}	Openload ON State Detection Threshold	$V_{IN}=5V$	0.6	0.9	1.2	A
$t_{DOL(on)}$	Openload ON State Detection Delay	$I_{OUT}=0A$			200	μs
V_{OL}	Openload OFF State Voltage Detection Threshold	$V_{IN}=0V$	1.5	2.5	3.5	V
$t_{DOL(off)}$	Openload Detection Delay at Turn Off				1000	μs

OPEN LOAD STATUS TIMING (with external pull-up)

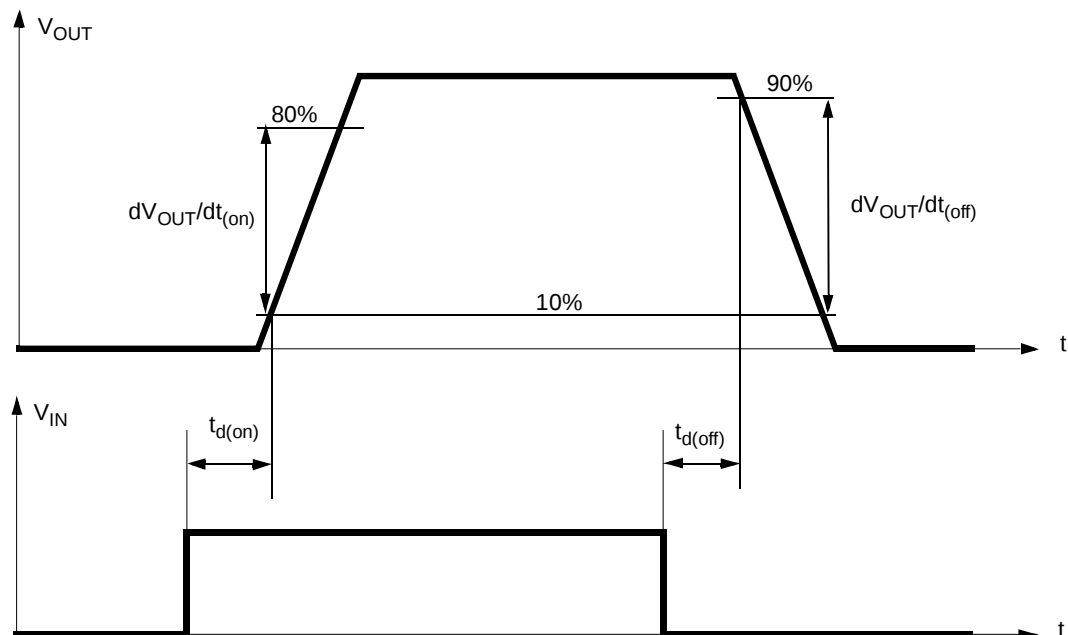


OVER TEMP STATUS TIMING



VN750SM

Switching time Waveforms



TRUTH TABLE

CONDITIONS	INPUT	OUTPUT	STATUS
Normal Operation	L	L	H
	H	H	H
Current Limitation	L	L	H
	H	X	$(T_J < T_{TSD})$ H
	H	X	$(T_J > T_{TSD})$ L
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Overvoltage	L	L	H
	H	L	H
Output Voltage > V_{OL}	L	H	L
	H	H	H
Output Current < I_{OL}	L	L	H
	H	H	L

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ELECTRICAL TRANSIENT REQUIREMENTS ON V_{CC} PIN

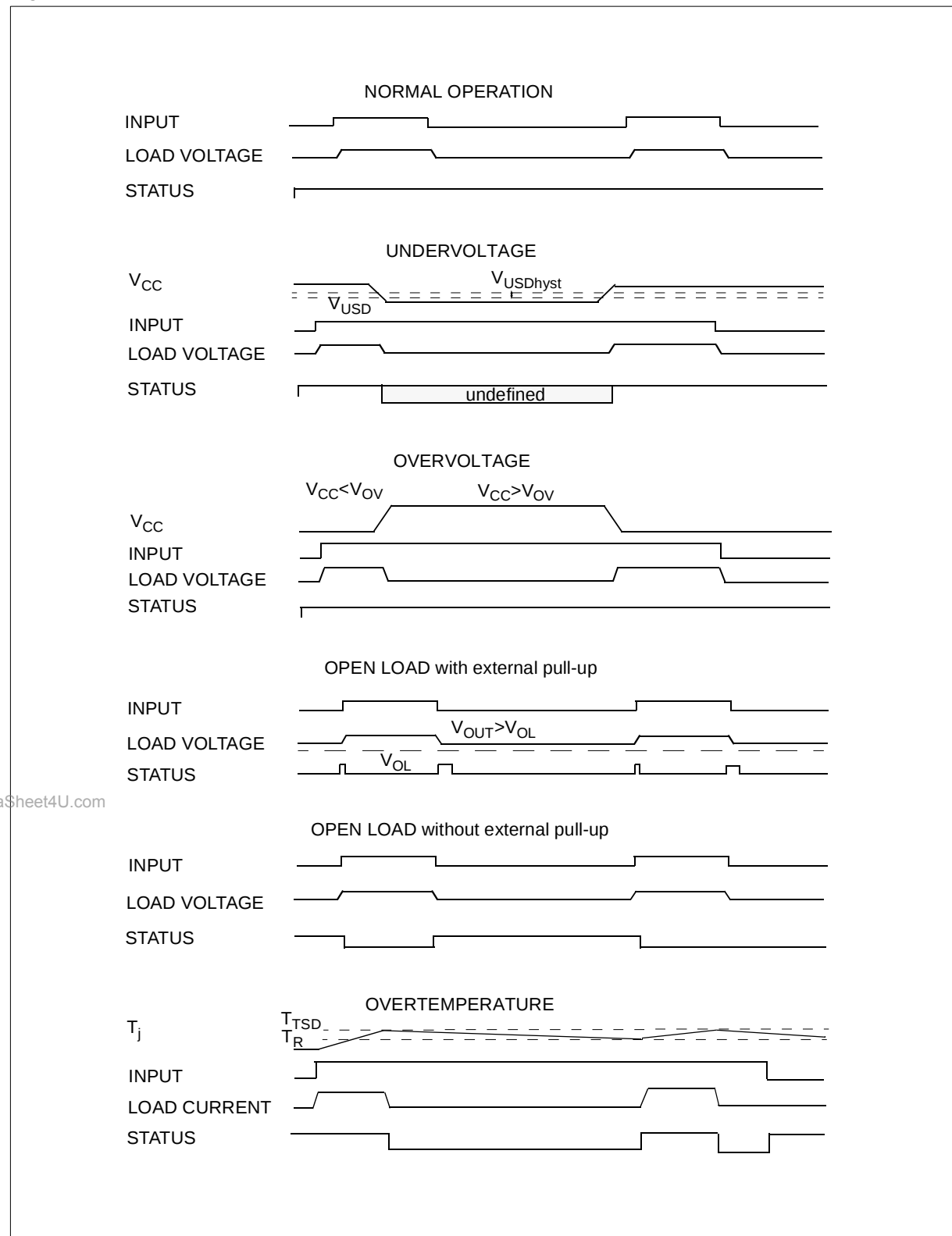
ISO T/R 7637/1 Test Pulse	TEST LEVELS				
	I	II	III	IV	Delays and Impedance
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 μ s 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 μ s 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

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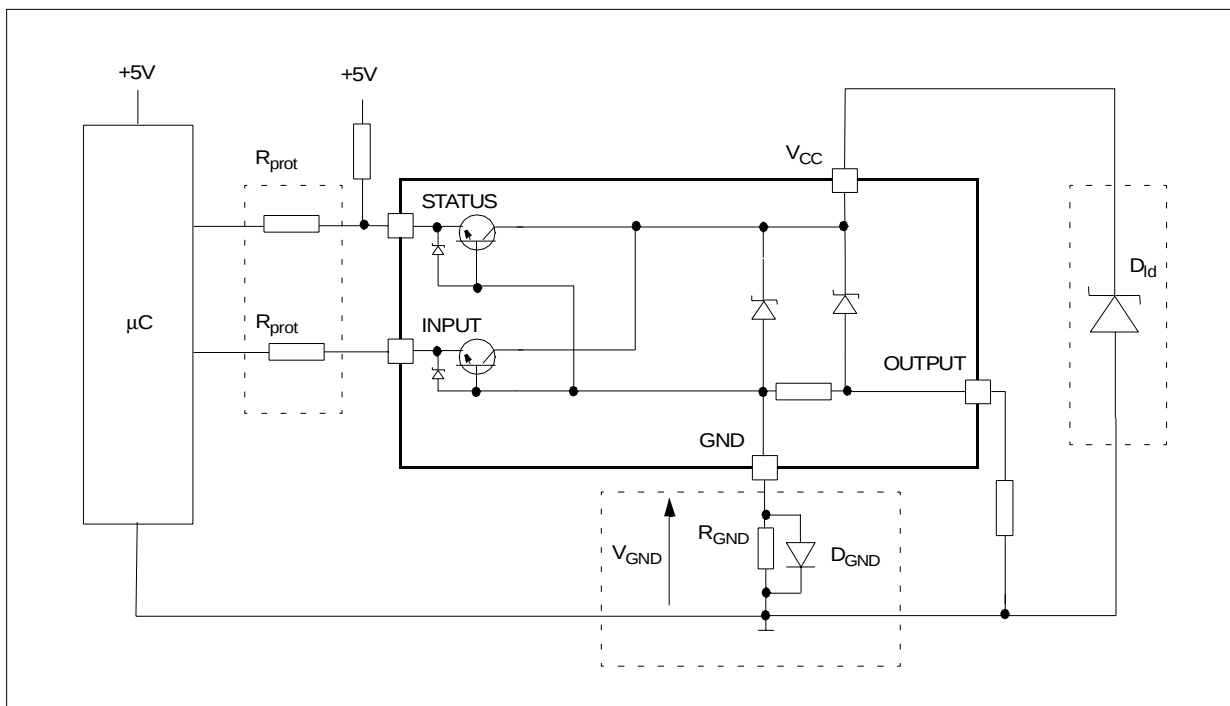
Figure 1: Waveforms



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APPLICATION SCHEMATIC



GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

- 1) $R_{GND} \leq 600\text{mV} / (I_{S(on)max})$.
- 2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where I_{GND} is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND} .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

Solution 2: A diode (D_{GND}) in the ground line.

A resistor ($R_{GND}=1\text{k}\Omega$) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift ($\approx 600\text{mV}$) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating.

Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

LOAD DUMP PROTECTION

D_{id} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds V_{CC} max DC rating. The same applies if the device will be subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

 μC I/Os PROTECTION:

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the μC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of μC I/Os.

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For $V_{CCpeak} = -100\text{V}$ and $I_{latchup} \geq 20\text{mA}$; $V_{OH\mu C} \geq 4.5\text{V}$
 $5\text{k}\Omega \leq R_{prot} \leq 65\text{k}\Omega$.

Recommended R_{prot} value is $10\text{k}\Omega$.

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OPEN LOAD DETECTION IN OFF STATE

Off state open load detection requires an external pull-up resistor (R_{PU}) connected between OUTPUT pin and a positive supply voltage (V_{PU}) like the +5V line used to supply the microprocessor.

The external resistor has to be selected according to the following requirements:

- 1) no false open load indication when load is connected: in this case we have to avoid V_{OUT} to be higher than V_{OLmin} ; this results in the following condition

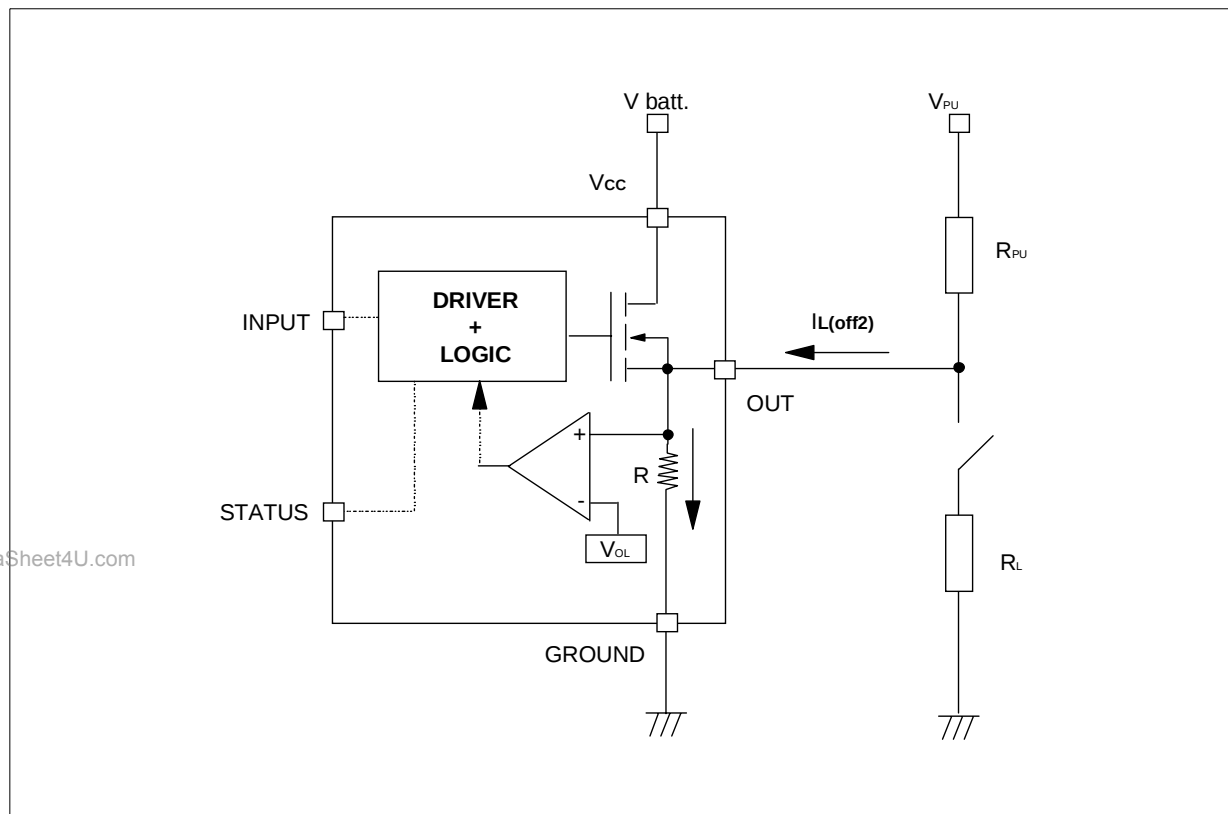
$$V_{OUT} = (V_{PU} / (R_L + R_{PU})) R_L < V_{OLmin}.$$

- 2) no misdetection when load is disconnected: in this case the V_{OUT} has to be higher than V_{OLmax} ; this results in the following condition $R_{PU} < (V_{PU} - V_{OLmax}) / I_{L(off2)}$.

Because $I_{S(OFF)}$ may significantly increase if V_{OUT} is pulled high (up to several mA), the pull-up resistor R_{PU} should be connected to a supply that is switched OFF when the module is in standby.

The values of V_{OLmin} , V_{OLmax} and $I_{L(off2)}$ are available in the Electrical Characteristics section.

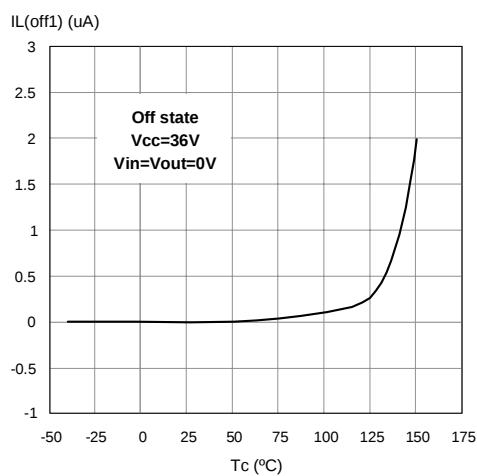
Open Load detection in off state



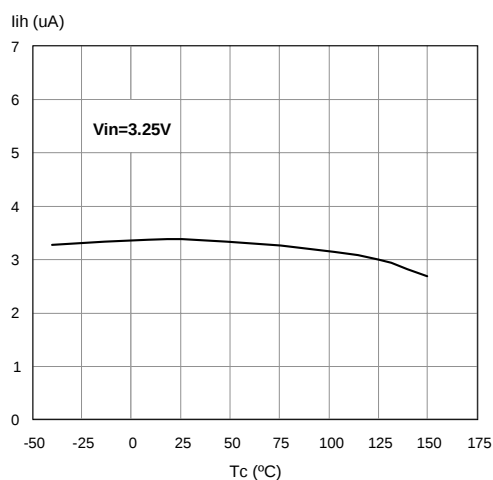
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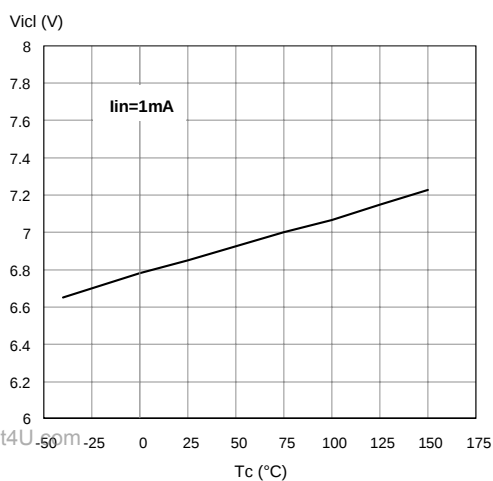
Off State Output Current



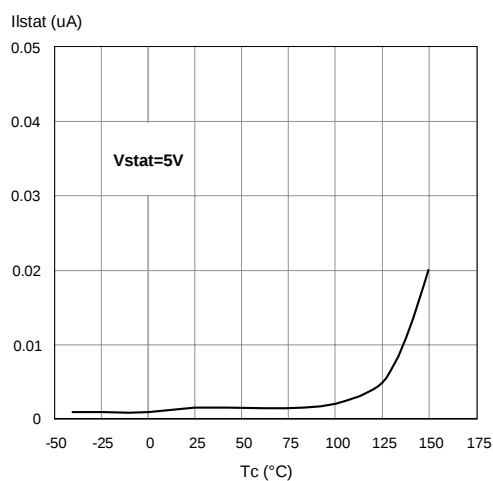
High Level Input Current



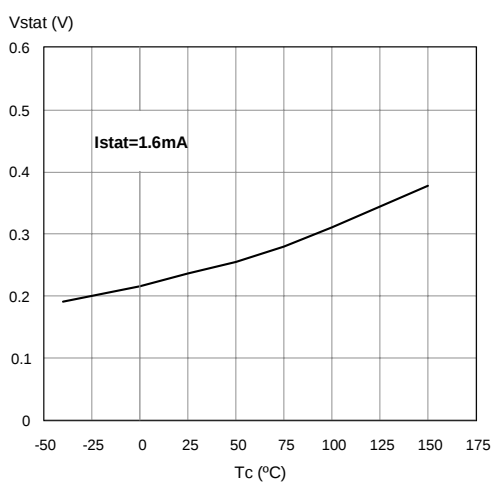
Input Clamp Voltage



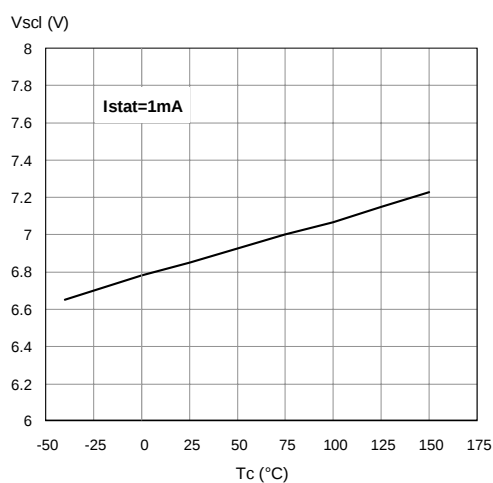
Status Leakage Current



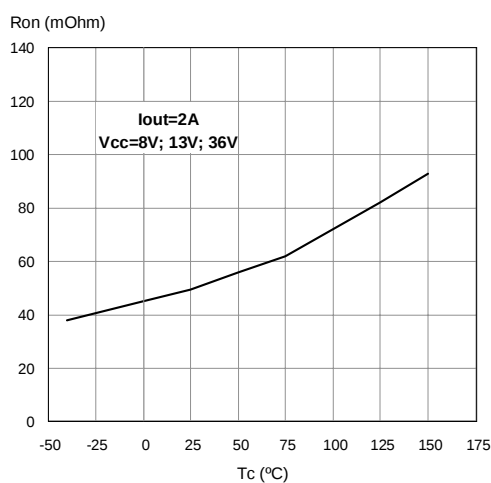
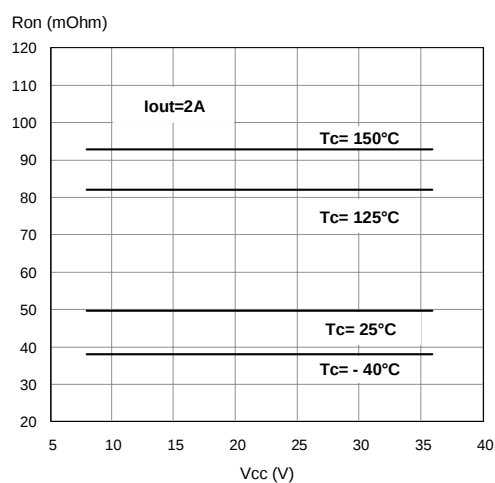
Status Low Output Voltage



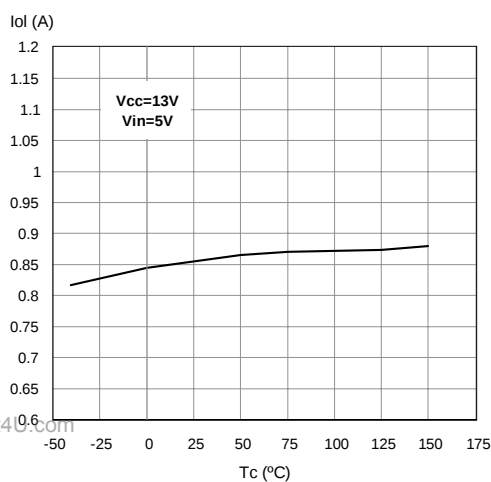
Status Clamp Voltage



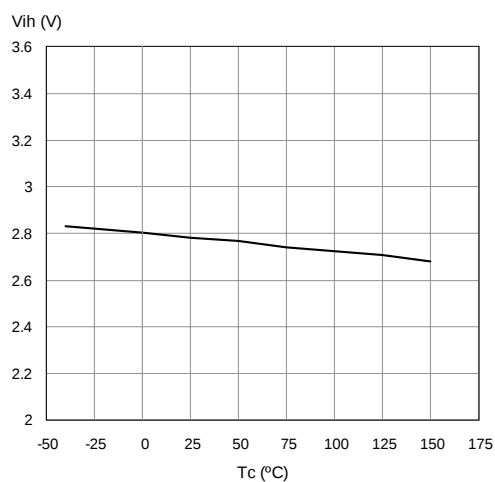
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On State Resistance Vs. T_{case} On State Resistance Vs. V_{CC} 

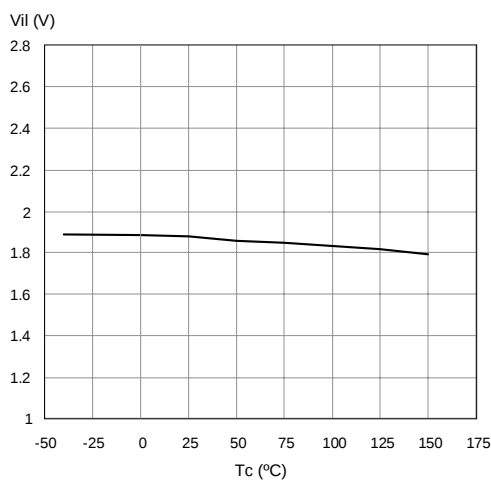
Openload On State Detection Threshold



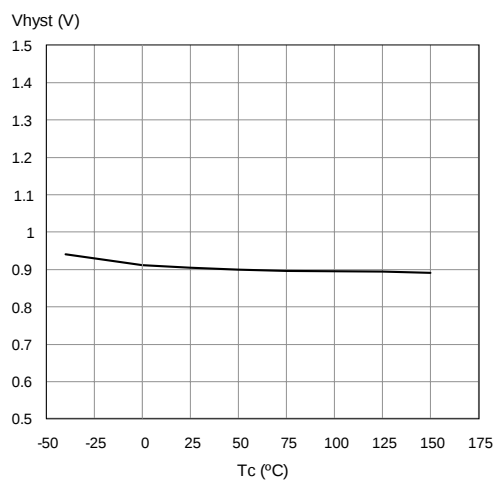
Input High Level



Input Low Level

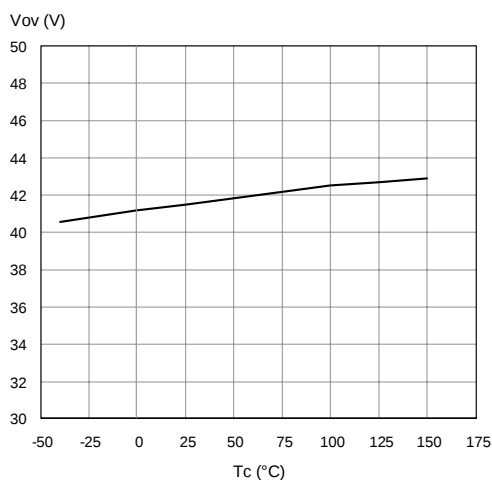


Input Hysteresis Voltage

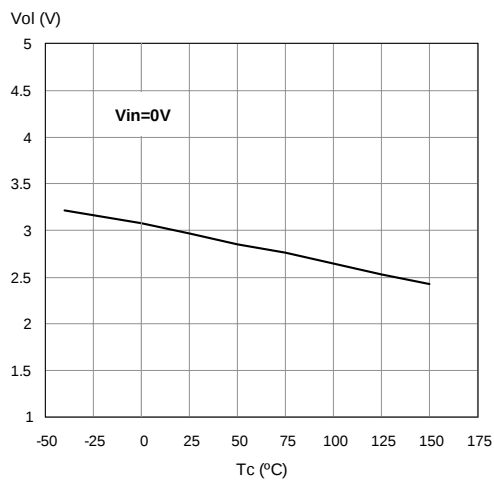


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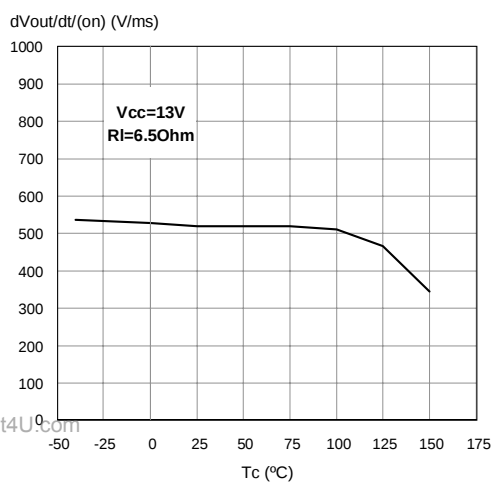
Overvoltage Shutdown



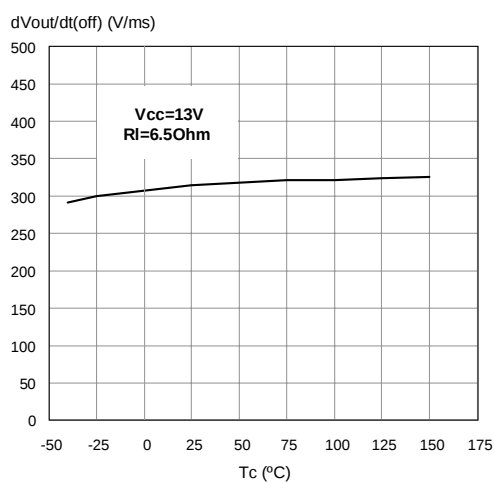
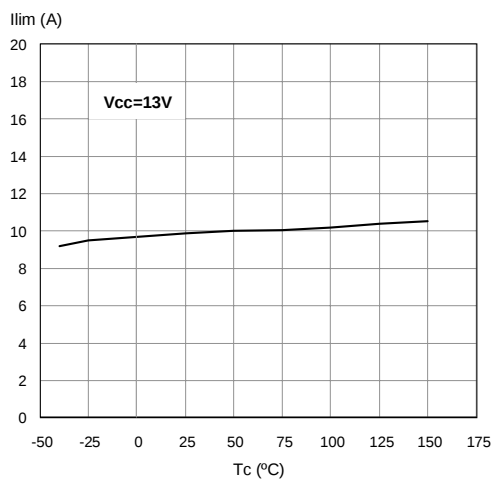
Openload Off State Voltage Detection Threshold



Turn-on Voltage Slope

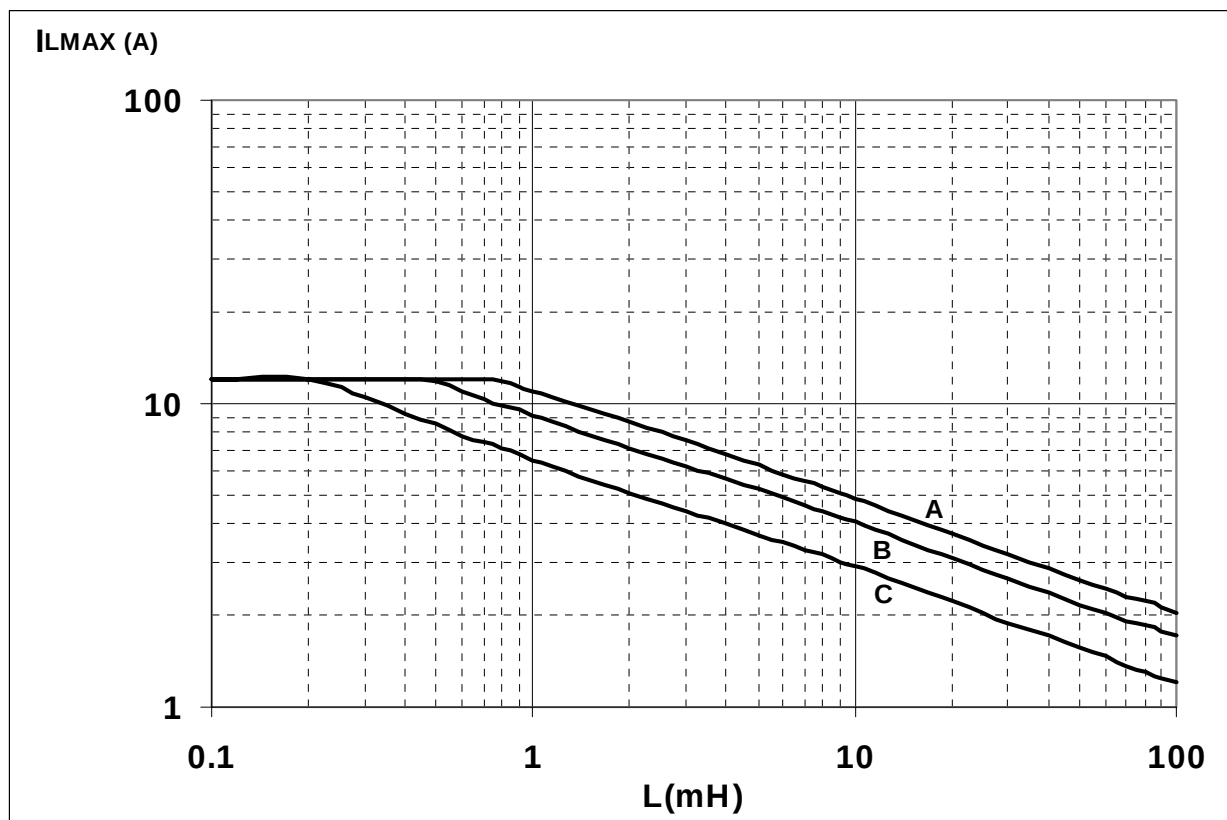


Turn-off Voltage Slope

 I_{lim} Vs. T_{case} 

VN750SM

Maximum turn off current versus load inductance



A = Single Pulse at $T_{jstart}=150^{\circ}\text{C}$

B= Repetitive pulse at $T_{jstart}=100^{\circ}\text{C}$

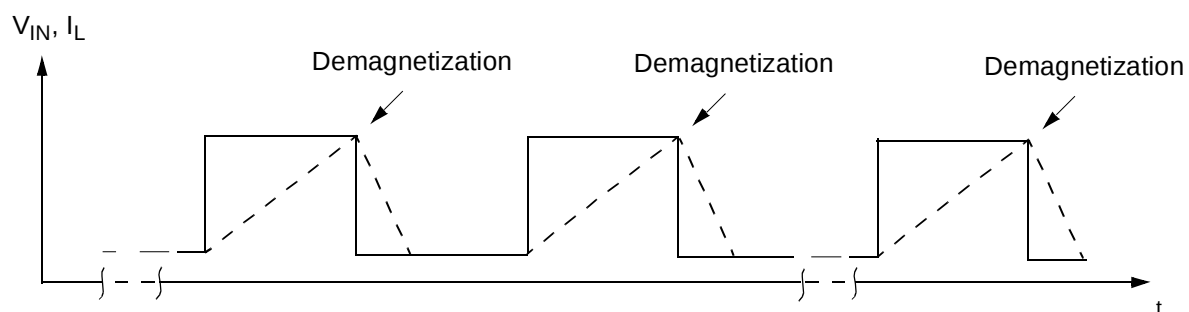
C= Repetitive Pulse at $T_{jstart}=125^{\circ}\text{C}$

www.DataSheet4U.com Conditions:

$V_{CC}=13.5\text{V}$

Values are generated with $R_L=0\Omega$

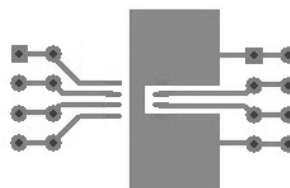
In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.



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SO-8 THERMAL DATA

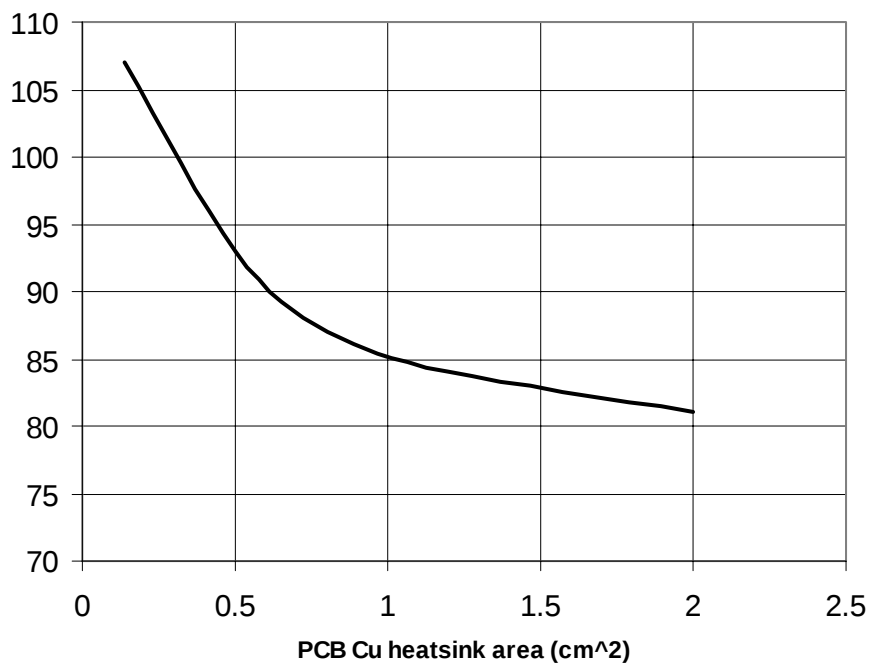
SO-8 PC Board

0.14cm²2cm²

Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 58mm x 58mm, PCB thickness=2mm, Cu thickness=35μm, Copper areas: 0.14cm², 2cm²).

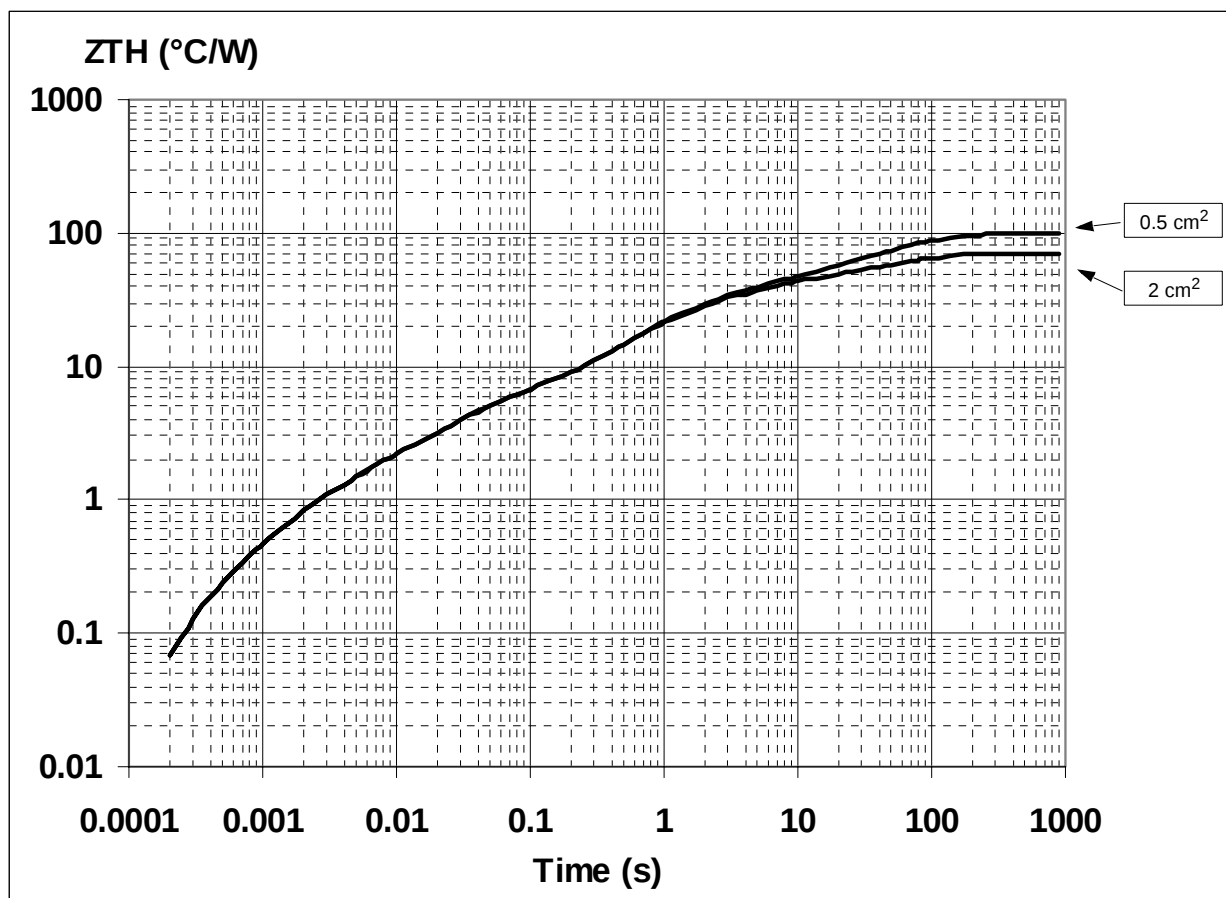
 $R_{thj-amb}$ Vs PCB copper area in open box free air condition $R_{thj-amb}$ (°C/W)

SO8 at 2 pins connected to TAB



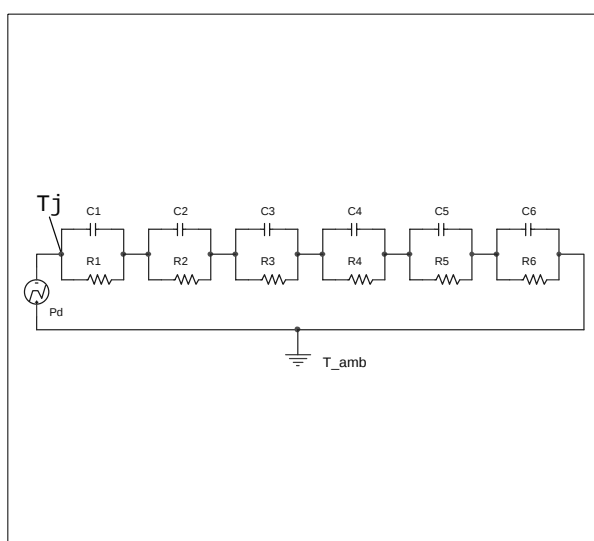
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SO-8 Thermal Impedance Junction Ambient Single Pulse



Thermal fitting model of a single channel HSD in SO-8

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Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

$$\text{where } \delta = t_p / T$$

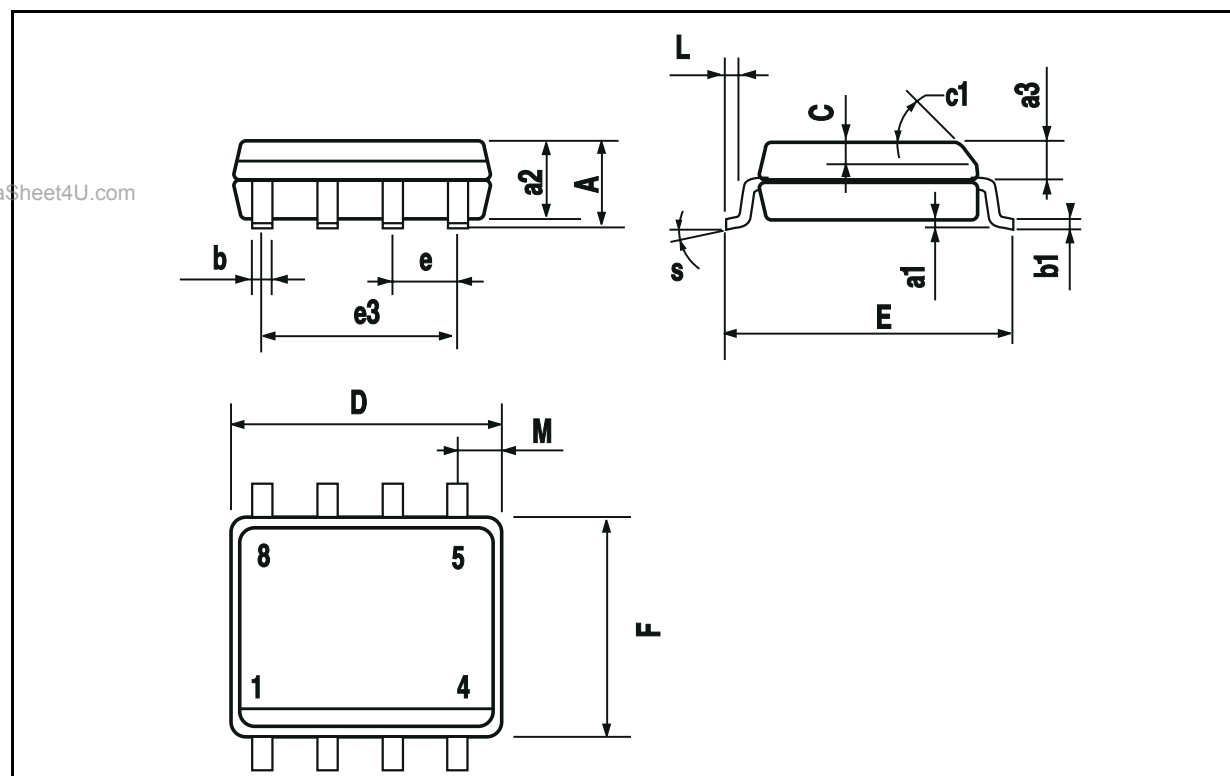
Thermal Parameter

Area/island (cm ²)	0.5	2
R1 (°C/W)	0.05	
R2 (°C/W)	0.8	
R3 (°C/W)	3.5	
R4 (°C/W)	21	
R5 (°C/W)	16	
R6 (°C/W)	58	28
C1 (W.s/°C)	0.006	
C2 (W.s/°C)	2.60E-03	
C3 (W.s/°C)	0.0075	
C4 (W.s/°C)	0.045	
C5 (W.s/°C)	0.35	
C6 (W.s/°C)	1.05	2

VN750SM

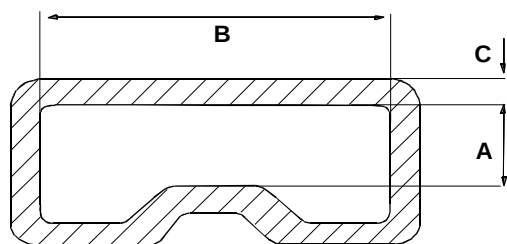
SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					
L1	0.8		1.2	0.031		0.047



VN750SM

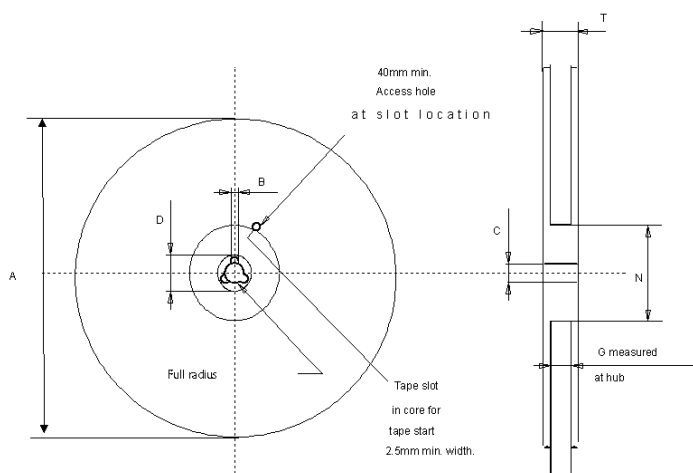
SO-8 TUBE SHIPMENT (no suffix)



Base Q.ty	100
Bulk Q.ty	2000
Tube length (± 0.5)	532
A	3.2
B	6
C (± 0.1)	0.6

All dimensions are in mm.

TAPE AND REEL SHIPMENT (suffix "13TR")



REEL DIMENSIONS

Base Q.ty	2500
Bulk Q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

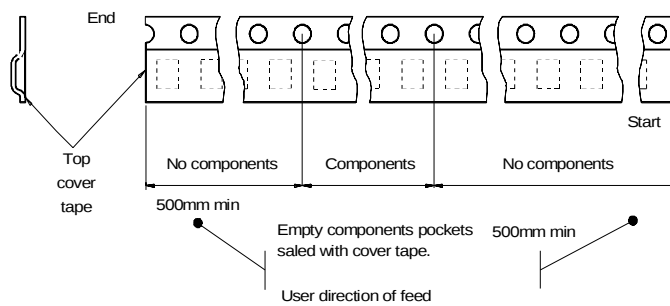
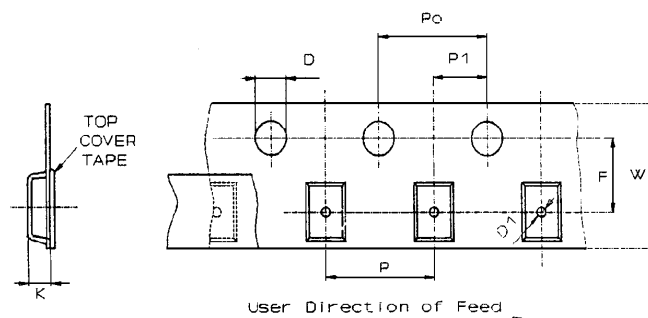
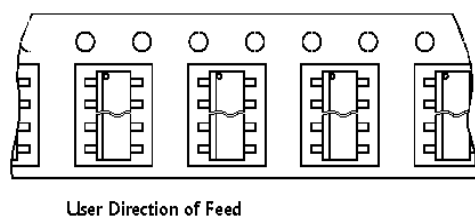
All dimensions are in mm.

TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	W	12
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	8
Hole Diameter	D ($\pm 0.1/-0$)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	5.5
Compartment Depth	K (max)	4.5
Hole Spacing	P1 (± 0.1)	2

All dimensions are in mm.



VN750SM

REVISION HISTORY

Date	Revision	Description of Changes
Jul 2004	1	- Minor changes - Current and voltage convention update (page 2). - "Configuration diagram (top view) & suggested connections for unused and n.c. pins" insertion (page 2). - 2cm² Cu condition insertion in Thermal Data table (page 3). - V_{CC} - OUTPUT DIODE section update (page 4). - Revision History table insertion (page18). - Disclaimers update (page 19).

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