Supertex inc.

Preliminary

N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			DIE	WAFER
60V	0.3Ω	10A	VN2206ND	VN2206NW
100V	0.3Ω	10A	VN2210ND	VN2210NW

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

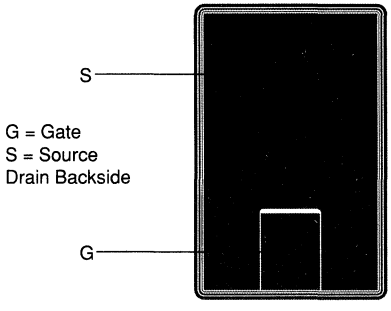
Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Specifications

- ☐ Die Size: 70 X 105 Mil
- ☐ Die Thickness: 11 ± 1.5 Mil
- ☐ Bonding Pad Size: Gate = 20 X 27 Mil
  Source = 20 X 27 Mil
- ☐ Recommended Bonding Wire Size: 8 Mil
- ☐ Backside Metal: Au (CrAg optional)

Die Geometry



Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	±20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics (@ θ_{jc} = 1.25°C/W)

I_D (continuous)*	I_D (pulsed)*	I_{DR}	I_{DRM}*
8A	15A	8A	15A

*I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN2206	60			V	V_{GS} = 0, I_D = 10mA
		VN2210	100				
$V_{GS(th)}$	Gate Threshold Voltage		0.8		2.4	V	V_{GS} = V_{DS}, I_D = 10mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.3	-5.5	mV/°C	V_{GS} = V_{DS}, I_D = 10mA
I_{GSS}	Gate Body Leakage			1	100	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				50	µA	V_{GS} = 0, V_{DS} = Max Rating
					10	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		3	5		A	V_{GS} = 5V, V_{DS} = 25V
			8				V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			0.22	0.45	Ω	V_{GS} = 5V, I_D = 1A
				0.2	0.3		V_{GS} = 10V, I_D = 4A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.85	1.2	%/°C	V_{GS} = 10V, I_D = 10A
G_{FS}	Forward Transconductance		2.0	3.0		℧	V_{DS} = 25V, I_D = 2A
C_{ISS}	Input Capacitance				500	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance				300		
C_{RSS}	Reverse Transfer Capacitance				125		
$t_{d(ON)}$	Turn-ON Delay Time			8	15	ns	V_{DD} = 25V, I_D = 5A, R_S = 50Ω
t_r	Rise Time			8	15		
$t_{d(OFF)}$	Turn-OFF Delay Time			70	90		
t_f	Fall Time			40	60		
V_{SD}	Diode Forward Voltage Drop			1.2	1.4	V	V_{GS} = 0, I_{SD} = 4A
t_{rr}	Reverse Recovery Time			500		ns	V_{GS} = 0, I_{SD} = 1A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit