

Preliminary



N-Channel Enhancement-Mode **Vertical DMOS Power FETs**

Ordering Information

BV _{DSS} /	R _{DS(ON)}	V _{GS(th)}	Order Number / Package TO-92		
BV _{DGS}	(max)	(max)			
200V	10Ω	1.5V	VN2010L		

Features

- ☐ Freedom from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-Channel devices

Applications

- Motor control
- Converters
- ☐ Amplifiers
- □ Switches □ Power supply circuits
- Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)
- Telecom Switching

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV _{DGS}
Gate-to-Source Voltage	± 40V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

^{*}Distance of 1.6 mm from case for 10 seconds.

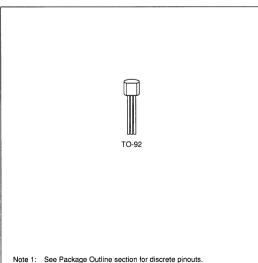
Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicongate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermallyinduced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options

(Note 1)



Thermal Characteristics

Package	I _D (continuous)*	I _D (pulsed)*	Power Dissipation @ T _C = 25°C	θ _{ja} ∘C/W	θ _{jc} ∘C/W	I _{DR}	I _{DRM} *	
TO-92	250mA	1.0A	1W .	125	170	250mA	1.0A	

^{*}I_D (continuous) is limited by max rated T_i.

Electrical Characteristics (@ 25°C unless otherwise specified)

(Notes 1 and 2)

Symbol	Parameter	Min	Тур	Max	Unit	Conditions	
BV _{DSS}	Drain-to-Source Breakdown Voltage	200			V	$V_{GS} = 0, I_{D} = 100 \mu A$	
V _{GS(th)}	Gate Threshold Voltage	0.6		1.5	V	$V_{GS} = V_{DS}, I_D = 1mA$	
I _{GSS}	Gate Body Leakage			10	nA	$V_{GS} = \pm 20V, V_{DS} = 0$	
I _{DSS}	Zero Gate Voltage Drain Current			10		V _{GS} = 0, V _{DS} = Max Rating	
				100	μΑ	$V_{GS} = 0$, $V_{DS} = 0.8$ Max Rating	
						T _A = 125°C	
V _{DS(ON)}	Static Drain-Source ON-State Voltage			0.5	V	$V_{GS} = 4.5V, I_{D} = 50mA$	
				1	V	V _{GS} = 10V, I _D = 100mA	
R _{DS(ON)}	Static Drain-to-Source			10	Ω	$V_{GS} = 4.5V, I_{D} = 50mA$	
	ON-State Resistance			10	Ω	V _{GS} = 10V, I _D = 100mA	
G _{FS}	Forward Transconductance	125			m℧	$V_{DS} = 25V, I_{D} = 100mA$	
C _{ISS}	Input Capacitance			60			
C _{oss}	Common Source Output Capacitance			30	pF	$V_{GS} = 0, V_{DS} = 25V$ f = 1 MHz	
C _{RSS}	Reverse Transfer Capacitance			15		1 = 1 1011 12	
t _{d(ON)}	Turn-ON Delay Time			10	ns	$V_{DD} = 25V, I_{D} = 100mA, R_{S} = 50\Omega$	
t _{d(OFF)}	Turn-OFF Delay Time			30	ns	$V_{DD} = 25V, I_{D} = 100mA, R_{S} = 50\Omega$	
V _{SD}	Diode Forward Voltage Drop			1.2	V	$V_{GS} = 0, I_{SD} = 250 \text{mA}$	

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

