N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package
			Die
500V	60Ω	150mA	VN1550NW

* Die in wafer form.

Features

- ❏ Free from secondary breakdown
- ❏ Low power drive requirement
- ❏ Ease of paralleling
- ❏ Low C_{ISS} and fast switching speeds
- ❏ Excellent thermal stability
- ❏ Integral Source-Drain diode
- ❏ High input impedance and high gain
- ❏ Complementary N- and P-channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ❏ Motor controls
- ❏ Converters
- ❏ Amplifiers
- ❏ Switches
- ❏ Power supply circuits
- ❏ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

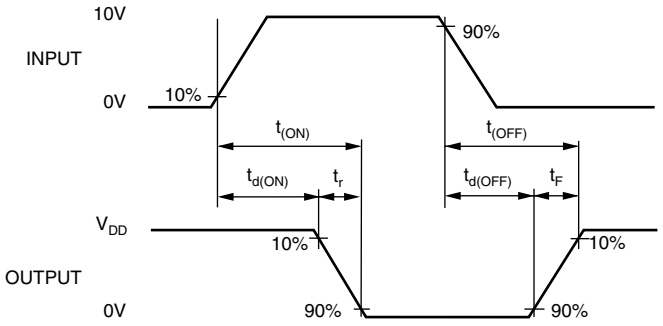
01/14/02

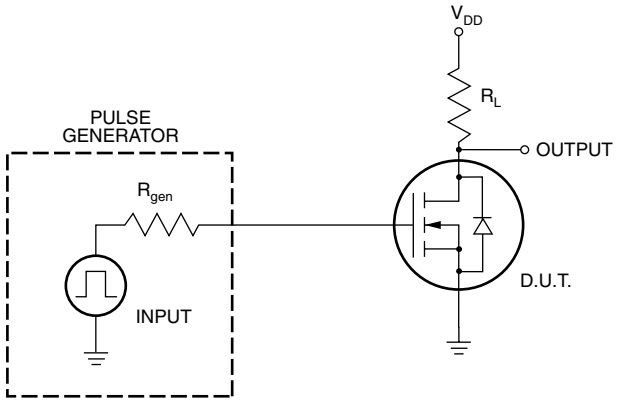
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	500			V	V_{GS} = 0V, I_D = 1mA
$V_{GS(th)}$	Gate Threshold Voltage	2		4	V	$V_{GS} = V_{DS}$, I_D = 1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature		-3.8	-5.0	mV/°C	$V_{GS} = V_{DS}$, I_D = 1mA
I_{GSS}	Gate Body Leakage			100	nA	V_{GS} = ±20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current			10	μA	V_{GS} = 0V, V_{DS} = Max Rating
				1	mA	V_{GS} = 0V, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		100		mA	V_{GS} = 5V, V_{DS} = 25V
		150	350			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		45		Ω	V_{GS} = 5V, I_D = 50mA
			40	60		V_{GS} = 10V, I_D = 50mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature		1	1.7	%/°C	V_{GS} = 10V, I_D = 50mA
G_{FS}	Forward Transconductance	50	100		m℧	V_{DS} = 25V, I_D = 50mA
C_{ISS}	Input Capacitance		45	55	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance		8	10		
C_{RSS}	Reverse Transfer Capacitance		2	5		
$t_{d(ON)}$	Turn-ON Delay Time			10	ns	V_{DD} = 25V, I_D = 150mA, R_{GEN} = 25Ω
t_r	Rise Time			15		
$t_{d(OFF)}$	Turn-OFF Delay Time			10		
t_f	Fall Time			10		
V_{SD}	Diode Forward Voltage Drop		0.8		V	V_{GS} = 0V, I_{SD} = 0.5A
t_{rr}	Reverse Recovery Time		300		ns	V_{GS} = 0V, I_{SD} = 0.5A

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





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