Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			TO-39	TO-92
40V	8Ω	0.5A	VN1304N2	VN1304N3
60V	8Ω	0.5A	VN1306N2	VN1306N3
100V	8Ω	0.5A	VN1310N2	VN1310N3

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

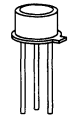
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

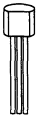
Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Note 1)



TO-39



TO-92

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
TO-39	0.4A	1.4A	3.0W	125	41.5	0.4A	1.4A
TO-92	0.25A	1.3A	1.0W	170	125	0.25A	1.3A

*I_D (continuous) is limited by max rated T_j.

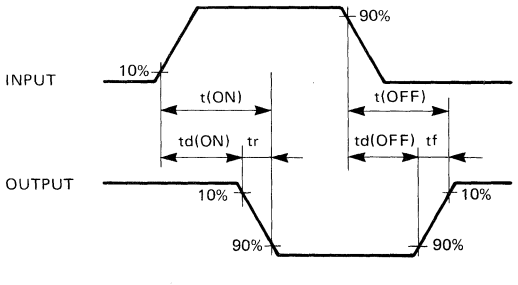
Electrical Characteristics (@ 25°C unless otherwise specified)

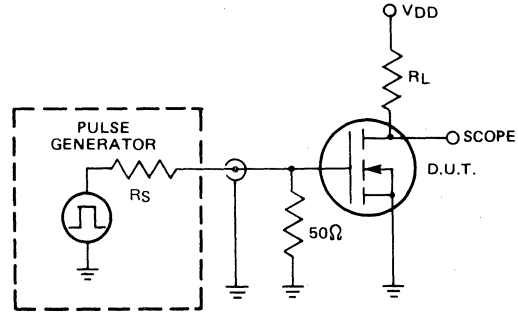
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BVDSS	Drain-to-Source Breakdown Voltage	VN1310	100			V	ID = 1mA, VGS = 0
		VN1306	60				
		VN1304	40				
VGS(th)	Gate Threshold Voltage		0.8		2.4	V	VGS = VDS, ID = 1mA
ΔVGS(th)	Change in VGS(th) with Temperature			−3.9	−5	mV/°C	ID = 1mA, VDS = VGS
IGSS	Gate Body Leakage			0.1	100	nA	VGS = ±20V, VDS = 0
IDSS	Zero Gate Voltage Drain Current				1	uA	VGS = 0, VDS = Max Rating
					100		VGS = 0, VDS = 0.8 Max Rating, TA = 125°C
ID(ON)	ON-State Drain Current		0.25	0.6		A	VGS = 5V, VDS = 25V
			0.50	1.4			VGS = 10V, VDS = 25V
RDS(ON)	Static Drain-to-Source ON-State Resistance			5	15	Ω	VGS = 5V, ID = 50mA
				5	8		VGS = 10V, ID = 500mA
ΔRDS(ON)	Change in RDS(ON) with Temperature			0.8	2	%/°C	ID = 500mA, VGS = 10V
GFS	Forward Transconductance		200	250		m℧	VDS = 25V, ID = 500mA
CISS	Input Capacitance			27	35	pF	VGS = 0V, VDS = 25V, f = 1 MHz
COSS	Common Source Output Capacitance			13	15		
CRSS	Reverse Transfer Capacitance			3	5		
td(ON)	Turn-ON Delay Time			2	5	ns	VDD = 25V, ID = 500mA, RS = 50Ω
tr	Rise Time			2	5		
td(OFF)	Turn-OFF Delay Time			2	5		
tf	Fall Time			2	5		
VSD	Diode Forward Voltage Drop			1.0	1.3	V	ISD = 1.0A, VGS = 0
trr	Reverse Recovery Time			350		ns	ISD = 1.0A, VGS = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

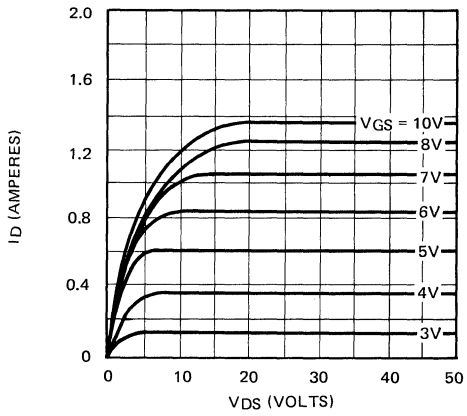
Switching Waveforms and Test Circuit



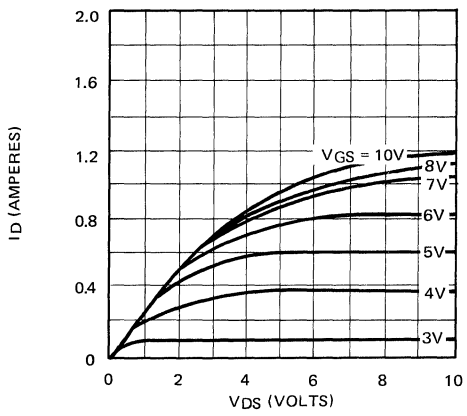


Typical Performance Curves

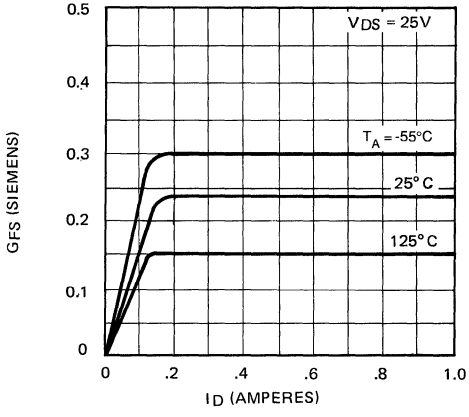
Output Characteristics



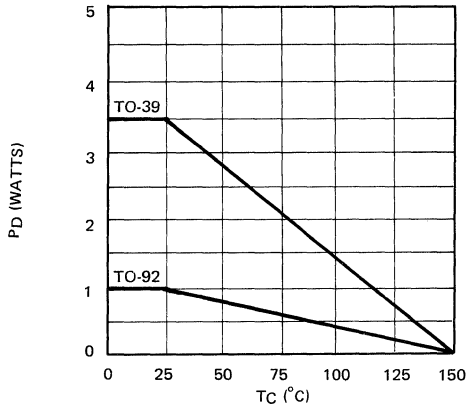
Saturation Characteristics



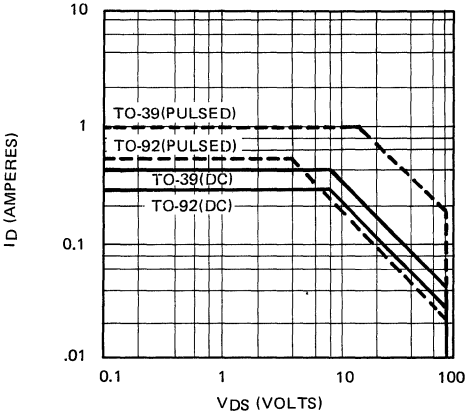
Transconductance Vs. Drain Current



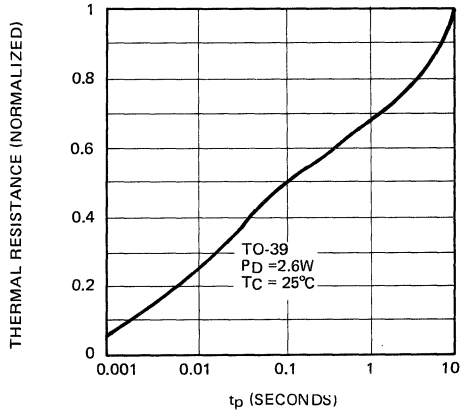
Power Dissipation Vs. Case Temperature



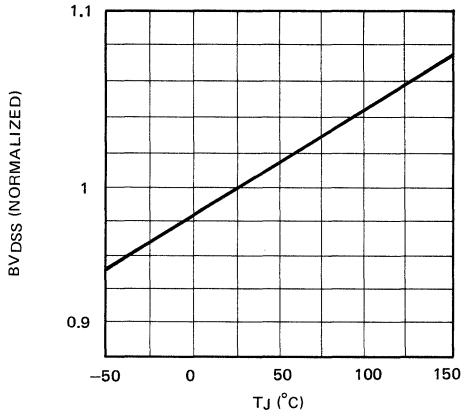
Maximum Rated Safe Operating Area



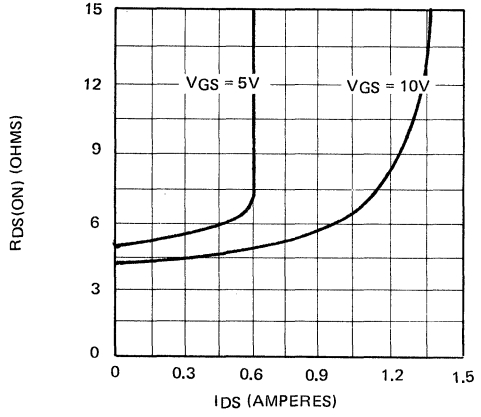
Thermal Response Characteristics



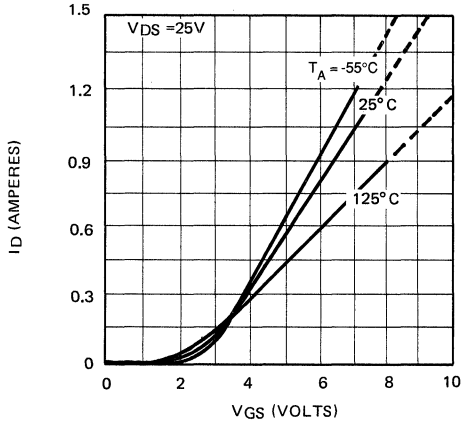
BVDSS Variation with Temperature



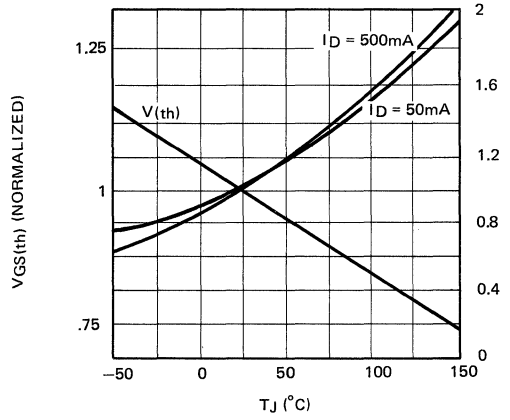
ON - Resistance Vs. Drain Current



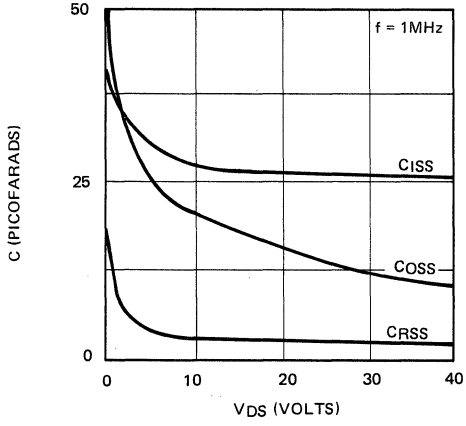
Transfer Characteristics



V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics