



VN13C

7-35-25



N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

$BV_{DSS} /$ BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			TO-39	TO-92
160V	40Ω	250mA	VN1316N2	VN1316N3
200V	40Ω	250mA	VN1320N2	VN1320N3

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{iss} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options

(Note 1)



TO-39



TO-92

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Note 1: See Package Outline section for discrete pinouts.

Thermal Characteristics

T-35-25

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ $T_C = 25^\circ\text{C}$	θ_{JA} $^\circ\text{C/W}$	θ_{JC} $^\circ\text{C/W}$	I_{DR}	I_{DRM}^*
TO-39	150mA	450mA	3.0W	125	41.5	150mA	450mA
TO-92	100mA	400mA	0.8W	155		100mA	400mA

* I_D (continuous) is limited by max rated T_J .Electrical Characteristics (@ 25°C unless otherwise specified)

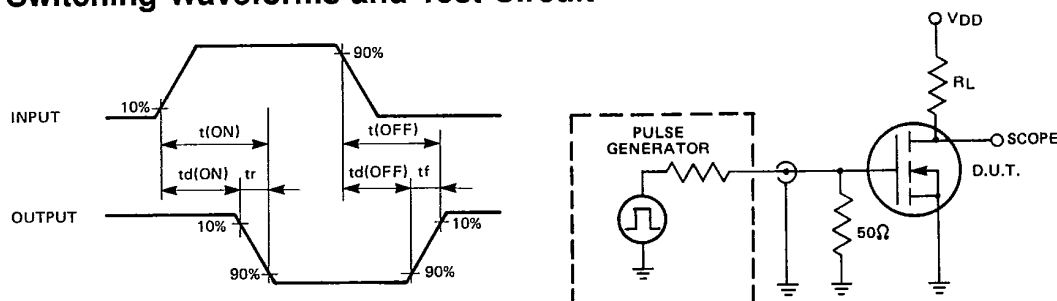
(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BVDS	Drain-to-Source Breakdown Voltage	VN1320	200		V	$I_D = 1\text{mA}$, $V_{GS} = 0$
		VN1316	160			
VGS(th)	Gate Threshold Voltage	1.5		3.5	V	$V_{GS} = V_{DS}$, $I_D = 1\text{mA}$
$\Delta V_{GS}(\text{th})$	Change in $V_{GS}(\text{th})$ with Temperature		-2.0	-4.0	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}$, $I_D = 1\text{mA}$
IGSS	Gate Body Leakage			100	nA	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0$
IDSS	Zero Gate Voltage Drain Current			10	μA	$V_{GS} = 0$, $V_{DS} = \text{Max Rating}$
				500		$V_{GS} = 0$, $V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
ID(ON)	ON-State Drain Current	50	160		mA	$V_{GS} = 5\text{V}$, $V_{DS} = 25\text{V}$
		250	300		mA	$V_{GS} = 10\text{V}$, $V_{DS} = 25\text{V}$
RDS(ON)	Static Drain-to-Source ON-State Resistance	r	30	40	Ω	$V_{GS} = 5\text{V}$, $I_D = 50\text{mA}$
			25	40		$V_{GS} = 10\text{V}$, $I_D = 100\text{mA}$
$\Delta R_{DS}(\text{ON})$	Change in $R_{DS}(\text{ON})$ with Temperature		0.8	2.0	%/ $^\circ\text{C}$	$I_D = 100\text{mA}$, $V_{GS} = 10\text{V}$
GFS	Forward Transconductance	50	70		mS	$V_{DS} = 25\text{V}$, $I_D = 100\text{mA}$
Ciss	Input Capacitance		25	35	pF	$V_{GS} = 0$, $V_{DS} = 25\text{V}$ $f = 1\text{MHz}$
Coss	Common Source Output Capacitance		10	15		
Crss	Reverse Transfer Capacitance		3	5		
td(ON)	Turn-ON Delay Time		1.5	5	ns	$V_{DD} = 25\text{V}$ $I_D = 0.2\text{A}$, $R_S = 50\Omega$
tr	Rise Time		2	5		
td(OFF)	Turn-OFF Delay Time		1.5	5		
tf	Fall Time		2	5		
VSD	Diode Forward Voltage Drop		1.2	2.0	V	$I_S = 1\text{A}$, $V_{GS} = 0$
trr	Reverse Recovery Time		300		ns	$I_S = 1\text{A}$, $V_{GS} = 0$

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)

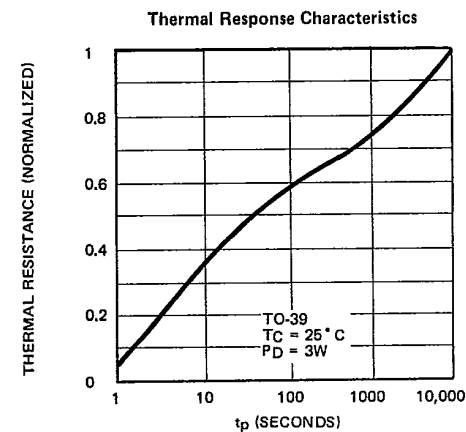
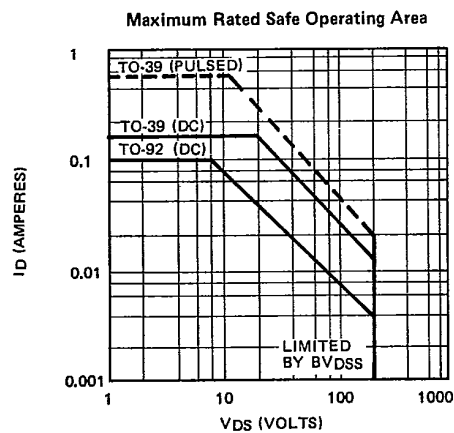
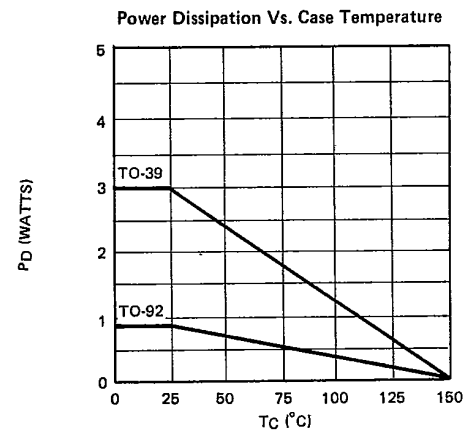
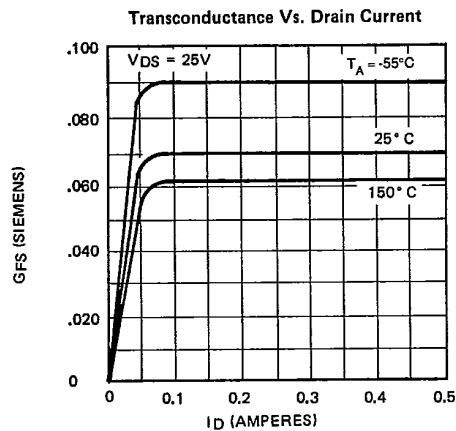
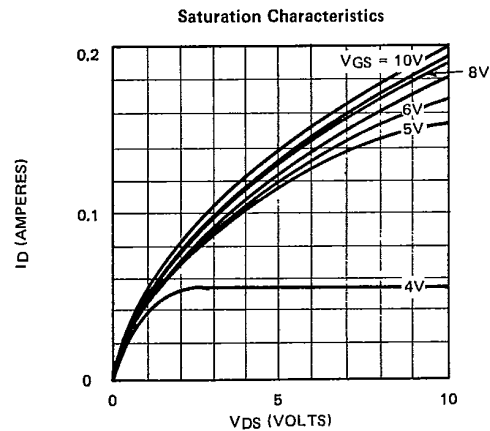
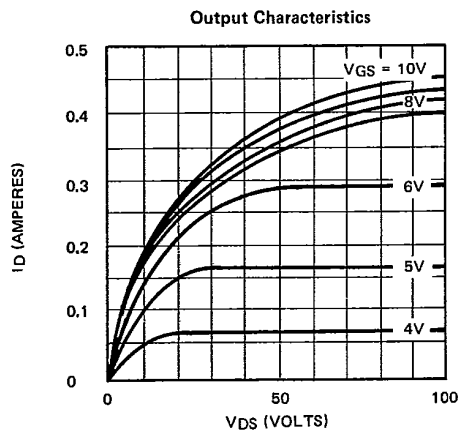
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit



Typical Performance Curves

T-35-25



T-35-25

