



N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

$BV_{DSS} /$ BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package			
			TO-3	TO-39	TO-220	Dice
160V	1 Ω	6.0A	VN1216N1	VN1216N2	VN1216N5	VN1216ND
200V	1 Ω	6.0A	VN1220N1	VN1220N2	VN1220N5	VN1220ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

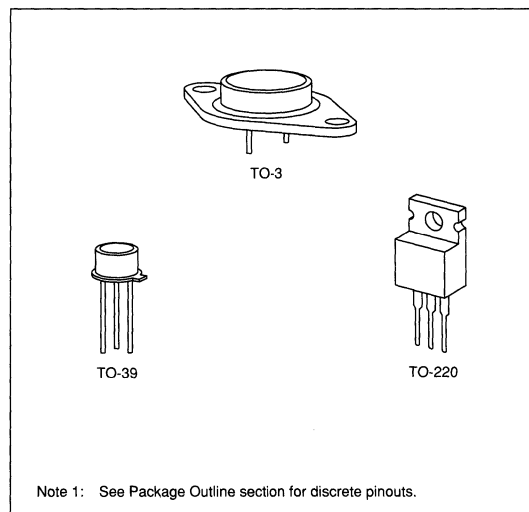
Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	$\pm 20V$
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Package Options

(Note 1)



Note 1: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ $T_C = 25^\circ\text{C}$	θ_{JA} $^\circ\text{C/W}$	θ_{JC} $^\circ\text{C/W}$	I_{DR}	I_{DRM}^*
TO-3	6.0A	14.0A	100W	30	1.25	6A	14A
TO-39	3.0A	11.0A	6.5W	125	20	3A	11A
TO-220	4.5A	13.0A	45W	70	2.75	4.5A	13A

* I_D (continuous) is limited by max rated T_J .

Electrical Characteristics (@ 25°C unless otherwise specified)

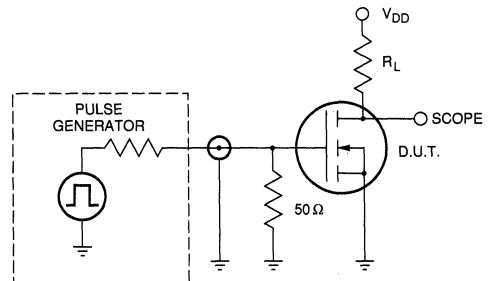
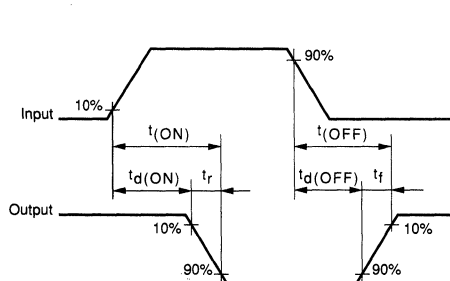
(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN1220 200 VN1216 160			V	$V_{GS} = 0, I_D = 10\text{mA}$
$V_{GS(th)}$	Gate Threshold Voltage	1		3	V	$V_{GS} = V_{DS}, I_D = 10\text{mA}$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature		-3.7	-4.5	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = 10\text{mA}$
I_{GSS}	Gate Body Leakage		1	100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current			100 10	μA mA	$V_{GS} = 0, V_{DS} = \text{Max Rating}$ $V_{GS} = 0, V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current	4 8	8 12		A	$V_{GS} = 5\text{V}, V_{DS} = 25\text{V}$ $V_{GS} = 10\text{V}, V_{DS} = 25\text{V}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		0.7 0.6	1.5 1	Ω	$V_{GS} = 5\text{V}, I_D = 2\text{A}$ $V_{GS} = 10\text{V}, I_D = 2\text{A}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature		1.0	1.4	%/ $^\circ\text{C}$	$V_{GS} = 10\text{V}, I_D = 5\text{A}$
G_{FS}	Forward Transconductance	2.0	3.2		S	$V_{DS} = 25\text{V}, I_D = 5\text{A}$
C_{ISS}	Input Capacitance		550	650		
C_{OSS}	Common Source Output Capacitance		180	250	pF	$V_{GS} = 0, V_{DS} = 25\text{V}$ $f = 1 \text{ MHz}$
C_{RSS}	Reverse Transfer Capacitance		12	20		
$t_{d(ON)}$	Turn-ON Delay Time		8	20		
t_r	Rise Time		10	20	ns	$V_{DD} = 25\text{V}$ $I_D = 2\text{A}$ $R_S = 50\Omega$
$t_{d(OFF)}$	Turn-OFF Delay Time		30	90		
t_f	Fall Time		30	60		
V_{SD}	Diode Forward Voltage Drop		1.3	2.5	V	$V_{GS} = 0, I_{SD} = 2\text{A}$
t_{rr}	Reverse Recovery Time		500		ns	$V_{GS} = 0, I_{SD} = 1\text{A}$

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

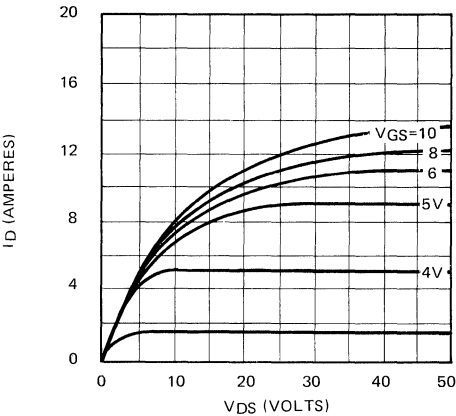
Switching Waveforms and Test Circuit



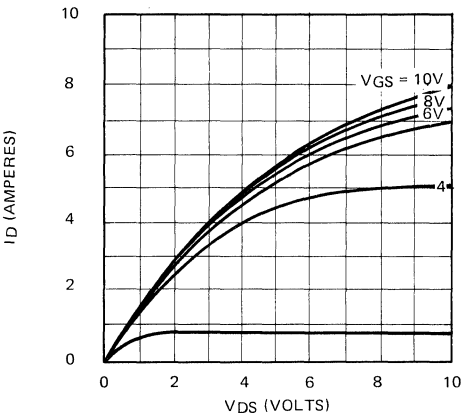
Typical Performance Curves

VN12C

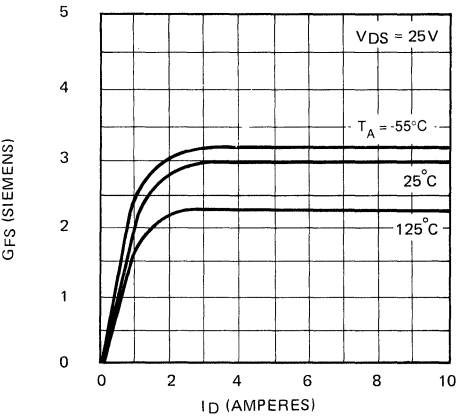
Output Characteristics



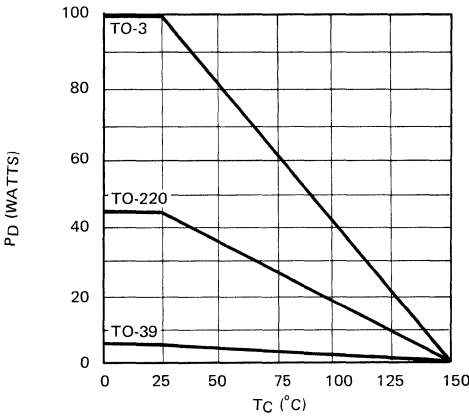
Saturation Characteristics



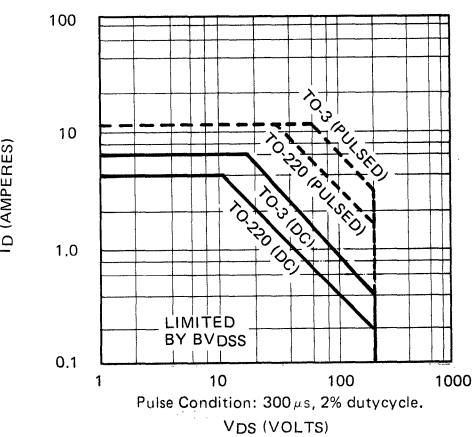
Transconductance Vs. Drain Current



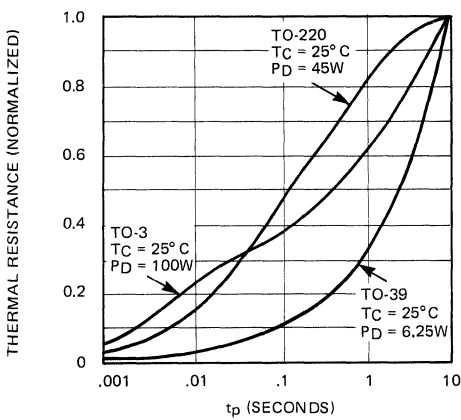
Power Dissipation Vs. Case Temperature



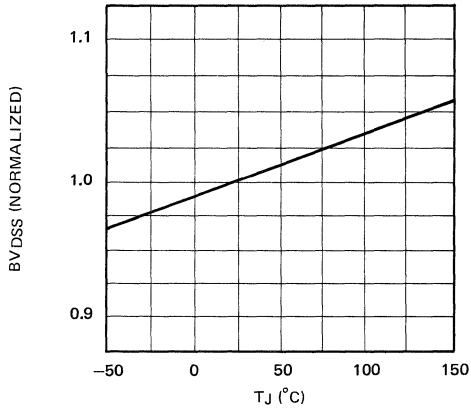
Maximum Rated Safe Operating Area



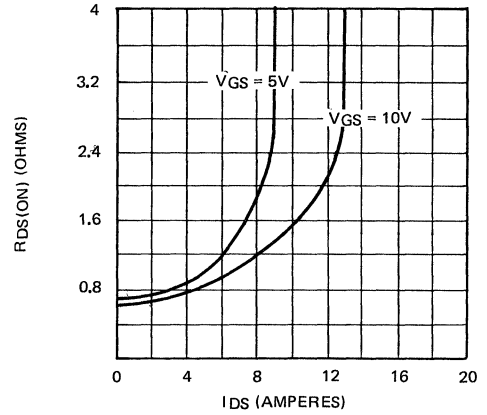
Thermal Response Characteristics



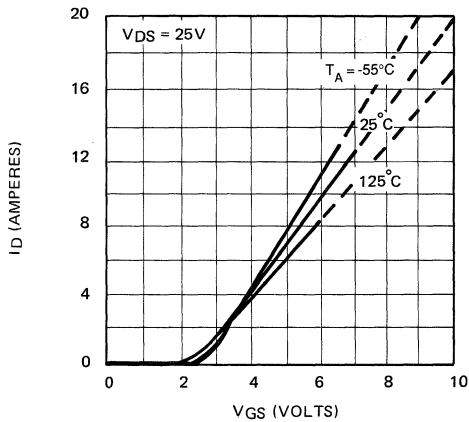
BVDSS Variation with Temperature



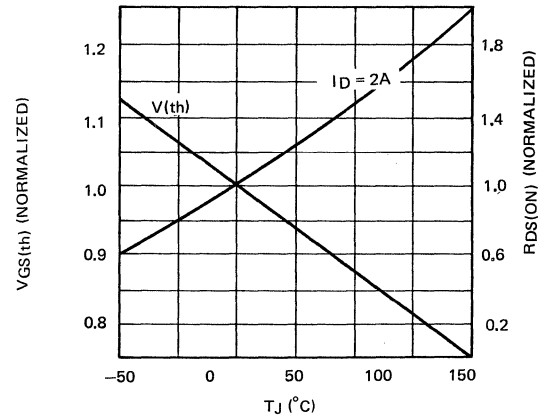
ON-Resistance Vs. Drain Current



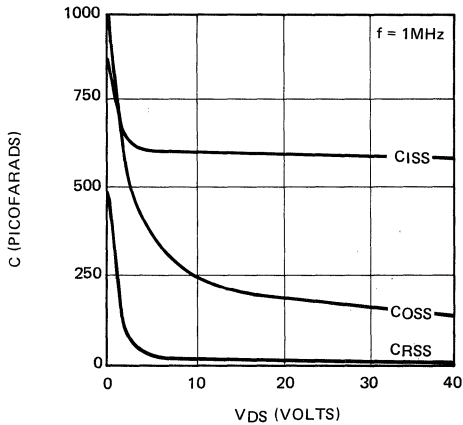
Transfer Characteristics



V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics

