



# N-Channel Enhancement-Mode Vertical DMOS Power FETs

## **Ordering Information**

BV <sub>DSS</sub> /	R <sub>DS(ON)</sub>	I <sub>D(ON)</sub>	Order Number / Package TO-92		
BV <sub>DGS</sub>	(max)	(min)			
60V	3Ω	1.5A	VN0606L		
60V	5Ω	0.75A	VN0610LL		

#### Features

- □ Freedom from secondary breakdown
- □ Low power drive requirement
- Ease of paralleling
- Low C<sub>ISS</sub> and fast switching speeds
- □ Excellent thermal stability
- Integral Source-Drain diode
- □ High input impedance and high gain
- □ Complementary N- and P-Channel devices

## Applications

- Motor control
- □ Converters
- □ Amplifiers
- Switches
- Power supply circuits
- Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

### **Absolute Maximum Ratings**

Drain-to-Source Voltage	BV <sub>DSS</sub>
Drain-to-Gate Voltage	BV <sub>DGS</sub>
Gate-to-Source Voltage	±40V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

\*Distance of 1.6 mm from case for 10 seconds.

### Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicongate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermallyinduced secondary breakdown.

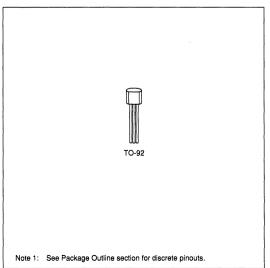
Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### **Package Options**

(Note 1)

VN0606

VN0610



#### **Thermal Characteristics**

Package	I <sub>D</sub> (continuous)*	I <sub>D</sub> (pulsed)	Power Dissipation @ T <sub>c</sub> = 25°C	θ <sub>ja</sub> ∘C/W	θ <sub>jc</sub> ∘C/W
TO-92	0.3A	2.0A	.4W	312.5	51

\*I<sub>D</sub> (continuous) is limited by max rated T<sub>i</sub>.

#### **Electrical Characteristics** (@ 25°C unless otherwise specified)

(Notes 1 and 2)

Symbol	Parameter		Min	Тур	Max	Unit	Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	VN0610	60			v	$I_{D} = 100 \mu A, V_{GS} = 0$
		VN0606	60			ν	$I_D = 10\mu A$ , $V_{GS} = 0$
V <sub>GS(th)</sub>	Gate Threshold Voltage	VN0610	0.8		2.5	v	$V_{GS} = V_{DS}, I_{D} = 1mA$
		VN0606	0.8		2.0	V	$V_{GS} = V_{DS}, I_{D} = 1mA$
IGSS	Gate Body Leakage				100	nA	$V_{GS} = \pm 15V$ , $V_{DS} = 0$
DSS	Zero Gate Voltage Drain Current				10	μA	$V_{GS} = 0V, V_{DS} = Max Rating$
				500	$V_{GS} = 0V, V_{DS} = Max Rating$ T <sub>A</sub> = 125°C		
<sup>I</sup> D(ON)	ON-State Drain Current	VN0610	0.75			А	$V_{GS}$ = 10V, $V_{DS} \ge 2 V_{DS(ON)}$
		VN0606	1.5				$V_{GS} = 10V, V_{DS} \ge 2 V_{DS(ON)}$
RDS(ON)	Static Drain-to-Source ON-State Resistance	VN0610			7.5		$V_{GS} = 5V, I_{D} = 0.2A$
		VN0610			5	Ω	$V_{GS} = 10V, I_D = 0.5A$
		VN0606			3		$V_{GS} = 10V, I_{D} = 1A$
G <sub>FS</sub>	Forward Transconductance		170			mΰ	$V_{DS} \ge 2 V_{DS(ON)}$ , $I_D = 0.5A$
CISS	Input Capacitance				50		$V_{GS}$ = 0, $V_{DS}$ = 25V f = 1MHz
COSS	Common Source Output Capacitance				25	pF	
C <sub>RSS</sub>	Reverse Transfer Capacitance				5		
<sup>t</sup> (ON)	Turn-ON Time				10	20	$V_{DD} = 25V, I_D = 1A$
<sup>t</sup> (OFF)	Turn-OFF Time				10	ns	$R_S = 50\Omega$
V <sub>SD</sub>	Diode Forward Voltage Drop	VN0610		-1.2		V	$I_{SD} = -0.47A, V_{GS} = 0$
		VN0606		85			$I_{SD} = -0.2A, V_{GS} = 0$

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

### Switching Waveforms and Test Circuit

