



N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

$BV_{DSS} /$ BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-39	TO-92	Dice
450V	60Ω	150mA	VN0545N2	VN0545N3	VN0545ND
500V	60Ω	150mA	VN0550N2	VN0550N3	VN0550ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

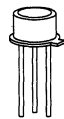
Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options

(Notes 1 and 2)



TO-39



TO-92

Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Thermal Characteristics

Package	ID (continuous)*	ID (pulsed)*	Power Dissipation @ $T_c = 25^\circ\text{C}$	θ_{jc} $^\circ\text{C/W}$	θ_{ja} $^\circ\text{C/W}$	I_{DR}	I_{DRM}^*
TO-39	100mA	300mA	6W	20	125	100mA	300mA
TO-92	50mA	250mA	1W	125	170	50mA	250mA

* I_D (continuous) is limited by max rated T_j .

Electrical Characteristics (@ 25°C unless otherwise specified)

(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BVDSS	Drain-to-Source Breakdown Voltage	VN0550	500			V	$V_{GS} = 0, I_D = 1\text{mA}$
		VN0545	450				
VGS(th)	Gate Threshold Voltage		2		4	V	$V_{GS} = V_{DS}, I_D = 1\text{mA}$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.8	-5	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = 1\text{mA}$
IGSS	Gate Body Leakage				100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0$
IDSS	Zero Gate Voltage Drain Current				10	μA	$V_{GS} = 0, V_{DS} = \text{Max Rating}$
					1000		$V_{GS} = 0, V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
ID(ON)	ON-State Drain Current			100		mA	$V_{GS} = 5\text{V}, V_{DS} = 25\text{V}$
			150	200			$V_{GS} = 10\text{V}, V_{DS} = 25\text{V}$
RDS(ON)	Static Drain-to-Source ON-State Resistance			50		Ω	$V_{GS} = 5\text{V}, I_D = 50\text{mA}$
				45	60		$V_{GS} = 10\text{V}, I_D = 50\text{mA}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			1	1.7	%/ $^\circ\text{C}$	$V_{GS} = 10\text{V}, I_D = 50\text{mA}$
GFS	Forward Transconductance		50	75		$\text{m}\Omega^{-1}$	$V_{DS} = 25\text{V}, I_D = 50\text{mA}$
Ciss	Input Capacitance			45	55	pF	$V_{GS} = 0, V_{DS} = 25\text{V}$ $f = 1 \text{ MHz}$
Coss	Common Source Output Capacitance			8	10		
CRSS	Reverse Transfer Capacitance			2	5	ns	$V_{DD} = 25\text{V}$ $I_D = 50\text{mA}$ $R_S = 50\Omega$
td(ON)	Turn-ON Delay Time			3	5		
tr	Rise Time			3	5		
td(OFF)	Turn-OFF Delay Time			3	5		
tf	Fall Time			3	5		
VSD	Diode Forward Voltage Drop			0.8		V	$V_{GS} = 0, I_{SD} = 0.5\text{A}$
trr	Reverse Recovery Time			300		ns	$V_{GS} = 0, I_{SD} = 0.5\text{A}$

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: $300\mu\text{s}$ pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

