VLSI TECHNOLOGY, INC.

T-75-37-07

VL86C410

RISC I/O CONTROLLER (IOC)

FEATURES

- Power on reset control
- Four independent 16-bit programmable counters
  –Two timers
  –Two baud rate generators
- Bidirectional serial keyboard interface
- Six programmable bidirectional control pins
- Interrupt mask, request and status registers for –IRQ and –FIRQ
- 14 level triggered interrupt inputs
- Two edge triggered interrupt inputs
- Four programmable peripheral cycles
  – Slow
  – Medium
  – Fast
  – 2 MHz synchronous
- Seven external peripheral selects
- ARM/IO bus interface control
- Expansion bus buffer control

DESCRIPTION

The VL86C410 Input/Output Controller (IOC) is designed to interface to the VL86C010/VL86C110/VL86C310 chip set to provide a unified view of interrupts and peripherals within an Acorn RISC Machine (ARM) based computer. It controls an 8-to-32 bit I/O data bus to which on-board peripherals and any I/O expansions are connected. It provides a set of internal functions, which are accessed without wait states, and programmable speed access to external peripherals.

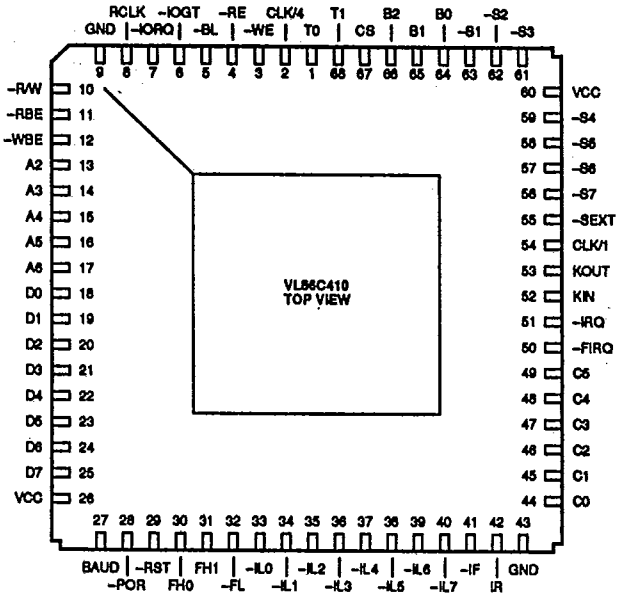
The VL86C410 provides system level I/O with six programmable control pins and a full-duplex, bidirectional serial keyboard interface. To support system timing requirements, the VL86C410 contains four independent programmable counters. Two of these counters are used as baud rate generators. One is dedicated to the keyboard and the other controls the BAUD output pin to generate a free-running clock. The other two counters can be used to generate system timing events.

The IOC serves as the interface between the very high-speed RISC system bus and the slower I/O or expansion bus. The part provides all the buffer control required between the two buses. The VL86C410 supports an interruptable I/O cycle thats allows the system to use slower, low-cost peripheral controllers such as the VL16C450 Asynchronous Communications Element and VL1772 Floppy Disk Controller without severe latency on the system bus.

Peripheral controllers are supported with 16 interrupt inputs (14 level sensitive and two edge-triggered), seven peripheral select outputs, and four programmable I/O cycle times.

PIN DIAGRAM

JEDEC TYPE-B CERAMIC LEADLESS CHIP CARRIER



ORDER INFORMATION

Part Number	Clock Frequency	Package
VL86C410-08QC	8 MHz	Plastic Leaded Chip Carrier (PLCC)
VL86C410-08LC		JEDEC Type-B Ceramic Carrier

Note: Operating temperature is 0°C to +70°C.

PLEASE CONSULT RISC FAMILY DATA MANUAL FOR DETAILED INFORMATION