VL86C310

RISC VIDEO CONTROLLER (VIDC)

FEATURES

- Pixel rate selectable as 8, 12, 16, or 24 MHz
- Serializes data to 1-, 2-, 4-, or 8- bits per pixel
- 16 x 13-bit words - 4096 color lookup palette
- Three 4-bit DACs (one for each CRT gun)
- Fully programmable screen parameters
- Screen border in any of the 4096 possible colors
- Flexible cursor sprite
- Support for interlaced display format
- External synchronization capability
- Very high resolution monochrome mode support
- High quality stereo sound generation

DESCRIPTION

The Video Controller (VIDC) accepts video data from DRAM under DMA control, serializes and passes it through a color look-up palette, and converts it to analog signals for driving the CRT guns. The chip also controls all the display timing parameters plus the position and pattern of the cursor sprite. In addition, the VIDC includes an exponential DAC and stereo image table for the generation of high quality sound from data in the DRAM.

The VIDC requests data from the RAM when required, and buffers it in one of three first-in, first-out memories (FIFOs). Note that the addressing of the data in RAM is controlled elsewhere in the system (usually in the VL86C110 Memory Controller, MEMC). Data is requested in blocks of four 32-bit words, allowing efficient use of page-mode DRAM without locking up the system data bus for long periods.

The VIDC is a highly programmable device, offering a very wide choice of display formats. The pixel rate can be selected in a range between 8 and 24 MHz and the data can be serialized to either 8-, 4-, 2-, or 1-bit per pixel. The horizontal timing parameters can be controlled to units of 2 pixels, and the vertical timing parameters can be controlled in units of a raster. The color lookup palette which drives the three on-chip DACs is 13-bits wide, offering a choice from 4096 colors or an external video source.

Extensive use is made of pipelining throughout the device.

The cursor sprite is 32 pixels wide, and any number of rasters high. Three simultaneous colors (from the 4096 possible) are supported, and any pixel can be defined as transparent, making possible cursors of many shapes. The cursor can be positioned anywhere on the screen.

The sound system implemented on the device can support up to eight channels, each with a separate stereo position.

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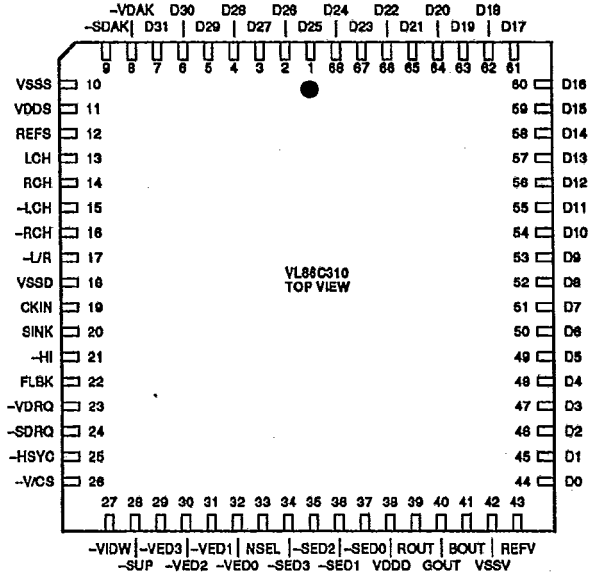
PIN DIAGRAM

PLASTIC LEADED CHIP CARRIER

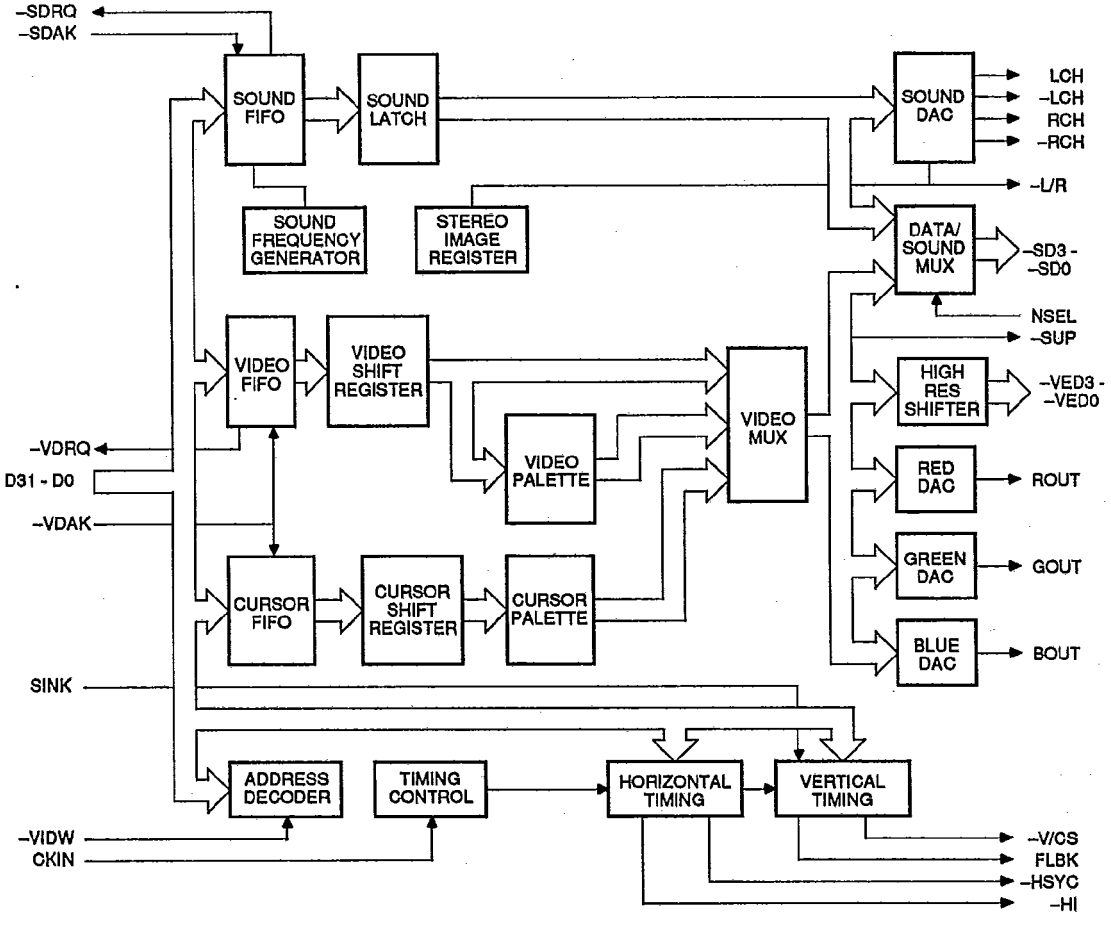


ORDER INFORMATION

Part Number	Clock Frequency	Package
VL86C310-12QC	12 MHz	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature is 0°C to +70°C.

BLOCK DIAGRAM



SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
CKIN	19	Clock In (TTL level input); Master 24 MHz system clock input - Usually this is the same signal as the VL86C110 Memory Controller (MEMC) uses to generate system timing. Since VIDC resynchronizes all its inputs to this clock reference, these two clocks are not required to be the same frequency, allowing the display frequency to be independent of the processor.
–VIDW	27	Register Write Strobe (TTL level input) - An active low on this line writes data into one of the VIDC registers. The address of the register is supplied on the upper bits, and the data to be written on the lower bits of the data bus. Normally, this signal is generated by MEMC as it is the device that decodes the memory address map in the system.
D31-D0	7-1, 68-44	Data Bus (TTL level inputs) - This 32-bit bus carries data for register writes, video DMA, cursor DMA, and sound DMA, according to which type of data strobe is present.
–VDRQ	23	Video Data Request (CMOS level output) - This signal is driven active (low) when the VIDC requires another block of 16 bytes of video data (when –HSYC is high) or cursor data (when –HSYC is low). It is driven high again by the first valid video data acknowledge, –VDAK.
–VDAK	8	Video Data Acknowledge (TTL level input) - An active low on this signal strobes a data word into the video or cursor FIFO depending on the state of HSYNC when the request was made. Note that a low on –VDRQ signifies a request for four words of data, and so –VDAK must go low four times to service each request.
–SDRQ	24	Sound Data Request (CMOS level output) - This signal is driven low when the VIDC requires another block of 16 bytes of sound data. It is driven high again by the first valid –SDAK.
–SDAK	9	Sound Data Acknowledge (TTL level input) - An active low on this signal strobes a data word into the sound FIFO. Note that a low on –SDRQ signifies a request for four words of data, and so –SDAK must go low four times to service each request.
FLBK	22	Vertical Flyback (CMOS level output) - This signal is driven high when the display is in vertical flyback (retrace). Specifically, it is set high at the start of the first raster which is not display data, although this may be border, (at the bottom of the screen), and is cleared down at the start of the first raster which is display data (at the top of the screen).
SINK	20	External Synchronization pulse (TTL level input) - A high on this signal resets the vertical timing counter, and if interlaced display format is being used, the odd field is selected. The horizontal timing counter, and all other registers are unaffected by this signal.
–HI	21	Horizontal Interlace Marker (Test pin - CMOS level output) - When an interlaced display format is selected this signal is driven low half way along the raster and stays low until the end of each raster. If non-interlaced displays are used, this pin may be used as a programmable timer on each raster.
–SD3 - –SD0	34-37	Multiplexed Sound Data (Test pins - CMOS level outputs) - These pins are used for testing the digital data paths through the chip. Normally, depending on the state of NSEL, they output the inverse of one of the two nibbles of the data byte being fed to the sound DAC, but in test mode three, they output the inverse of the data being fed to the green or blue DACs, again depending on the state of NSEL. For more information on test mode three, refer to the control register section.
NSEL	33	Sound Data Ouput Selector (Test pin - TTL level input) - When this signal is low, the sound data bus port outputs the low nibble of the sound data, or the green DAC data. When NSEL is high, the sound data bus port outputs the high nibble of the sound data, or the blue DAC data.
–L/R	17	Left/Right (Test pin - TTL level output) - This signal is driven low when the sound output is steered to the left output port, and is high when the sound output is steered to the right output port. In test mode three, the pin changes its function, and outputs the sound sampling clock instead.
REFV	43	Video DAC Reference Current (Analog input) - A current must be fed into this pin to set the output current of the video DACs. The full scale output current is 15 times this current. In most applications a resistor from VDD to this pin is sufficient to set the current.

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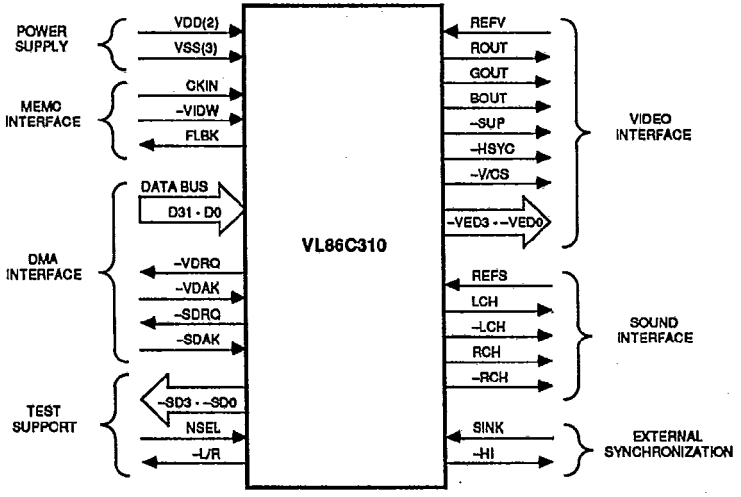
SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Description
ROUT	39	Red Analog output (Analog output) - The output to the CRT guns is in the form of a current sink. Maximum brightness is defined as 15 times the reference current, and "black" is defined as zero current. Level shifting and buffering is normally required to drive the CRT inputs.
GOUT	40	Green Analog output (Analog output) - Same description as for ROUT.
BOUT	41	Blue Analog output (Analog output) - Same description as for ROUT.
–SUP	28	Supremacy output signal (CMOS level output) - This signal is used to control a multiplexer between the output of VIDC and an external source when video mixing is required. If bit 12 of the video or cursor palette for any logical color is set, –SUP is driven low when that logical color is displayed. In this way any logical color can be defined as being supreme or not, on a pixel-by-pixel basis.
–HSYC	25	Horizontal Synchronization pulse (CMOS level output) - This signal is required by some monitors. It is also used by the MEMC to discriminate between cursor and video data requests. The pulse is active low, and the pulse width is programmable in units of two pixels, though there are certain system-related restrictions. See section Restrictions On Parameters.
–V/CS –VED0	26	Vertical/Composite Synchronization pulse (CMOS level output) - Depending on bit seven in the control register, this pin can be either the vertical sync pulse, or a form of composite sync pulse. The vertical sync pulse width is programmable in units of a raster and, if selected, is active low. The composite sync pulse is the XNOR of –HSYC and –VSYC.
–VED3 -	39-32	Video External Data output (CMOS level output) - The inverse of the four bits of data which are fed to the red DAC are output on these pins. With an external serializer, this data can be used to produce very high resolution monochrome displays.
REFS	12	Sound DAC Reference Current (Analog input) - A current must be fed into this pin to set the output current of the sound DAC. The full scale output current is approximately 32 times this current. In most applications, a resistor from VDD to this pin is sufficient to set the current.
LCH	13	Left Channel Positive Sound output (Analog output) - The sound output is the form of a current sink which is switched to one of four pins (pins 13-16). The left channel signal is produced by externally integrating and subtracting the two signals, LCH and –LCH. Similarly, the right channel signal is produced by externally integrating and subtracting the two signals RCH and –RCH.
–LCH	14	Left Channel Negative Sound output (Analog output) - See description of LCH.
RCH	15	Right Channel Positive Sound output (Analog output) - See description of LCH.
–RCH	16	Right Channel Negative Sound output (Analog output) - See description of LCH.
VSSD	18	Power (Digital ground) - This pin is the ground supply to the digital circuits in the device.
VSSS	10	Power (Sound ground) - This pin is the ground supply to the sound DAC in the device. It must be connected to the pin VSSD outside the chip.
VSSV	42	Power (Video ground) - This pin is the ground supply to the video DACs in the device. It must be connected to the pin VSSD outside the chip.
VDDD	38	Power (Digital +5 V ±5% supply) - This pin is the positive supply to the digital circuits in the device.
VDDS	11	Power (Sound +5 V ±5% supply) - This pin is the positive supply to the sound DAC in the device. It must be at the same potential as VDDD, and should be decoupled to VSSS. Note that the sound reference current input and the sound analog output currents are all referenced to this signal.

FUNCTIONAL PIN DIAGRAM



FUNCTIONAL DESCRIPTION

Apart from the three 32-bit wide FIFOs (video, cursor, and sound), the VIDC contains 46 write-only registers of up to 13-bits each. In all cases the address of the register is contained in the top 6-bits (31-26) of the data field. Bits 25 and 24 are not used. The actual data bits are distributed among the remaining 24-bits of the data field according to the register in question. The encoding format is shown in Figure 1.

Treating bit 24 as the least significant address bit, the register map is shown in Table 1 on the following page. Note that there are 18 undefined locations. These locations should never be written to as they may actually contain other registers. (Some registers are dual-mapped within the device.)

In order to define the display format, eleven registers must be programmed. Screen parameter definitions are shown in Figure 2 on the following page.

Video Palette Logical Colors 0-FH: Addresses 00-3CH

In 1-, 2-, and 4-bits per pixel mode, data bits D12-D0 define the physical color corresponding to that logical color. The data bus encoding is shown in Figure 3. Figure 4 shows the physical color field specification.

FIGURE 1. DATA BUS ENCODING FORMAT

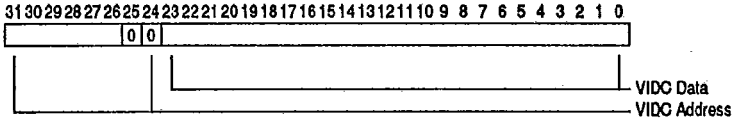


FIGURE 3. VIDEO PALETTE LOGICAL COLOR FORMAT

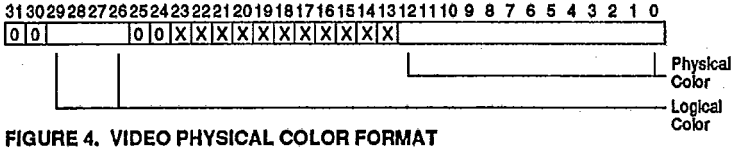


FIGURE 4. VIDEO PHYSICAL COLOR FORMAT

12	11	10	9	8	7	6	5	4	3	2	1	0
SUP	BLUE				GREEN				RED			
D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

D3-D0 define the red amplitude (D0 least significant)
D7-D4 define the green amplitude (D4 least significant)
D11-D8 define blue amplitude (D8 least significant)
D12 defines the supremacy bit for that color

In 8-bits per pixel mode, only 9-bits are defined as shown in Figure 5. The palette outputs define the least significant bits of each color. The most significant bits for each color now come directly from the upper 4-bits of the logical color field, giving the physical data field as shown in Figure 6.

In four and 8-bits per pixel mode, all 16 locations should be programmed. In 2-bits per pixel mode only colors zero, one, two, and three need to be defined. In 1-bit per pixel mode, only colors zero and one need to be programmed.

Border Color Register: Address 40H

In all modes, this register defines the border physical color. The data bus encoding is shown in Figure 7.

D3-D0 define the red amplitude (D0 least significant)
D7-D4 define the green amplitude (D4 least significant)
D11-D8 define the blue amplitude (D8 least significant)
D12 defines the supremacy bit for the border

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FIGURE 2. VL86C310 DISPLAY PARAMETERS

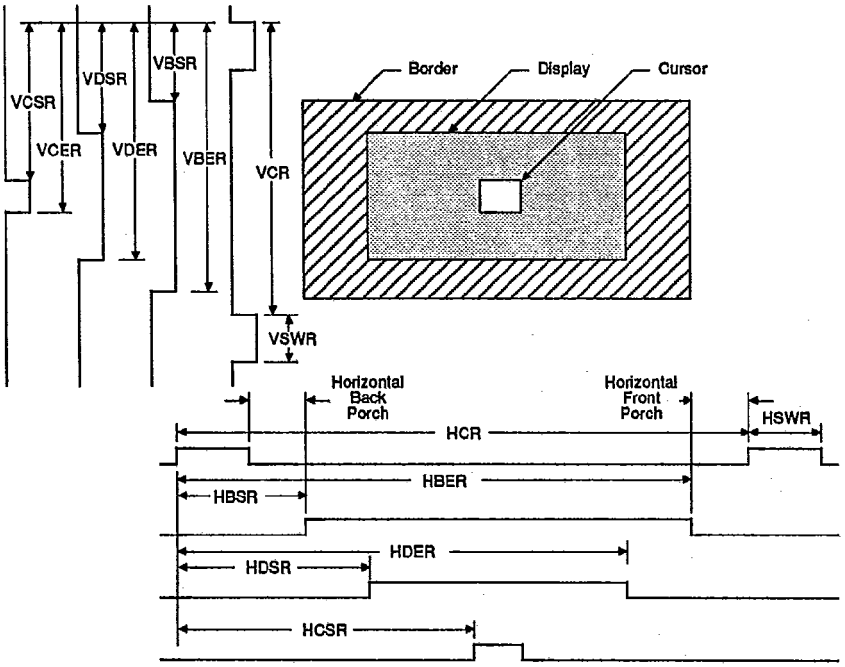

TABLE 1. REGISTER ADDRESS ASSIGNMENTS

Address (Hex)	Register Function	Address (Hex)	Register Function	Address (Hex)	Register Function
00	Video Palette Logical Color 0	44	Cursor Palette Logical Color 1	94	Horizontal Border End Register
04	Video Palette Logical Color 1	48	Cursor Palette Logical Color 2	98	Horizontal Cursor Start Register
08	Video Palette Logical Color 2	4C	Cursor Palette Logical Color 3	9C	Horizontal Interlace Register
0C	Video Palette Logical Color 3	50 - 5C	Reserved	A0	Vertical Cycle Register
10	Video Palette Logical Color 4	60	Stereo Image Register 7	A4	Vertical Sync Width Register
14	Video Palette Logical Color 5	64	Stereo Image Register 0	A8	Vertical Border Start Register
18	Video Palette Logical Color 6	68	Stereo Image Register 1	AC	Vertical Display Start Register
1C	Video Palette Logical Color 7	6C	Stereo Image Register 2	B0	Vertical Display End Register
20	Video Palette Logical Color 8	70	Stereo Image Register 3	B4	Vertical Border End Register
24	Video Palette Logical Color 9	74	Stereo Image Register 4	B8	Vertical Cursor Start Register
28	Video Palette Logical Color A	78	Stereo Image Register 5	BC	Vertical Cursor End Register
2C	Video Palette Logical Color B	7C	Stereo Image Register 6	C0	Sound Frequency Register
30	Video Palette Logical Color C	80	Horizontal Cycle Register	C4 - DC	Reserved
34	Video Palette Logical Color D	84	Horizontal Sync Width Register	E0	Control Register
38	Video Palette Logical Color E	88	Horizontal Border Start Register	E4 - FC	Reserved
3C	Video Palette Logical Color F	8C	Horizontal Display Start Register		
40	Border Color Register	90	Horizontal Display End Register		

FIGURE 5. VIDEO PALETTE DATA ENCODING FOR 8 BITS PER PIXEL MODE

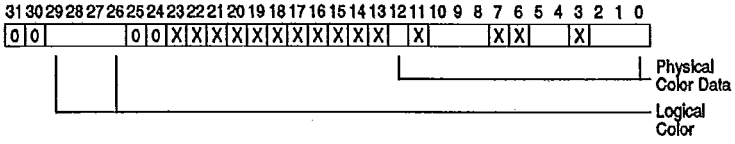

FIGURE 6. VIDEO PALETTE DEFINITION FOR 8 BITS PER PIXEL MODE

12	11	10	9	8	7	6	5	4	3	2	1	0
SUP	BLUE				GREEN				RED			
D12*	L7**	D10*	D9*	D8*	L6**	L5**	D5*	D4*	L4**	D2*	D1*	D0*

* Dn: These bits are from the palette field.
** Ln: These bits are from the logical field.

Cursor Palette Logical Colors 1-3: Address 44-4CH

In all modes, these registers define the physical cursor colors corresponding to the logical colors. Note that cursor logical color 00 is transparent (i.e., no cursor display), and this location is used for the Border Color Register. Figure 8 illustrates the data bus encoding for this register.

D3-D0 define the red amplitude (D0 least significant)
D7-D4 define the green amplitude (D4 least significant)
D11-D8 define the blue amplitude (D8 least significant)
D12 defines the supremacy bit for that cursor color

Stereo Image Registers, Channels 0-7: Addresses 60H-7CH

These eight registers define the stereo image position for each of the eight possible channels as shown in Table 1.

When only four channels are used, registers 4, 5, 6, 7 should be programmed to the same values as registers 0, 1, 2, 3 respectively. If only two channels are used, registers 0, 2, 4, and 6 pertain to one channel, and so should be programmed to the same value, and registers 1, 3, 5, and 7 pertain to the other channel. When only one channel is used, all eight registers should be programmed with the same value. The 3-bit value is defined in Table 2 and data bus encoding is shown in Figure 9.

FIGURE 7. BORDER COLOR REGISTER DATA BUS ENCODING

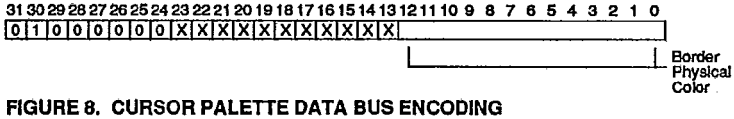

FIGURE 8. CURSOR PALETTE DATA BUS ENCODING

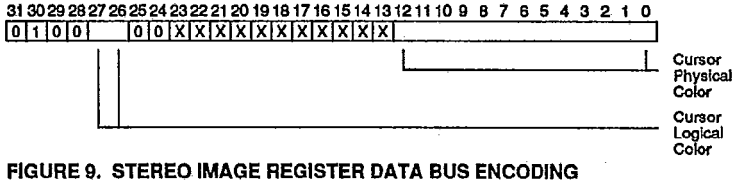

FIGURE 9. STEREO IMAGE REGISTER DATA BUS ENCODING

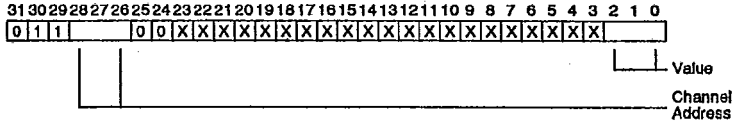

FIGURE 10. HORIZONTAL CYCLE REGISTER DATA BUS ENCODING

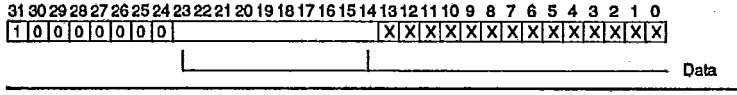

TABLE 2. STEREO IMAGE REGISTER VALUES

Value	Stereo Image Position
0	Undefined
1	100% Left Channel
2	83% Left Channel
3	67% Left Channel
4	Center
5	67% Right Channel
6	83% Right Channel
7	100% Right Channel

Horizontal Cycle Register (HCR): Address 80H

This register defines the period, in units of two pixels, of the horizontal scan (i.e., display time + horizontal retrace time). If N pixels are required in the horizontal scan period, then a value of (N-2)/2 should be programmed into the HCR (N must be even). If interlace display is selected, N/2 must also be even. This is a 10-bit register, with bit 14 the least significant. Data bus encoding is shown in Figure 10.

Horizontal Sync Width Register (HSWR): Address 84H

This register defines the width, in units of two pixel periods, of the horizontal sync pulse. Encoding of the data bus is shown in Figure 11. If N pixels are required in the horizontal sync pulse, then value (N-2)/2 should be programmed into the HSWR. (N must be even.) The minimum value programmed may be 0, but system constraints impose a larger minimum value. See section Restriction On Parameters. This is a 10-bit register, with bit 14 the least significant.

Horizontal Border Start Register (HBSR): Address 88H

This register defines the time, in units of two pixel periods, from the start of –HSYC pulse to the start of the border display. If M pixels are required in this time, then value (M-1)/2 should be programmed into the HBSR. (M must be odd.) Note that this register must

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FIGURE 11. HORIZONTAL SYNC WIDTH REGISTER DATA BUS ENCODING

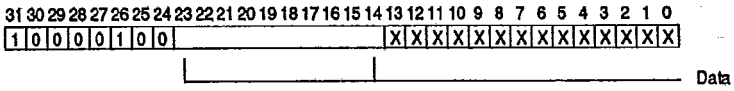


FIGURE 12. HORIZONTAL BORDER START REGISTER DATA BUS ENCODING

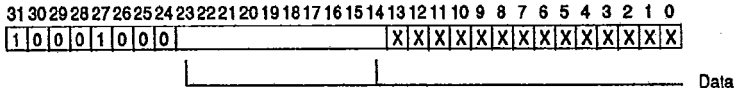


FIGURE 13. HORIZONTAL DISPLAY START REGISTER DATA BUS ENCODING

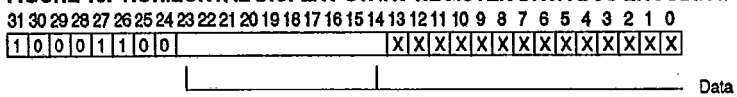


FIGURE 14. HORIZONTAL DISPLAY END REGISTER DATA BUS ENCODING

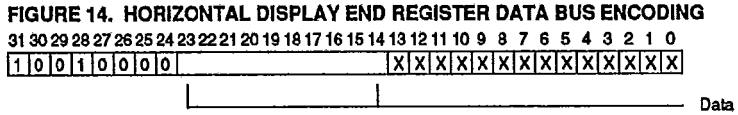


FIGURE 15. HORIZONTAL BORDER END REGISTER DATA BUS ENCODING

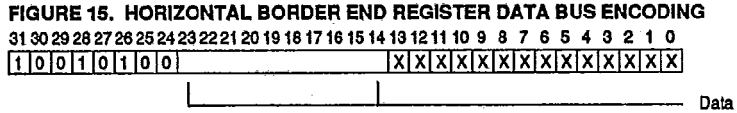
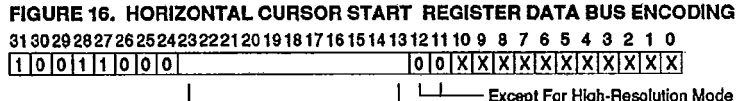


FIGURE 16. HORIZONTAL CURSOR START REGISTER DATA BUS ENCODING



always be programmed, even when a border is not required. If a border is not required, then the value in the HBSR must be such as to start the border in the same place as the display start (i.e, M[HBSR] = M[HDSR]). This is a 10-bit register with bit 14 the least significant. Data bus encoding is shown in Figure 12.

Horizontal Display Start Register (HDSR): Address 8CH

This register defines the time, in units of two pixel periods, from the start of the –HSYC pulse to the beginning of the video display. The value programmed here depends on the screen mode in use. If M pixels are required in this time, then: in 8-bits per pixel mode, the value (M-5)/2 should be program-med into the HDSR; in 4-bits per pixel mode, value (M-7)/2 should be programmed into the HDSR; in 2-bits per pixel mode, value (M-11)/2 should be programmed into the HDSR; in 1-bit per pixel mode, value (M-19)/2 should be programmed into the HDSR. M must be odd in all cases. This is a 10-bit register, with bit 14 the least significant. Data bus encoding for this register is shown in Figure 13.

Horizontal Display End Register (HDER): Address 90H

This register defines the time, in units of two-pixel periods, from the start of the horizontal sync pulse to the end of the video display (i.e., the first pixel which is not displayed). The value programmed here depends on the screen mode used. If M pixels are required in this time, then: in 8-bits per pixel mode, value (M-5)/2 should be programmed into the HDSR; in 4-bits per pixel mode, value (M-7)/2 should be programmed into the HDSR; in 2-bits per pixel mode, value (M-11)/2 should be programmed into the HDSR; in 1-bit per pixel mode, value (M-19)/2 should be programmed into the HDSR. M must be odd in all cases. This is a 10-bit register, with bit 14 the least significant. Figure 14 shows data bus encoding of register values.

Horizontal Border End Register (HBER): Address 94H

This register defines the time, in units of two-pixel periods, from the start of –HSYC pulse to the end of the border display (i.e., the first pixel which is not border). If M pixels are required in this time, then value (M-1)/2 should be programmed into the HBER. [M must be odd.] Again, if no border is required, this register must still be programmed such that M[HBER] = M[HDER]. This is a 10-bit register, with bit 14 the least significant. Data bus encoding for this register is shown in Figure 15.

Horizontal Cursor Start Register (HCSR): Address 98H

This register defines the time, in units of single pixel periods, from the start of the –HSYC pulse to the start of the cursor display. If M pixels are required in this time, then value (M-6) should be programmed into the HCSR. This is normally an 11-bit register, with bit 13 the least significant. Bits 11 and 12 must be zero except in the High Resolution mode.

In this mode, where each 24 MHz pixel is further divided into four pixels, the cursor sub-position can be defined by programming bits 11 and 12 of the HCSR, which will move the cursor position within the 24 MHz pixel. Refer to the High Resolution Mode section.

Note that only the cursor start positon needs to be defined, as the cursor is automatically disabled after 32 pixels. If a cursor smaller than this is required, then the remaining bits in the cursor pattern should be programmed to logical color 00 (transparent). Figure 16 shows the data bus encoding scheme.

Horizontal Interlace Register (HIR): Address 9CH

This register must be programmed if an interlaced sync display is required. Otherwise, it may be ignored. If value L is written into the HCR, the value (L+1)/2 should be written into the HIR. [L is odd.] This is a 10-bit register with bit 14 the least significant. Data bus encoding is shown in Figure 17.

Vertical Cycle Register (VCR): Address A0H

This register defines the period, in units of a raster, of the vertical scan, i.e., display time + flyback time. If N rasters

FIGURE 17. HORIZONTAL INTERLACE REGISTER DATA BUS ENCODING

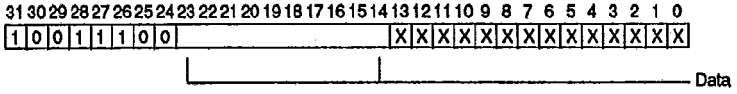


FIGURE 18. VERTICAL CYCLE REGISTER DATA BUS ENCODING

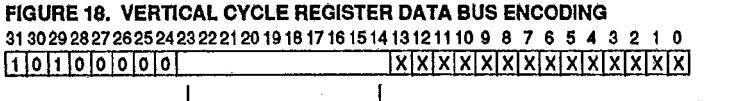


FIGURE 19. VERTICAL SYNC WIDTH REGISTER DATA BUS ENCODING

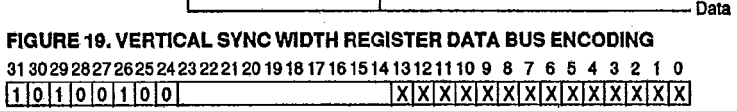


FIGURE 20. VERTICAL BORDER START REGISTER DATA BUS ENCODING

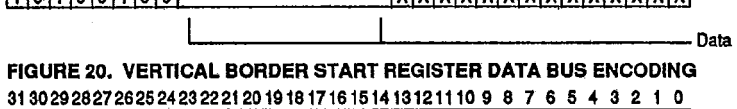


FIGURE 21. VERTICAL DISPLAY START REGISTER DATA BUS ENCODING

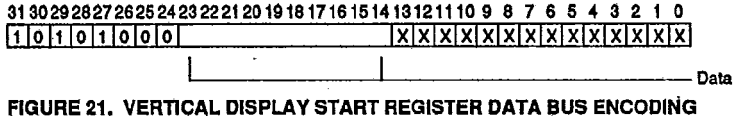


FIGURE 22. VERTICAL DISPLAY END REGISTER DATA BUS ENCODING

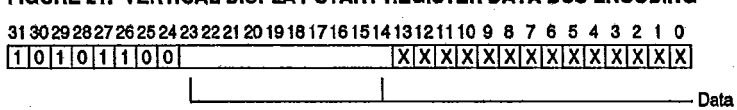
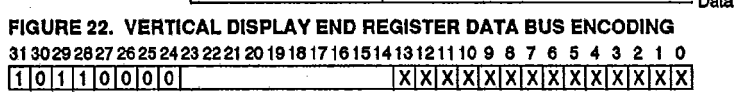


FIGURE 23. VERTICAL BORDER END REGISTER DATA BUS ENCODING



are required in a complete frame, then value (N-1) should be programmed into the VCR. If interlaced display is used, (N-3)/2 must be programmed into the VCR. [N is odd.] Here N is still the number of rasters in a complete frame, not a field. This is a 10-bit register, with bit 14 the least significant. Figure 18 shows the data bus encoding scheme.

Vertical Sync Width Register (VSWR): Address A4H
This register defines the width, in units of a raster, of the –V/CS pulse. If N rasters are required in the vertical sync pulse, then value (N-1) should be programmed into the VSWR. The minimum value allowed for N is 1. This is a 10-bit register, with bit 14 the least significant. Data bus encoding is shown in Figure 19.

Vertical Border Start Register (VBSR): Address A8H
This register defines the time, in units of a raster, from the start of the vertical sync pulse to the start of the border display. If N rasters are required in this time, then value (N-1) should be programmed into the VBSR. If no border is required, then this register must still be programmed, in this case to the same value as the VDSR. This is a 10-bit register, with bit 14 the least significant. Figure 20 shows the data bus encoding.

Vertical Display Start Register (VDSR): Address ACH
This register defines the time, in units of a raster, from the start of the vertical sync pulse to the start of the video display. If N rasters are required in this time, then value (N-1) should be programmed in the VDSR. This is a 10-bit register, with bit 14 the least significant. The data bus encoding is shown in Figure 21.

Vertical Display End Register (VDER): Address B0H
This register defines the time, in units of a raster, from the start of the vertical sync pulse to the end of the video display (i.e., the first raster on which the display is not present). If N rasters are required in this time, then the value (N-1) should be programmed into the VDER. This is a 10-bit register, with bit 14 the least significant. Figure 22 illustrates the data bus encoding.

Vertical Border End Register (VBER): Address B4H
This register defines the time, in units of a raster, from the start of the vertical sync pulse to the end of the border display (i.e., the first raster on which the border is not present). If N rasters are required in this time, then the value (N-1) should be programmed into the VBER. If no border is required, then this register must be programmed to the same value as the VDER. This is a 10-bit register, with bit 14 the least significant. Data bus encoding for this register is shown in Figure 23.

Vertical Cursor Start Register (VCSR): Address B8H
This register defines the time, in units of a raster, from the start of the vertical sync pulse to the start of the cursor display. If N rasters are required in this time, then value (N-1) should be programmed into the VCSR. This is a 10-bit register, with bit 14 being the least significant. Figure 24 shows the data bus encoding for this register.

Vertical Cursor End Register (VCER): Address BCH
This register defines the time, in units of a raster, from the start of the vertical sync pulse to the end of the cursor display (i.e., the first raster on which the cursor is not present). If N rasters are required in this time, then value (N-1) should be programmed into the VCER. This is a 10-bit register, with bit 14 the least significant. Data bus encoding is shown in Figure 25.

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FIGURE 24. VERTICAL CURSOR START REGISTER DATA BUS ENCODING

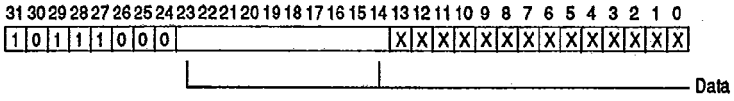


FIGURE 25. VERTICAL CURSOR END REGISTER DATA BUS ENCODING

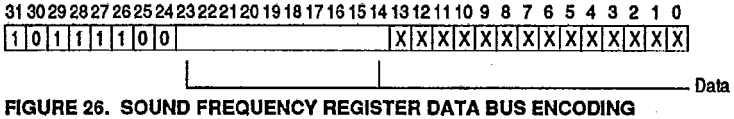
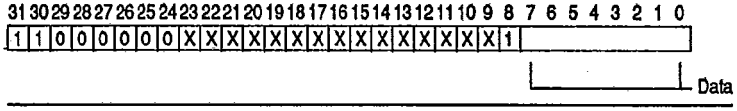


FIGURE 26. SOUND FREQUENCY REGISTER DATA BUS ENCODING



Sound Frequency Register (SFR): Address C0H

This register defines the byte sample rate of the sound data. It is defined in units of 1 µs. If a sample period of N µs is required, then (N-1) should be programmed into the SFR. N may take any value between three and 256. This is a 9-bit register with bit 0 the least significant. Bit 8 in the SFR is used as a test bit, and should always be set to one. When this bit is set to zero, all the internal timing signals are cleared. Figure 26 shows the data bus encoding.

Control Register (CR): Address E0H

This register contains the operating mode controls: a total of 11 bits are defined, and three of these are for test purposes only. Note that bit 8 in the SFR must also be set before the device can operate correctly.

The two bit-pairs for the pixel rate and the bits per pixel selects are defined in Figure 27. The bit-pair to define the point at which the DMA request flag is set is further explained in the Restriction On Parameters section.

To select interlaced sync displays, D[6] in this register must be set as well as setting the correct values in the vertical and horizontal timing registers.

The –V/CS pin on the device can be programmed to output either the vertical sync pulse or the composite sync pulse which is the XNOR of vertical and horizontal sync. Selection is made by D[7].

The remaining 3-bits are for testing the device and are of little interest to the user, but their action is as follows.

In test mode zero (D[14] high, D[15] low), the upper 5-bits of the horizontal counter are clocked by a derivative of the pixel clock.

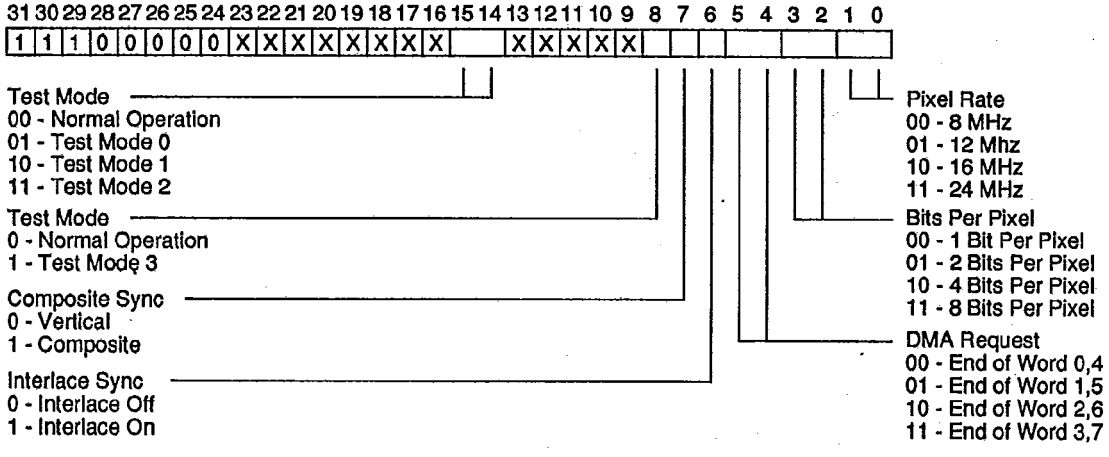
In test mode one (D[14] low, D[15] high) the lower 5-bits of the vertical counter are clocked by a derivative of the pixel clock.

In test mode two (D[14] high, D[15] high), the upper 5-bits of the vertical counter are clocked by a derivative of the pixel clock.

In test mode three (D[8] set), the pin –L/R outputs a signal which is eight times the frequency of the sound byte sampling clock, and the pins SD3-SD0 output the inverse of the data which is fed to the green DAC [NSEL low] or the blue DAC [NSEL high].

Note that the device cannot function properly in test modes zero, one, and two, but test mode three has no effect on the normal operation.

FIGURE 27. CONTROL REGISTER DATA BUS ENCODING



USING THE VIDC

The DMA Interface

The VIDC has three FIFOs into which DMA data is written. The sound FIFO is four 32-bit words deep, and works independently from the the other two FIFOs. The video FIFO is eight 32-bit words deep, and the cursor FIFO is again four 32-bit words deep.

Sound FIFO

Each word of data is strobed into the FIFO on the rising edge of –SDAK. Data is read out of the FIFO into a byte wide latch which then drives the DAC. When the last byte in the FIFO is read into the latch, the signal –SDRQ is driven low, requesting another 16 bytes of data. The signal –SDRQ is driven high when the first –SDAK is received.

The time available to service this data request is dependent on the sound data rate. The minimum value of the SFR is three, which defines a byte-rate of 3 µs. Therefore, the first word must be loaded into the FIFO less than 3 µs after the –SDRQ signal is generated.

Cursor FIFO

The cursor FIFO contains 16 bytes of data, which is enough for two rasters of cursor display. When the VIDC is programmed to display a cursor, –VDRQ is driven low at the same time as –HSYC goes low on the first raster on which the cursor is to appear. Data is loaded into the FIFO on the rising edge of –VDAK. The load cycle must be complete before the –HSYC pulse has ended.

–VDRQ is driven high again when the first –VDAK is received. The cursor may be any number of rasters high, and the cursor FIFO requests data during the –HSYC of every alternate raster on which it is displayed.

Video FIFO

The video FIFO is eight 32-bit words deep, and it is arranged as a circluar buffer. Data must always be loaded into it in blocks of four words, and this FIFO shares the same –VDRQ and –VDAK signals as the cursor FIFO.

To accommodate the vastly different rates at which video data is required in the different modes, and to accommodate different DRAM speeds, the point at which more data is requested can be varied. This is done by bits 4 and 5 in the Control Register.

During the vertical sync pulse, the FIFO is cleared, and the signal –VDRQ is high. After the –HSYC pulse of the first displayed raster, –VDRQ is driven low. Eight words must now be written into the FIFO by driving –VDAK low eight times. This fills the FIFO. –VDRQ is set high again when the fifth –VDAK is received.

Thereafter, the –VDRQ signal is set low whenever the FIFO empties to the point predetermined by bits 4 and 5 in the Control Register. The –VDRQ signal is normally set high when the first –VDAK signal is received. However, if the data request is not serviced quickly, and the FIFO has emptied to the point where another four words have been read out when the first new data word arrives, then the –VDRQ signal will stay low, requesting another four words of data.

The Video DMA Interface

As noted above, the cursor and video FIFOs share the same DMA interface signals. Normally, a –VDRQ low during the –HSYC pulse is a request for cursor data, and –VDRQ low at any other times is a request for video data. Figure 28 shows the relationships graphically.

However, often a video request happens just before the end of a raster requesting data for the next raster. The load cycle for this video request is allowed to overlap the –HSYC pulse, even if a cursor request happens during the –HSYC pulse. Note that in this case the –VDRQ signal may not be driven high between these two cycles. The first cycle must be video data and the second cycle must be cursor data. The cursor load cycle must still be complete before the end of the –HSYC pulse. This is shown in Figure 29.

Figure 30 shows the situation where a cursor is displayed on the first raster of the frame. Note the double video load cycle. The cursor load cycle must not overlap the end of the –HSYC pulse (otherwise data will be loaded into the wrong FIFO), and the first word of video data must be present in the FIFO before the display starts.

Restrictions On Parameters

It is clear from the above that certain restrictions must be applied to the screen parameters, most of which are system dependent. The following paragraphs assume the VIDC is being used in a system with the processor and MEMC and two/one clock page-mode DRAM memory. In this system DRAM cycles consist of an N-cycle (two RCLK clocks) followed by up to three sequential S-cycles (one RCLK clock).

5

FIGURE 28. VIDEO AND CURSOR DMA OPERATION

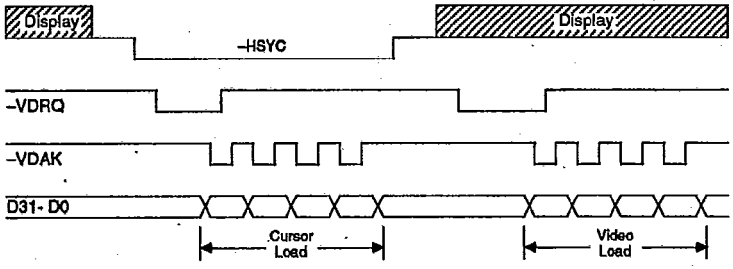


FIGURE 29. VIDEO DMA OVERLAPPING –HSYC PULSE

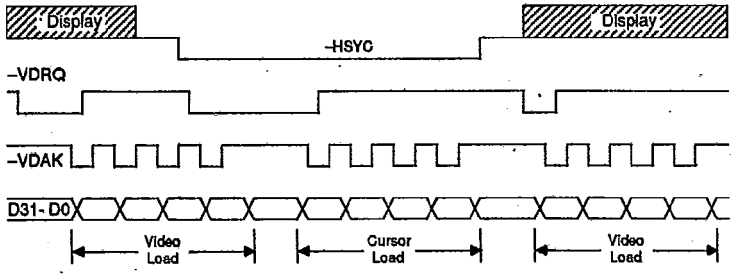
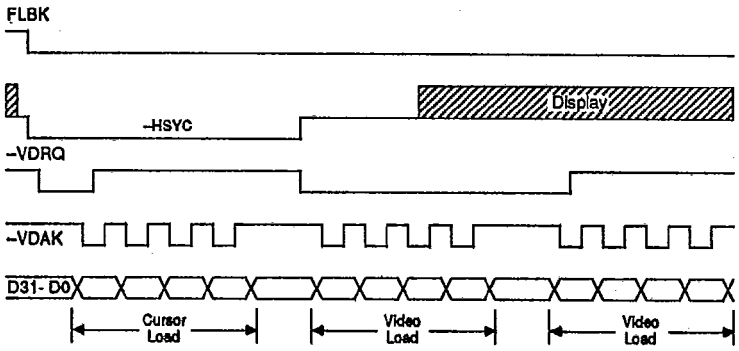


FIGURE 30. CURSOR DMA AT THE BEGINNING OF A FRAME



Hence, a VIDC FIFO load cycle consists of 1N + 3S requiring five RCLK clocks (417 ns at 12 MHz).

FIFO Request Pointer Values (Control Register Bits [4:5])

The video FIFO is a circular buffer, although the core is asynchronous, with a ripple-through time of 150 ns from the top to the bottom. Data is loaded in blocks of four words, and is read out in bytes, starting with byte 0 of word zero and so on. –VDRQ can be set low half way through reading the last byte of any of word 0-3 (and correspondingly 7-4) according to bits 5-4 in the Control Register. In the high resolution video modes where the bytes are being consumed quickly, the request signal must be set at an earlier point than in the low resolution modes. Selections are defined in Table 3.

The request signal –VDRQ should be brought low as soon as the FIFO can accept the four words of data when they arrive. The minimum time between setting the request and receiving the last word of data is 187 ns + 625 ns = 812 ns (at 8 MHz). [The 187 ns figure is the minimum time in which MEMC can start a DMA cycle.] If the FIFO is full at the start, then it will have four words spare 150 ns after the start of word 4. [150 ns is the ripple-through time of the FIFO.] Hence, the request should be made at the first opportunity after (812 ns - 150 ns = 652 ns) before the start of word four. The request can be made halfway through the last byte of any of words 0-3 by programming the Control Register.

TABLE 3. FIFO POINTER SETTINGS

Control Register		–VDRQ Set At End Of Words
Bit 5	Bit 4	
0	0	0, 4
0	1	1, 5
1	0	2, 6
1	1	3, 7

Depending on the video mode in use, data can be read from the FIFO at 1.5, 2, 3, 4, 6, 8, 12, or 16 Mbytes/second.

Figure 31 shows the case for the 16 Mbytes/second mode. The request must be set at the end of words one and five.

Figure 32 shows the case for the 12 Mbytes/second mode. The request must be set at the end of words two and six.

Figure 33 shows 8 Mbytes per second mode. Again, the request must be set at the end of words two and six.

In all other modes, the request should be set at the end of words three and seven.

Horizontal Sync Pulse Width

The –HSYC pulse width must be long enough to allow a complete load of the cursor FIFO. This is made up as follows:

2*[N+3S] (current + cursor cycles) + syncmax + 2*Tprop.

i.e. 2*625 + 312+ 100 = 1662 ns.

FIGURE 31. FIFO OPERATING AT 16 MBYTES PER SECOND

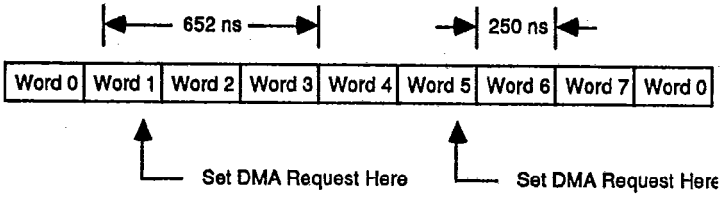


FIGURE 32. FIFO OPERATING AT 12 MBYTES PER SECOND

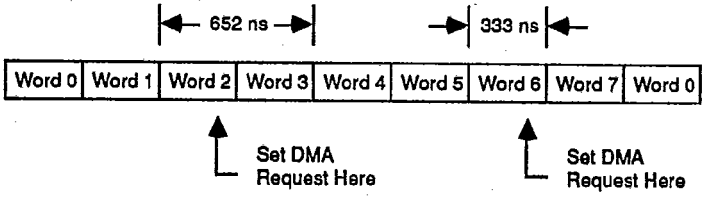
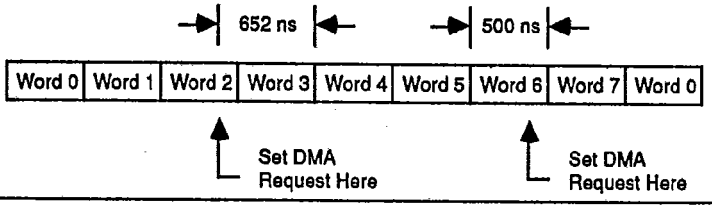


FIGURE 33. FIFO OPERATING AT 8 MBYTES PER SECOND



Syncmax is the maximum time MEMC can take to recognize the DMA request. Tprop is the time taken for the –VDRQ signal to reach MEMC, or the time taken for –VDAK to reach VIDC.

The pulse must also be long enough to allow the processor to write to the DMA address generator (DAG) in the MEMC to reset the screen pointer. This may be as follows:

3*[N+3S] (current + cursor + sound cycles) + DAG write.

i.e. 3*625 + 250 = 2125 ns. Since both these parameters must be met, this larger value must therefore be used.

Horizontal Front Porch Width
The front porch may be zero length. The total time from the end of display to the end of the –HSYC pulse must be more than 1912 ns. As the –HSYC pulse width has to be at least 2125 ns, this does not impose a restriction on the value of the back porch.

Horizontal Front Porch Width
The back porch must be long enough to allow the load of at least one word into the video FIFO before the data is read out again. This is important at the start of the frame because data is required in the bottom of the FIFO at least four pixel-times before the start of display, due to the pipeline delays. Hence the back porch must be greater than:

N+3S+N (current cycle + video N cycle) + syncmax + 2*Tprop + FIFO-ripple + 4 pixels.

i.e. 250 + 375 + 250 + 312 + 100 + 150 + 4*83 = 1769 ns for 12 MHz displays.

or 250 + 375 + 250 + 312 + 100 + 150 + 4*125 = 1937 ns for 8 MHz displays.

Vertical Sync Pulse and Porch Width
There are no restricitons on the values of the vertical front porch, back porch, or sync width. The Vertical Sync Width Register (VSWR) may be programmed to a value of 0 which gives a vertical sync width of one raster.

Horizontal Display Width
The number of bits in the pixels of each raster must be a multiple of 128.

Border
The border cannot be disabled. If no border is required, then it should be programmed to start and finish in exactly the same place as the display (both vertically and horizontally).

Cursor Position
The cursor should not be programmed to be outside the display area vertically, but it may be programmed to start or end outside the display area horizontally. Note that the cursor will not be displayed outside the border area either vertically or horizontally.

TABLE 4. SCREEN MODE SUPPORT

Pixel Rate	Bits/Pixel	FIFO Data Rate	Pixel Rate	Bits/Pixel	FIFO Data Rate
24 MHz	8	Not Supported	12 MHz	8	12 Mbytes / Second
	4	12 Mbytes / Second		4	6 Mbytes / Second
	2	6 Mbytes / Second		2	3 Mbytes / Second
	1	3 Mbytes / Second		1	1.5 Mbytes / Second
16 MHz	8	16 Mbytes / Second	8 MHz	8	8 Mbytes / Second
	4	8 Mbytes / Second		4	4 Mbytes / Second
	2	4 M ytes / Second		2	2 Mbytes / Second
	1	2 Mbytes / Second		1	Not Supported

DISPLAY FORMATS

Screen Modes
Fourteen of the possible 16 display modes are supported (See Table 4).

Data Display
Pixels are displayed starting at the top left hand corner of the screen, with the least significant end of the first word loaded into the FIFO. In 8-bits per pixel mode, bits 0-7 of word zero are the first displayed pixel. In 4-bits per pixel mode, bits 0-3 of word zero are the first displayed pixel. In 2-bits per pixel mode, bits 0-1 of word zero are the first displayed pixel. In 1-bit per pixel mode, bit zero of word zero is the first displayed pixel.

Logical Data Fields
In 1-bit per pixel mode, the data field selects the palette at location zero or one. The other 14 locations need not be programmed. In 2-bits per pixel mode, the data field addresses the palette at locations zero through three. The other 12 locations need not be programmed. In 4-bits/pixel mode, the data field addresses the palette at all 16 locations. In 8-bits per pixel mode, the least significant 4-bits drive the palete as in 4-bits per pixel mode, and the most significant four bits drive the most significant bits of the RGB DACs directly.

Physical Data Fields
In 1-, 2-, and 4- bits per pixel mode, the physical data field is shown in Figure 34. In 8-bits per pixel mode, the physical data field is shown in Figure 35. The Dn bits come from the palette field and the Ln bits come from the logical field.

Cursor Format
The cursor, in all video modes, is defined to be 32 pixels wide and any number of rasters high. Any pixel may be defined as being transparent, enabling cursors of any shape to be constructed within the 32 pixel horizontal limit. It is always 2-bits per pixel, with bits zero, one in the first word to be loaded into the cursor FIFO representing the first pixel, etc. The logical cursor pixel bit-pairs are defined in Table 5.

The cursor physical field is exactly as the video physical field in 1-, 2-, or 4- bits per pixel modes.

FIGURE 34. PHYSICAL COLOR FIELD DEFINITIONS

12	11	10	9	8	7	6	5	4	3	2	1	0
SUP	BLUE				GREEN				RED			
D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

FIGURE 35. PHYSICAL COLOR FIELD DEFINITIONS FOR 8 BITS PER PIXEL

12	11	10	9	8	7	6	5	4	3	2	1	0
SUP	BLUE				GREEN				RED			
D12	L7	D10	D9	D8	L6	L5	D5	D4	L4	D2	D1	D0

TABLE 5. CURSOR LOGICAL COLORS

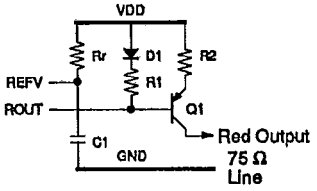
Cursor Bit		
MSB	LSB	Color
0	0	Transparent
0	1	Logical Color 1
1	0	Logical Color 2
1	1	Logical Color 3

Border Field
The border physical field is exactly as the video physical field in 1-, 2-, and 4-bits per pixel modes.

Controlling the Screen On / Off
The simplest method of turning the screen off is to program the Vertical Display End Register (VDER) to be less than the VDSR. This will not generate any video requests, but will display the border color over the whole screen. The border can be turned off either by programming it to physical color black, or by programming the VBSR to be greater than the VBER. Doing the latter will also disable the cursor, though cursor data requests will still be generated. Turning the screen back on should only be done during vertical flyback.

Cursor On / Off
The cursor should be turned off by setting the VCER to be less than VCSR. [Value 0 is suggested.] This will also disable cursor data requests. Turning the cursor on, and moving it around should only be done during vertical flyback to prevent flash.

FIGURE 36. EXAMPLE VIDEO OUTPUT CIRCUIT



Suggested Component Values
Rr – 10 kΩ
R1 – 330 Ω
R2 – 68 Ω
D1 should have similar characteristics to the emitter-base junction of Q1

Writing to the Palettes and Other Registers
The palettes may be programmed reliably at any time, but are best programmed during vertical flyback. Changing the values of other registers should only be done during vertical flyback. The signal FLBK is set high from the start of the first raster after the end of display (though it may still be border), until the start of the first raster which is display.

Video DAC Outputs
The video DAC outputs are in the form of current sinks. Each DAC has a resolution of 4-bits, giving a linear transfer characteristic with 16 values.

A digital input value of four zeros gives zero current sink, and a digital input value of four ones gives the maximum current sink. The magnitude of the output is a function of the video reference input current, with the maximum current sink being 15 times the reference input current.

High Resolution Modes
The four bits of digital data which normally drive the red DAC are available to the user on pins –VED3 through –VED0. This pixel rate bit-stream can be externally serialized to a single bit-stream of four times the VIDC pixel rate. With the VIDC operating at 24 MHz, four bits per pixel mode, 96 MHz bit rates are generated giving very high resolution monochrome displays. Alternatively, with an external DAC, 48 MHz grey-level displays are possible.

Refering to the block diagram, it will be noted that the data passes through the High Res. Shifter block before reaching the pins –VED3 - –VED0. This block enables the cursor to be positioned to any (96 MHz) pixel. Note that this block also inverts the data from the red DAC.

When used in this mode, the VIDC must be programmed to a different set of values. But note that the "normal" analog modes of VIDC are still available simply by reprogramming: the addition of the shifter hardware will not affect the other modes, and the sound system is totally independent from this.

(1) Four-bits per pixel should always be selected.

(2) The programmed VIDC pixel rate is one quarter of the external pixel rate. The vertical timing parameters are unaffected by this as they are defined in units of a raster, but the horizontal timing parameters which are defined in units of two (24 MHz) pixels can only be programmed in units of eight (96 MHz) pixels. There are now four times as many pixels on a line as are actually programmed. For example, if a display of 1024 * 1024 is required, the VIDC should be programmed to generate a display of 256 (horizontal) by 1024 (vertical).

(3) All 16 locations of the video palette should be programmed to a 1:1 logical to physical mapping. Only D[0:3] (red DAC values) need to be programmed, as D[4:11] are ignored. The supremacy bit (D[12]) may be used if required.

(4) D[4,5] in the Border Color Register must be set to zero. D[0:3] and D[12] may also be programmed if a border is required.

(5) The cursor palette should be programmed to the following values:
cursor color 1 : 10H
cursor color 2 : 20H
cursor color 3 : 30H
Supremacy may also be used.

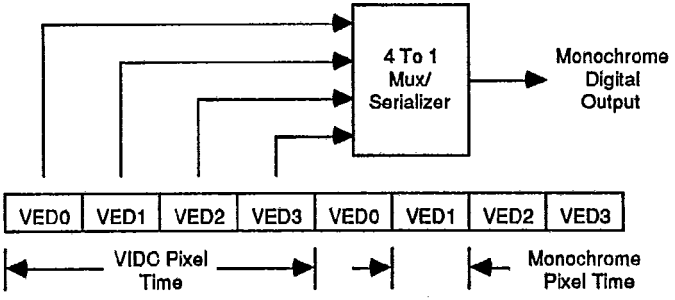
Then the 2-bits which define each cursor pixel are defined in Table 6.

Note that the cursor can only be defined horizontally in units of four (96 MHz) pixels, though it can be positioned anywhere on the screen to within one (96 MHz) pixel. See the section on Horizontal Cursor Start Register for more detail. The hardware should be arranged so that –VED0 is the first bit to be serialized.

TABLE 6. CURSOR COLOR IN HIGH-RESOLUTION MODE

Cursor Bits		
MSB	LSB	Definition
0	0	Transparent
0	1	Cursor Black
1	0	Do Not Use
1	1	Cursor White

FIGURE 37. HIGH RESOLUTION PIXEL GENERATOR



External Synchronization and Mixing
The VIDC has two signals associated with external synchronization applications: SUP and SINK. SUP is an output which can be used to control an external multiplexer for mixing the VIDC output with that from an external source. All video and cursor logical colors from the palettes and the border color can control SUP. When D[12] in any of the above registers is set and that color is being displayed, SUP is driven low. The output is pipelined and is synchronous with the DAC outputs and the –VED3 - –VED0 signals.

The signal SINK is an input which when driven high resets the vertical counters to the first raster. If an interlaced sync display is being generated, then SINK will reset the counters to the first raster of the odd field. The pulse applied to this pin must be shorter than a raster time. The horizontal counters are not affected by this signal. The horizontal synchronization must be done by phase-locking (or in simple applications, by interrupting) the input clock CKIN. Remember that the sound system is also driven from a derivative of CKIN.

Composite Sync
According to the setting of D[7] in the Control Register, the –V/CS can output a composite sync pulse. This is synthesized from the XNOR of vertical and horizontal syncs as shown in Figure 38.

Interlaced Displays
The VIDC can generate an interlaced sync display. An example of interlace timing is shown in Figure 39. Normally the video data in each field is the same. The VIDC Vertical Cycle Register is set to a value (N-3)/2, where N is the total number of rasters in a frame. There are N/2 raster in the even and odd fields. On raster (N+1)/2, the vertical sync pulse is output and the cycle repeats, but this is now the odd field, so the vertical sync pulse is delayed by half a raster time as defined by the value in the HIR. On the first raster in the odd field which is not vertical sync, a dummy raster is inserted. This makes the odd field N/2 rasters long as well.

FIGURE 38. COMPOSITE SYNC GENERATION

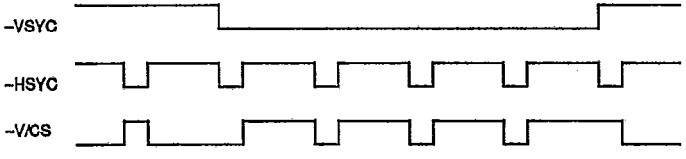


FIGURE 39. INTERLACE DISPLAY TIMING GENERATION

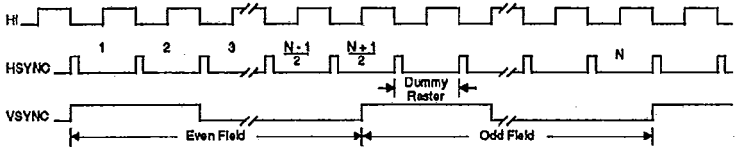
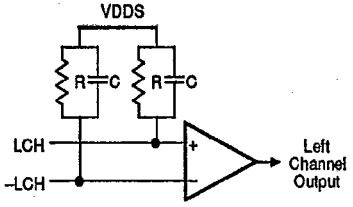


FIGURE 40. SOUND OUTPUT CIRCUIT



Sound System
The sound system consists of a four word FIFO and byte wide latch which drive a 7-bit exponential DAC. The eighth bit steers the DAC output to one of two pairs of output pins, one pair designated "+", and the other pair designated "-". The sound signal is generated externally by integrating and then subtracting these two pairs of signals. An example circuit is shown in Figure 40. The integration is performed by the capacitor C.

Stereo image is synthesized by time-division multiplexing the output between the "left" and "right" pair of output signals as shown in Figure 41. The first quarter of each sample is muted to allow for DAC settling and deglitching. The stereo image is specified for each channel by programming the corresponding Stereo Image Register.

The system can operate in 1, 2, 4, or 8 channel modes. In 8 channel mode, the channels are sampled sequentially, starting with the first byte of data, which is channel 0; the second byte of data is channel 1 and so on. The external integrating time constant must be long enough to integrate over a complete sample cycle. In 4 channel mode, the fifth byte to be sampled is again channel 0, so Stereo Image Register 4 must be programmed to the same value as Stereo Image Register 0, and so on. In 2 channel mode, Stereo Image Registers 0, 2, 4, and 6 correspond to channel 0 and Stereo Image Registers 1, 3, 5, and 7 correspond to channel 1. In single channel mode, all eight Stereo Image Registers should contain the same value.

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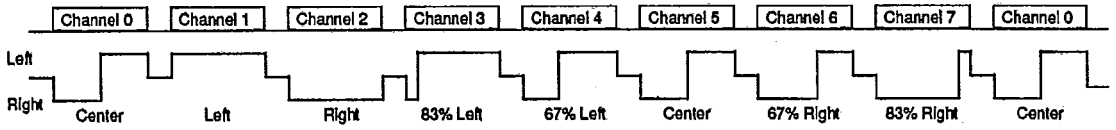
FIGURE 41. STEREO IMAGE SYNTHESIS



The sample rate is selectable by the SFR in units of 1 µs, with a minimum value of 3 µs. Clearly, in eight channel mode the bytes for each channel are sampled with one-eighth of the frequency of single channel mode for a given value in the SFR.

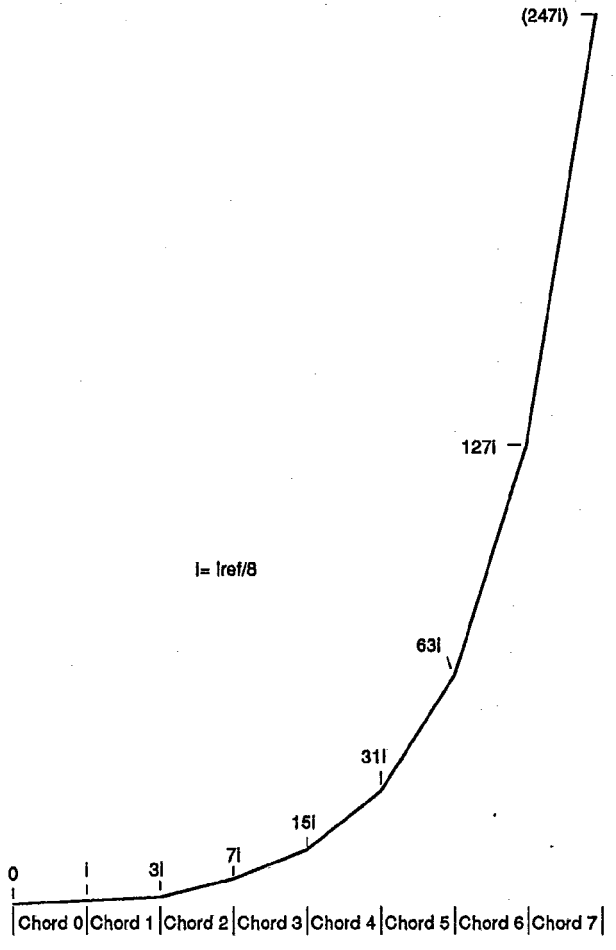
The DAC transfer characteristic consists of eight linear segments (chords). Each chord consists of 16 steps, and the step size in one chord is twice the step in the preceding chord. This gives an approximation to the "µ255 law." The sound data field format is shown in Figure 42.

The outputs are in the form of current sinks. The magnitude of the output is a function of the sound reference input current. The reference current is equal to the step size in the highest chord, which is 8i in Figure 43.

FIGURE 42. SOUND DATA FIELD FORMAT

D7	D6	D5	D4	D3	D2	D1	D0
Chord Select			Point On Chord				Sign

FIGURE 43. SOUND DAC OUTPUT



TIMING CHARACTERISTICS: TA = 0°C to +70°C, VDD = +5 V ±5%

Symbol	Parameter		Min	Typ	Max	Units	Conditions
t1	CKIN High		10	–	–	ns	
t2	CKIN Low		13	–	–	ns	
t3	CKIN Frequency		–	–	33	MHz	
t4	Data Setup Time to –VDAK, –SDAK		9	–	–	ns	
t5	Data Hold Time to –VDAK, –SDAK		9	–	–	ns	
t6	–VDAK, –SDAK Pulse Width		15	–	–	ns	
t7	Data Setup Time to –VIDW		10	–	–	ns	See Note 1
t8	Data Hold Time to –VIDW		20	–	–	ns	
t9	–VIDW Pulse Width		20	–	–	ns	
t10	CKIN to –SD3 - –SD0 Delay		–	70	–	ns	See Notes 2, 3
t11	CKIN to –VED3 - –VED0, –SUP Delay		–	70	–	ns	See Note 2
t12	CKIN to –HSYC, –V/CS, FLBK		–	75	–	ns	
t13	CKIN to –HI Delay		–	75	–	ns	
t14	CKIN to ROUT, GOUT, BOUT		–	30	–	ns	See Note 2
t15	Analog Output Rise/Fall Time		–	10	–	ns	See Note 4
t16	NIBSEL to –SD3 - –SD0		–	50	–	ns	
t17	Acknowledge To Request Delay	–SDAK to –SDRQ	–	50	–	ns	See Note 5
		–VDAK to –VDRQ	–	50	–	ns	See Note 5

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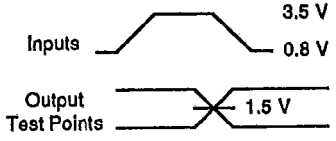
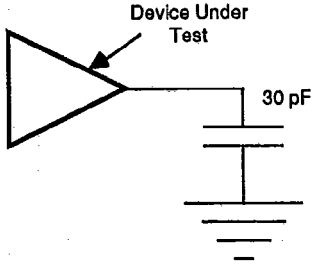
A.C. TEST WAVEFORMS



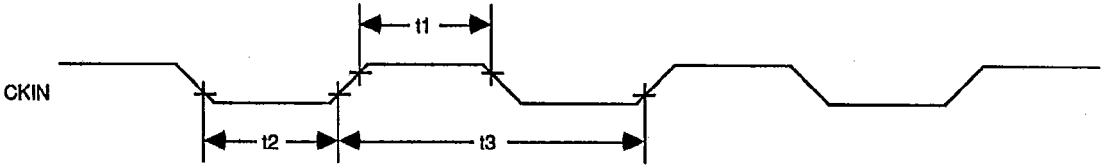
A.C. TEST LOAD CIRCUIT



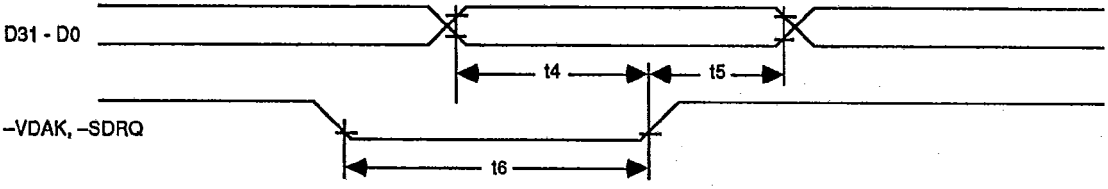
Notes:
1. The data must be setup before –VIDW goes active (low) because the data also contains the register address.
2. For pixel rates of 12 and 24 MHz, the outputs are referenced to the rising edge of CKIN. For pixel rates of 8 and 16MHz, the outputs are alternately referenced to either edge of CKIN.
3. The –SD3 - –SD0 signals are output one pixel time before the corresponding –VED3 - –VED0 due to pipeline differences.
4. Assumes a 5 pF external load.
5. –VDRQ or –SDRQ are cleared by the first –VDAK or –SDAK respectively, as long as no request is pending.

TIMING DIAGRAMS

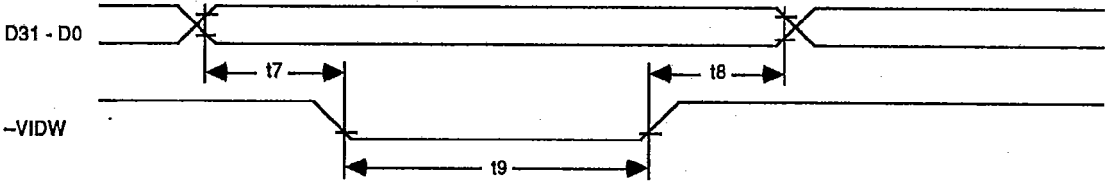
INPUT CLOCK



DMA WRITE CYCLES

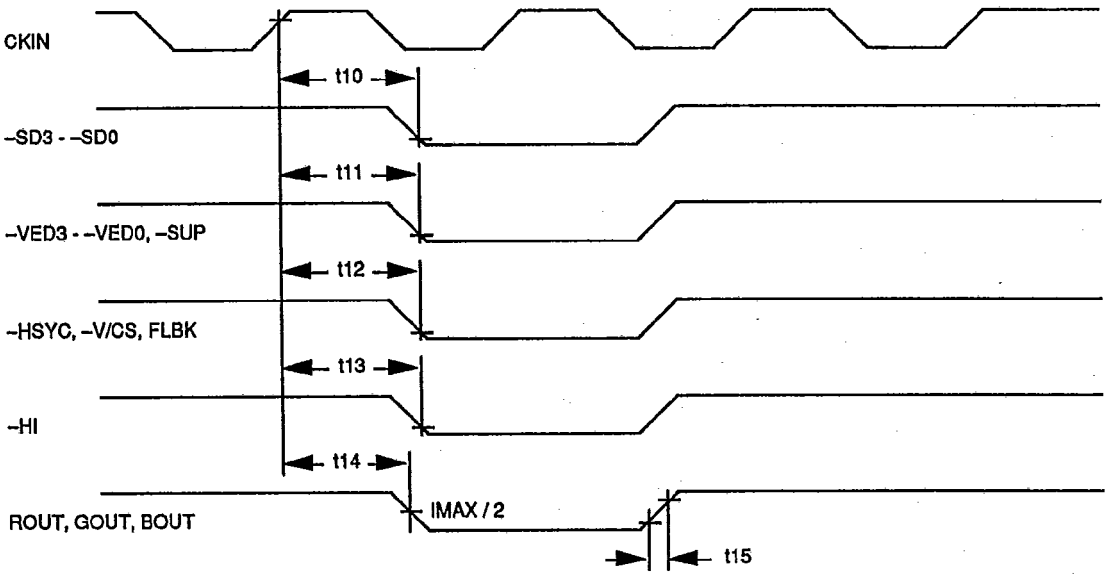


DMA WRITE CYCLES

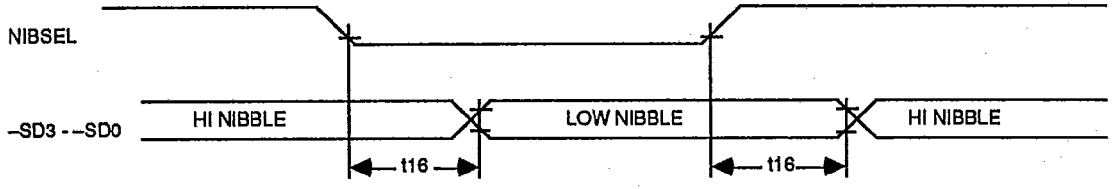


TIMING DIAGRAMS

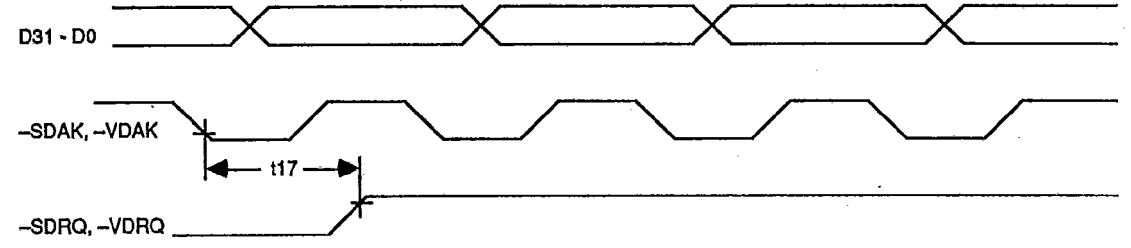
CLOCK OUTPUTS



NIBSEL TIMING



DMA ACKNOWLEDGE CYCLE



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ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	−10°C to +80°C
Storage Temperature	−65°C to +150°C
Supply Voltage to Ground Potential	−0.5 V to VDD +0.3 V
Applied Output Voltage	−0.5 V to VDD +0.3 V
Applied Input Voltage	−0.5 V to +7.0 V
Power Dissipation	2.0 W

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

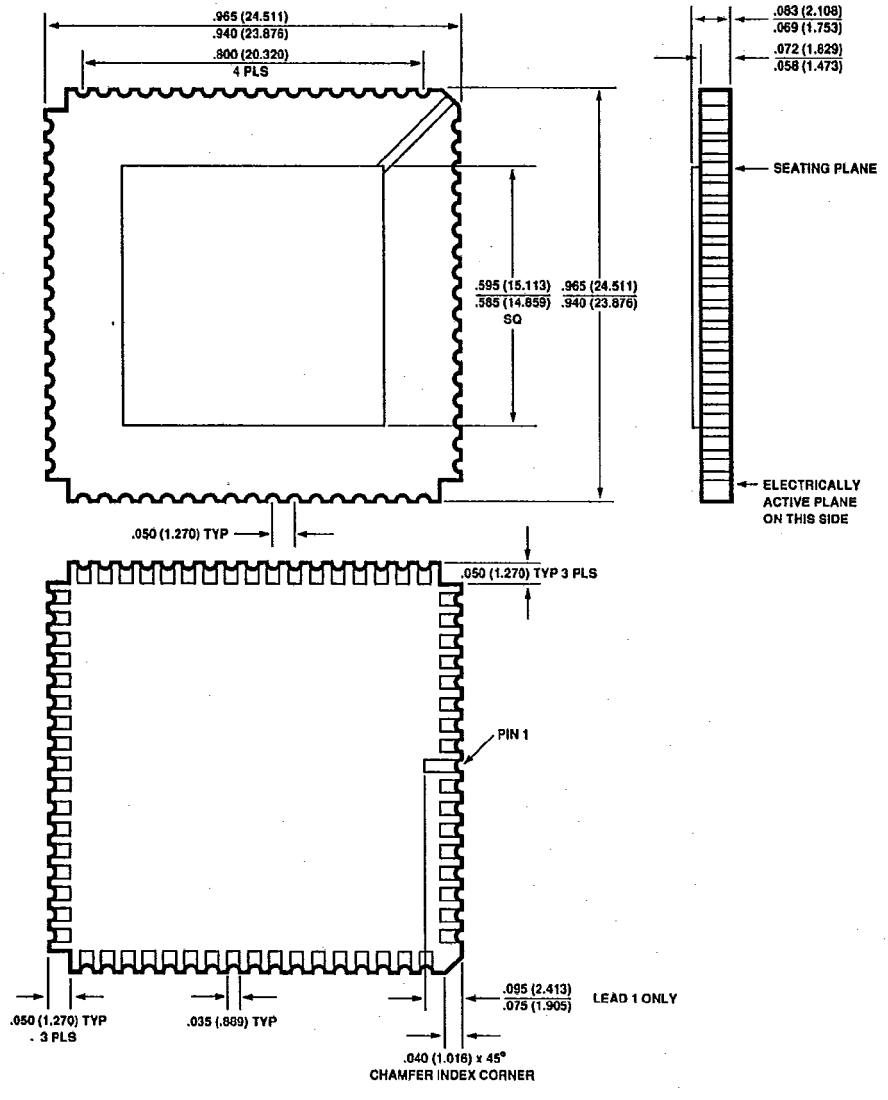
D.C. CHARACTERISTICS: TA = 0°C to +70°C, VDD = +5 V ±5%

Symbol	Parameter		Min	Typ	Max	Units	Conditions
VOH	Output High Voltage		VDD - 0.75	–	VDD	V	IOH = 10.0 mA
VOL	Output Low Voltage		–	–	0.4	V	IOL = - 3.0 mA
VIH	Input High Voltage		2.4	–	–	V	
VIHV	Input High, VIDW		3.5	–	–	V	
VIL	Input Low Voltage		0.0	–	0.8	V	
ILI	Input Leakage Current		–	–	10	µA	VIN = 0 V - VDD
ILO	Output Leakage Current		–	–	10	µA	VOUT= 0 V - VDD
ICC	Operating Supply Current		–	–	20	mA	See Note 1
IOS	Output Short Circuit Current		–	25	–	mA	See Note 2
IVOUT	Output Current Video DACs		–	–	−2.0	mA	
ISOUT	Output Current Sound DAC		–	–	−2.0	mA	
ADVOL	RVDAC, RSDAC Voltage		–	VDD - 1.3	–	V	See Note 3
ILATCH	Input/Output Latchup Current		200	–	–	mA	See Note 4
VCOMP	Voltage Compliance	Video DACs	–	VDD - 1.7	–	V	IVOUT = −2.0 mA
		Sound DAC	–	VDD - 1.5	–	V	ISOUT = −2.0 mA
CCOMP	Current Compliance	Video DACs	–	4.5	–	mA	VOUT = VDD - 0.7
		Sound DAC	–	3	–	mA	VOUT = VDD - 0.7

Notes:
1. Measured at 24 MHz pixel rate. This value does not include any current output by the video DACs.
2. Not more than one output should be shorted to either rail and for no longer than one second.
3. This assumes 10 kΩ resistors to VDD.
4. This value is the current that inputs or outputs can tolerate before the chip latches up. This condition should be avoided to prevent device damage.

PACKAGE OUTLINES

68-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



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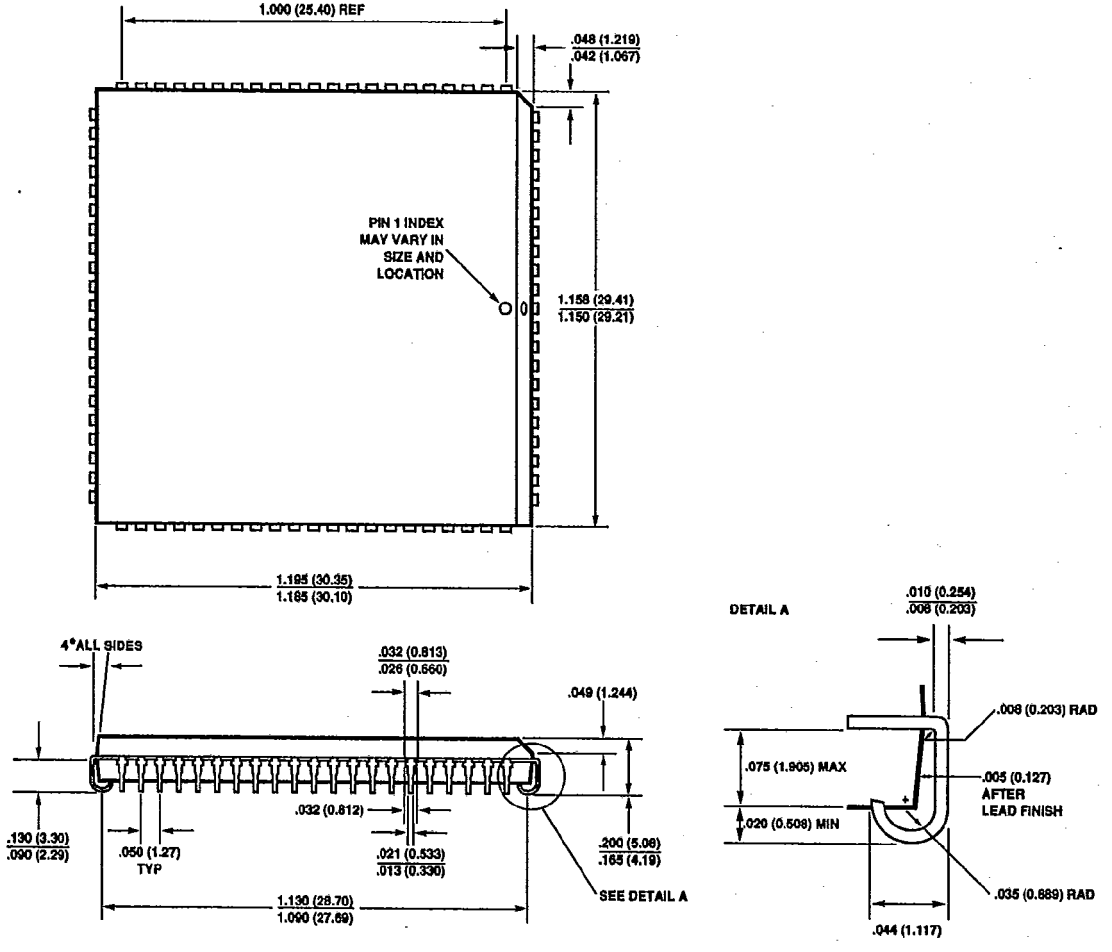
PACKAGE OUTLINES (Cont.)
84-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



NOTES: UNLESS OTHERWISE SPECIFIED.
1. TOLERANCE TO BE +/- .005 (0.127).
2. LEADFRAME MATERIAL: COPPER.
3. LEAD FINISH: MATTE TIN PLATE OR SOLDER DIP.
4. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG FULL LENGTH OF LEAD.
5. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS .010 (0.254) MAX ON FOUR SIDES.
6. CONTROLLING DIMENSIONS ARE METRIC, ALL METRIC DIMENSIONS ARE IN PARENTHESES.

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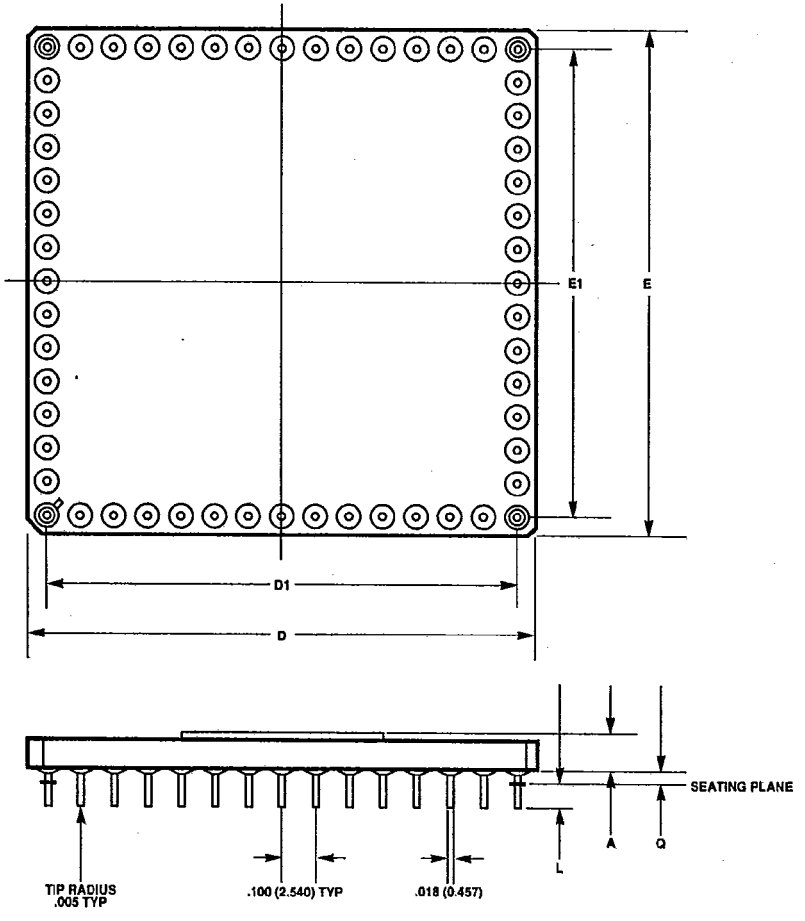
PACKAGE OUTLINES (Cont.)

144-PIN CERAMIC PIN GRID ARRAY



Pin Count	Matrix	Cavity Position	A		D (E)		D1 (E1)		Q	L
			Min	Max	Min	Max	Min	Max	Ref	Ref
144	15 x 15	Up	.0780 (1.981)	.1020 (2.591)	1.559 (39.60)	1.591 (40.41)	1.388 (35.26)	1.412 (35.86)	0.050 (1.270)	0.130 (3.302)

Notes: 1. All dimensions are in inches (mm).
2. Material: Al203
3. Lead Material: Kovar
4. Lead Finish: Gold plating 60 micro-inches min. thickness over 100 micro-inches nominal thickness of nickel

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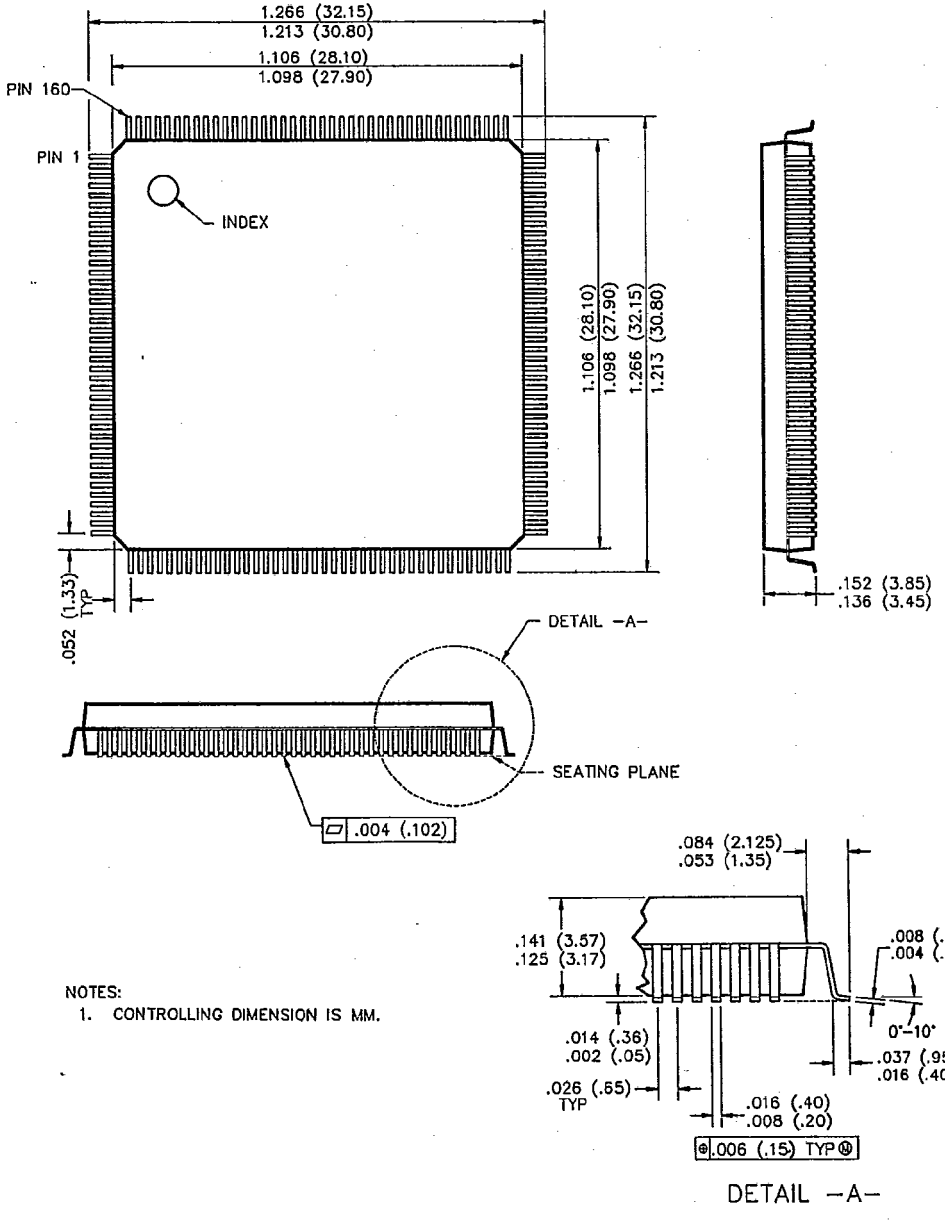
PACKAGE OUTLINES (Cont.)

160-PIN CERAMIC PIN GRID ARRAY



NOTES:

1. CONTROLLING DIMENSION IS MM.