VL82C59A

PROGRAMMABLE INTERRUPT CONTROLLER

FEATURES

- Compatible with 8086, 8088, and similar microprocessors
- Low power consuming CMOS
- Interrupt modes are programmable
- Minimizes software overhead
- Eight prioritized control levels
- 64 levels of expandability
- Single 5 V power supply
- 28-pin DIP Package

DESCRIPTION

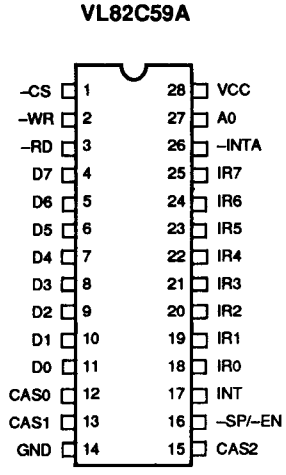
The VL82C59A Programmable Interrupt Controller can manage up to eight vectored priority interrupts for the system's CPU. It can be cascaded to handle up to 64 interrupts. No additional circuitry is required.

The VL82C59A has been designed to relieve the software of the burden of handling multi-level priority interrupts. It controls several modes, permitting optimization for a large number of system needs.

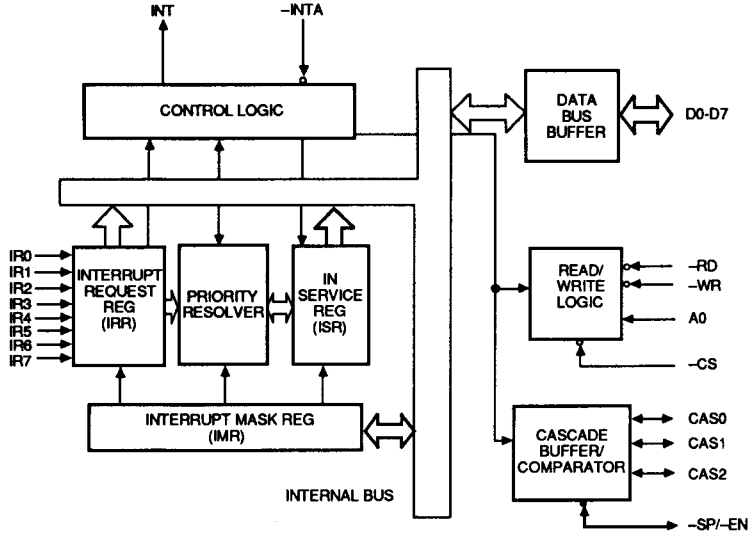
The VL82C59A is fully upward compatible with the HMOS 8259 or 8259A. Software originally written for the HMOS 8259 or 8259A will operate the VL82C59A in all 8259 or 8259A equivalent modes.

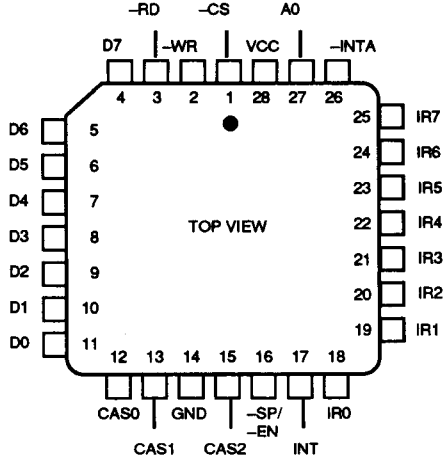
The VL82C59A is housed in a 28-pin DIP, uses CMOS technology and requires a single 5 V supply. The circuit is totally static, requiring no clock input.

PIN DIAGRAM



BLOCK DIAGRAM





ORDER INFORMATION

Part Number	Bus Speed	Package
VL82C59A-08PC	8 MHz	Plastic DIP
VL82C59A-08QC		Plastic Leaded Chip Carrier (PLCC)
VL82C59A-08CC		Ceramic DIP
VL82C59A-10PC	10 MHz	Plastic DIP
VL82C59A-10QC		Plastic Leaded Chip Carrier (PLCC)
VL82C59A-10CC		Ceramic DIP

Note: Operating temperature range is 0°C to +70°C.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
–CS	1	I	Chip Select - A low on –CS enables –RD and –WR communication between the CPU and the VL82C59A INTA functions are independent of –CS.
–WR	2	O	Write - A low on –WR when –CS is low enables the VL82C59A to accept command words from the CPU.
–RD	3	I	Read - A low on –RD when –CS is low enables the VL82C59A to release status onto the data bus for the CPU.
D0-D7	11-4	I/O	Bidirectional Data Bus - Control, status, and interrupt-vector information is transferred by this bus.
CAS0-CAS2	12, 13, 15	I/O	Cascade Lines - The CAS lines form a unique VL82C59A bus to control a multiple VL82C59A configuration. These pins are outputs for a master VL82C59A and inputs for a slave VL82C59A.
–SP/–EN	16	I/O	Slave Program/Enable Buffer - The –SP/–EN pin provides a dual function. When in the Buffered Mode, it can be used as an output to control the buffer transceivers (EN). When not in the buffered mode, it is used as an input to designate a master (SP = 1) or a slave (SP = 0).
INT	17	O	Interrupt - The INT pin goes high whenever a valid interrupt request is present. It is used to interrupt the CPU and is connected to the CPU's interrupt pin.
IR0-IR7	18-25	I	Interrupt Requests - Asynchronous inputs. An interrupt request is executed by raising an IR input (low to high) and holding it high until it is acknowledged (Edge Triggered Mode), by a high level on an IR input (Level Triggered Mode).
–INTA	26	I	Interrupt Acknowledge - The –INTA pin is used to enable the VL82C59A's interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued from the CPU.
A0	27	I	A0 Address Line - The A0 pin acts together with the –CS, –WR, and –RD pins. It is used by the VL82C59A to decode various Command words the CPU writes and status the CPU needs to read. It is typically connected to the CPU A0 address line (A1 on the iAPX86, 88).
VCC	28	I	+5 V Supply
GND	14	I	Ground

FUNCTIONAL DESCRIPTION

The VL82C59A has been designed to be used in real-time, interrupt-driven microcomputer systems. It controls eight levels or requests, and has a built-in feature for expandability to other VL82C59A's (up to 64 levels). It is programmed by the system's software as an I/O peripheral. A selection of priority modes are usable by the programmer so that the way in which the requests are handled by the VL82C59A can be configured to match the system requirements. The priority modes can be changed at any time during the main program. The entire interrupt structure can be defined as needed, based on the total system requirements.

Interrupt Request Register (IRR) and In-Service Register (ISR) - The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR stores all the interrupt levels which are requesting service, and the ISR stores all of the interrupt levels which are being handled.

Priority Resolver - This logic block sets the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during the –INTA pulse.

Interrupt Mask Register (IMR) - The IMR holds the bits which mask the interrupt lines. The IMR changes the IRR. Masking of a higher priority input will not affect the interrupt request lines of a lower priority.

Interrupt (INT) - This output interfaces to the CPU interrupt input. The VOH level on this line has been designed to be fully compatible with the 8080A, 8085A and 8086 input levels.

Interrupt Acknowledge (–INTA) - The –INTA pulses will cause the VL82C59A to release vectoring information onto the data bus. The format of this data depends on the system mode of the VL82C59A.

Data Bus Buffer- This three-state, bidirectional 8-bit buffer is used to interface the VL82C59A to the system Data Bus. Control words and status information are transferred through the Data Bus Buffer.

Read/Write Control Logic - The purpose of this block is to accept output commands from the CPU. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers. They store the various control formats for device operation. This function block also permits the status of the VL82C59A to be transferred onto the Data Bus.

Chip Select (–CS) - A low on this input enables the VL82C59A. Reading or writing of the chip will not occur unless the device is selected.

Write (–WR) - A low on this input permits the CPU to write control words (ICWs and OCWs) to the VL82C59A.

Read (–RD) - A low on this input enables the VL82C59A to transmit the status of the Interrupt Request Register (IRR), In-Service Register (ISR), the Interrupt Mask Register (IMR), or the interrupt level to the Data bus.

Cascade Buffer/Comparator - This function block stores and compares the identities of all VL82C59A's used in the system. The three I/O pins (CAS0-CAS2) are outputs when the VL82C59A functions as a master and are inputs when the VL82C59A functions as a slave. As a master, the VL82C59A sends the identity of the interrupting slave device onto the CAS0-CAS2 lines. The slave selected can now send its preprogrammed address to the Data Bus during the next consecutive –INTA pulses.

Interrupt Sequence - Interrupt routine addressing is a very important aspect of VL82C59A operation, as is device programmability. Interrupt routine addressing permits direct or indirect jumping to the specific interrupt routine requested with no polling of the interrupting devices. The activities occurring during an interrupt depends on the type of CPU being used.

The events occur as shown below in an MCS 80/85 system:

1. Interrupt Request lines (IR0-IR7) are raised high, setting the corresponding IRR bit(s).
2. The VL82C59A evaluates these requests, then sends an INT to the CPU, if necessary.
3. The CPU acknowledges the INT and responds with the –INTA pulse.
4. When receiving an –INTA from the CPU group, the highest priority ISR bit is asserted, and the proper IRR bit is reset. The VL82C59A will also send a CALL instruction code (11001101) to the 8-bit Data Bus through its D0-D7 pins.
5. The CALL instruction will initiate two additional –INTA pulses which will be sent to the VL82C59A from the CPU group.
6. The two –INTA pulses permit the VL82C59A to send its preprogrammed subroutine address to the Data Bus. The lower 8-bit address is sent at the first –INTA pulse and the higher 8-bit address is sent at the next –INTA pulse.
7. The 3-byte CALL instruction sent by the VL82C59A is then completed. In the AEOI mode, the ISR bit is reset at the end of the third –INTA pulse. If not, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

The sequence of events occurring in an iAPX86-type system are the same until step 4. The sequence then continues:

4. When receiving an –INTA from the CPU group, the highest priority ISR bit is set and the corresponding IRR bit is reset. The VL82C59A does not use the Data Bus during this cycle.
5. The iAPX 86/10 will send a second –INTA pulse. During this second pulse, the VL82C59A releases an 8-bit pointer to the Data Bus and it is read by the CPU.
6. The interrupt cycle is then complete. In the AEOI mode the ISR bit is reset at the end of the second –INTA pulse. If not, the ISR bit remains set until a valid EOI command is sent at the end of the interrupt subroutine.

If there is no interrupt request present at step 4 of either sequence (i.e., the

request duration was too short) the VL82C59A will send an interrupt level 7. Both the vectoring bytes and the CAS lines will appear as though an interrupt level 7 was requested.

INTERRUPT SEQUENCE OUTPUTS FOR MCS-80® & MCS-85®

This sequence is timed by three –INTA pulses. During the first –INTA pulse the CALL opcode is enabled onto the Data Bus.

CONTENTS OF FIRST INTERRUPT VECTOR BYTE

	D7	D6	D5	D4	D3	D2	D1	D0
CALL OPCODE	1	1	0	0	1	1	0	1

During the second –INTA pulse the lower address of the selected service routine is enabled to the data bus. When the interval = 4 address bits A5-A7 are programmed, while addresses A0-A4 are automatically inserted by the VL82C59A. When interval = 8 only A6 and A7 are programmed, while A0-A5 are automatically inserted.

CONTENT OF SECOND INTERRUPT VECTOR BYTE

IR	Interval = 4							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	A5	1	1	1	0	0
6	A7	A6	A5	1	1	0	0	0
5	A7	A6	A5	1	0	1	0	0
4	A7	A6	A5	1	0	0	0	0
3	A7	A6	A5	0	1	1	0	0
2	A7	A6	A5	0	1	0	0	0
1	A7	A6	A5	0	0	1	0	0
0	A7	A6	A5	0	0	0	0	0

IR	Interval = 8							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	1	1	1	0	0	0
6	A7	A6	1	1	0	0	0	0
5	A7	A6	1	0	1	0	0	0
4	A7	A6	1	0	0	0	0	0
3	A7	A6	0	1	1	0	0	0
2	A7	A6	0	1	0	0	0	0
1	A7	A6	0	0	1	0	0	0
0	A7	A6	0	0	0	0	0	0

During the third INTA pulse, the higher address of the correct service routine-programmed as byte 2 of the initialization sequence (address lines A8-A15)-is enabled to the bus.

CONTENT OF THIRD INTERRUPT VECTOR BYTE

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

INTERRUPT SEQUENCE OUTPUTS FOR iAPX86® & iAPX88®

iAPX 86 mode is the same as the MCS-80 mode, with the exception that only two interrupt acknowledge cycles are issued by the processor and no CALL opcode is sent to the processor. The first interrupt acknowledge cycle is like that of MCS-80, 85 systems in that the VL82C59A uses it to internally hold the state of the interrupts for priority resolution. As a master, it issues the interrupt code on the cascade lines at the termination of the INTA pulse. On this first cycle, it does not send any data to the processor. It leaves its Data Bus buffers disabled. On the second interrupt acknowledge cycle (in iAPX86 and iAPX88 modes) the master (or slave) will send a byte of data to the processor with the acknowledged interrupt code as follows (The state of the ADI mode control is ignored and address lines A5-A11 are unused in iAPX86 and iAPX88 mode.):

CONTENT OF INTERRUPT VECTOR BYTE FOR iAPX86, iAPX88 SYSTEM MODE

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

PROGRAMMING

The VL82C59A uses two types of command words generated by the CPU:

1. Initialization Command Words (ICWs): Before normal operation begins, each VL82C59A in the system should be brought to a starting point. This is done by a sequence of 2 to 4 bytes timed by –WR pulses.
2. Operation Command Words (OCWs): OCWs are the command words which command the VL82C59A to operate in various interrupt modes. These modes are:
   A. Fully nested mode
   B. Rotating priority mode
   C. Special mask mode
   D. Polled mode

The OCWs may be written into the VL82C59A anytime following initialization.

Initialization Command Words (ICWS) - When a command is issued with address line A0 = 0 and D4 = 1, this is decoded as Initialization Command Word 1 (ICW1). ICW1 commences the initialization sequence during which the following occurs:

A. The edge sense circuit is reset. Following initialization, an interrupt request (IR) input should make a low-to-high transition to generate an interrupt.
B. The Interrupt Mask Register is cleared.
C. IR7 input is assigned priority 7.
D. The slave mode address is set to 7.
E. Special Mask Mode is cleared and Status Read is set to IRR.
F. If IC4 = 0, all functions that were selected in ICW4 are set to zero. (Non-Buffered mode, no Auto-EOI, MCS-80 and MCS-85 system. Master/Slave in ICW4 is only used in the buffered mode.)

Initialization Command Words 1 and 2 (ICW1, ICW2) - A5-A15: Page starting address of service routines. In an MCS80/MCS85 system, all eight request levels will generate CALLs to eight locations equally separated in memory. These can be programmed to be separated at intervals of four or eight memory locations. The eight routines

will then occupy a page of 32 or 64 bytes, respectively.

The address format is 2 bytes in length (A0-A15). When the routine interval is 4, A0-A4 are inserted by the VL82C59A, while A5-A15 are externally programmed. When the routine interval is 8, A0-A5 are inserted by the VL82C59A, while A6-A15 are externally programmed.

The 8-byte interval will maintain compatibility with software presently being used, while 4-byte interval should be used for a small jump table.

In an iAPX86 and iAPX88 system address lines A15-A11 are inserted in the five most significant bits of the vectoring byte and the VL82C59A sets the three least significant bits in accordance with the interrupt level. A10-A5 are ignored and ADI (Address Interval) is not used.

LTIM: If LTIM = 1, the VL82C59A will operate in the level interrupt mode. Edge detection logic on the interrupt inputs will be disabled.

ADI: CALL address interval. ADI = 1 then interval = 4; ADI = 0 then interval = 8.

SNGL: Single. This indicates that only one VL82C59A is in the system. If SNGL = 1 no ICW3 will be issued.

IC4: If this bit is set, ICW4 must be read. If ICW4 is not used, set IC4 = 0.

Initialization Command Word 3 (ICW3) - This word indicates that there is more than one VL82C59A in the system and cascading is used (SNGL = 0). It will load the 8-bit slave register. The functions of this register are below:

A. In the master mode (either when SP = 1, or in buffered mode when M/S = 1 in ICW4) a "1" is set for every slave in the system. The master will release byte 1 of the CALL sequence (for MCS80/MCS85 system) and will then enable the corresponding slave to release bytes 2 and 3 (for iAPX86, iAPX88 only byte 2) through the cascade lines.

B. In the slave mode (either when –SP = 0, or if BUF = 1 and M/S = 0 in ICW4) bits 2-0 identify the slave. The slave compares its cascade input with these bits. If they are equal, bytes 2 and 3 of the CALL sequence (or just byte 2 of iAPX86, iAPX88) are released by it on the Data Bus.

Initialization Command Word (ICW4) - SFNM: If SFNM = 1, the special fully nested mode is programmed.

BUF: If BUF = 1, then the buffered mode is programmed. In buffered mode –SP/–EN becomes an enable output and the master/slave selection is made by M/S.

M/S: M/S = 1 indicates the VL82C59A is a master, M/S = 0 indicates the VL82C59A is a slave. If BUF = 0, M/S has no meaning.

AEOI: If AEOI = 1, then the automatic end of interrupt mode is programmed.

Microprocessor mode: μPM = 0 sets the VL82C59A for MCS80, MCS85 system operation. μPM = 1 sets the VL82C59A for iAPX86 system operation.

Operation Command Words (OCWs) - After the initialization Command Words (ICWs) are programmed into the VL82C59A, the chip is prepared to accept interrupt requests on its inputs. During VL82C59A operation, a selection of algorithms can command the VL82C59A to operate in different modes through the Operation Command Words (OCWs).

OPERATING CONTROL WORDS (OCWs)

OCW1

A0	D7	D6	D5	D4	D3	D2	D1	D0
1	M7	M6	M5	M4	M3	M2	M1	M0

OCW2

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	R	SL	EOI	0	0	L2	L1	L0

OCW3

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	ESSM	SMM	0	1	P	RR	RIS

Operation Control Word (OCW1) - OCW1 sets and clears the mask bits in the interrupt Mask Register (IMR). M7-M0 control the eight mask bits. M = 1 indicates the channel is masked , M = 0 indicates the channel is enabled.

Operation Control Word 2 (OCW2) - R, SL, EOI - These three bits control the Rotate and End of Interrupt modes and their combinations. A drawing of these combinations can be found on the Operation Command Word Format, Figure 3.

L2, L1, L0 - These bits determine the interrupt level responded to when the SL bit is active.

Operation Control Word 3 (OCW3) ESMM - Enable Special Mask Mode. When this bit is set to 1 it enables the SMM bit to set or reset the Special Mask Mode. When ESMM = 0 the SMM bit is a "don't care".

SMM - Special Mask Mode. If ESMM = 1 and SMM = 1 the VL82C59A will enter Special Mask Mode. If ESMM = 1 and SMM = 0 the VL82C59A will revert to normal mask mode. When ESMM = 0, SMM is not used.

FIGURE 1. INITIALIZATION SEQUENCE

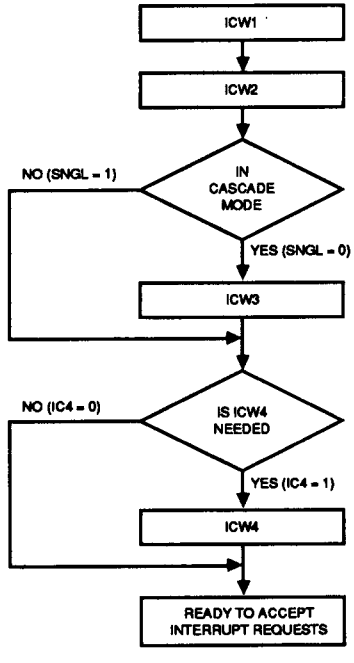
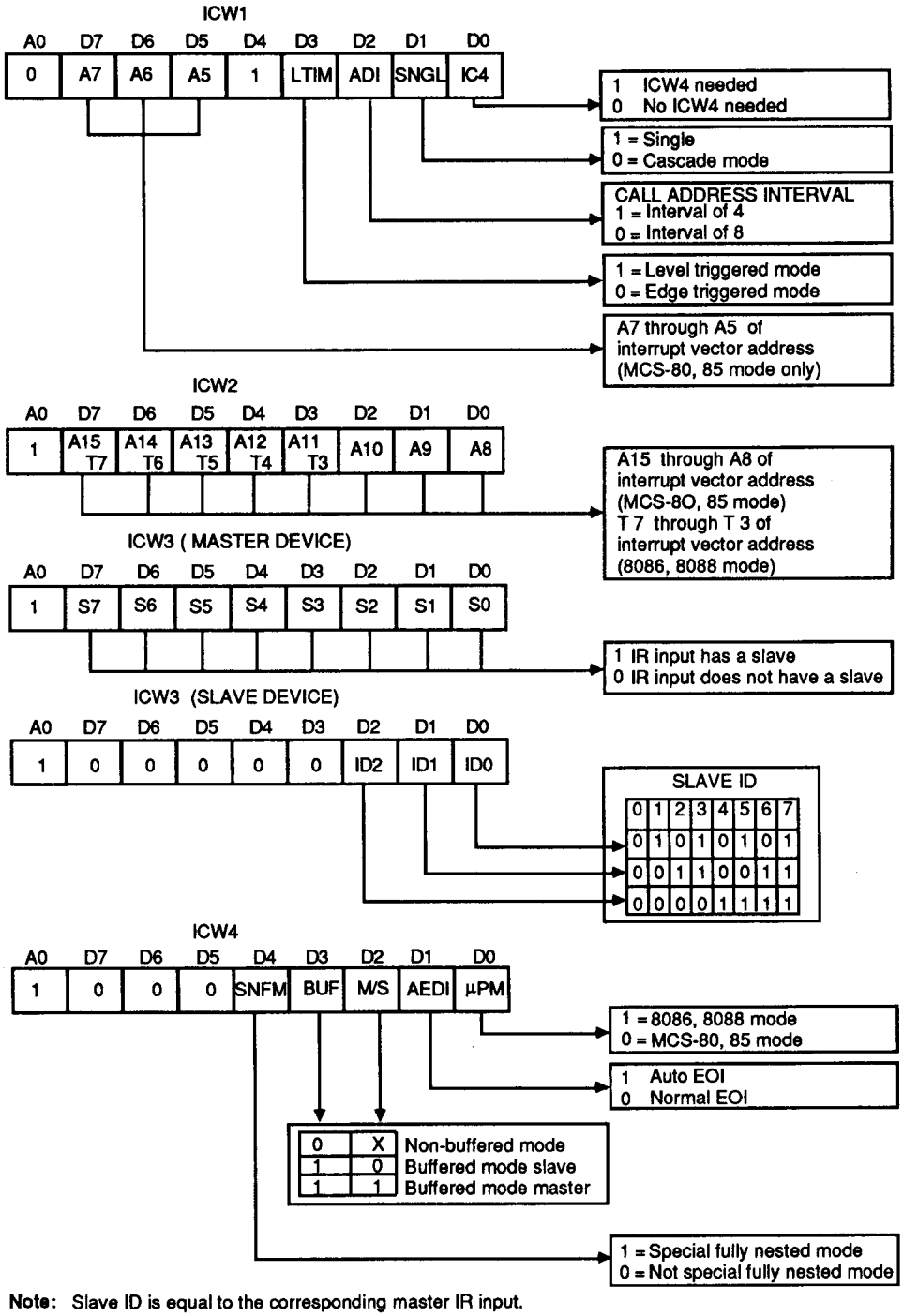
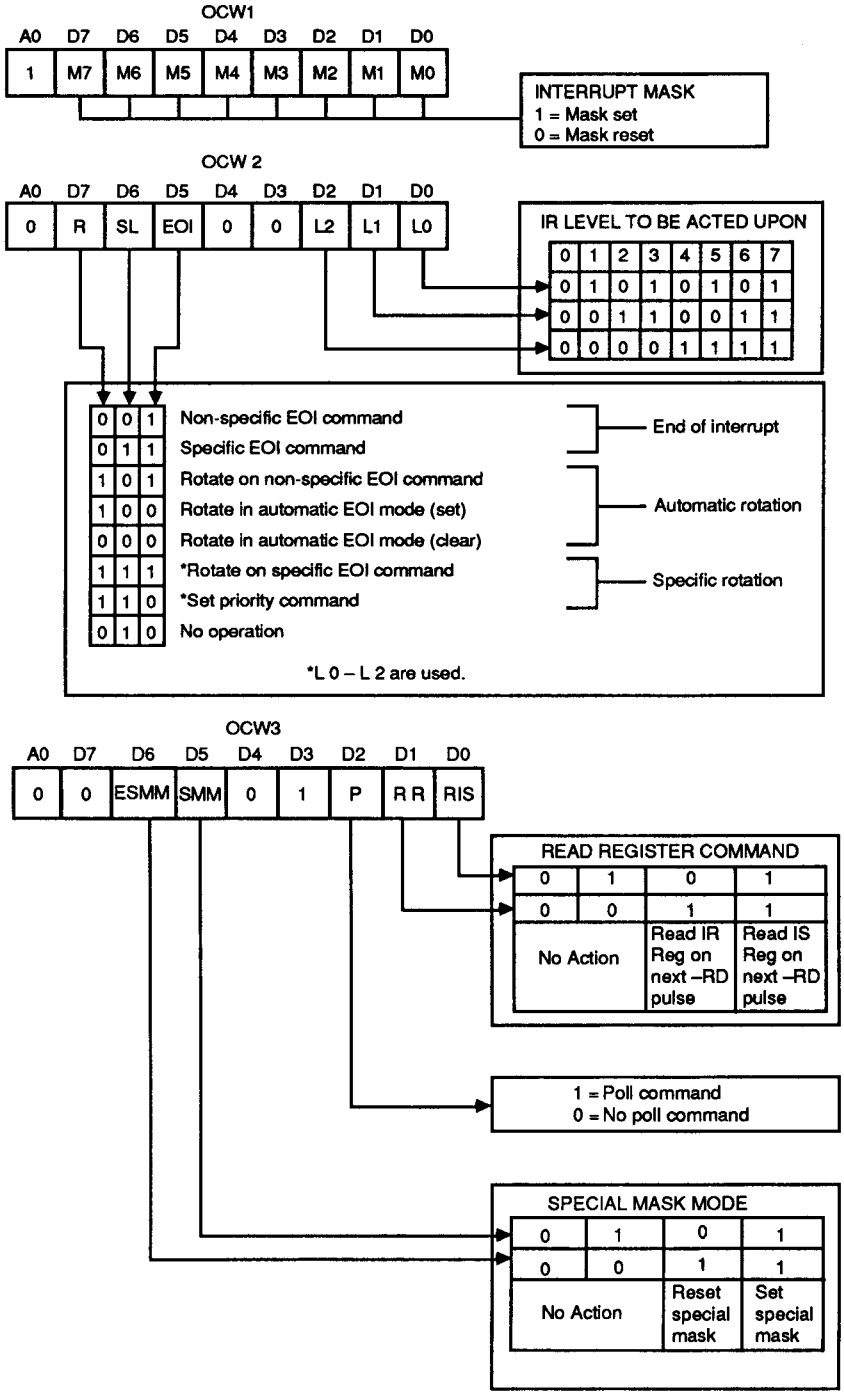


FIGURE 2. INITIALIZATION COMMAND WORD FORMAT



Note: Slave ID is equal to the corresponding master IR input.

FIGURE 3. OPERATION COMMAND WORD FORMAT



MODES

Fully Nested Mode - This is the default mode after initialization unless another mode is programmed. The interrupt requests are ordered in priority from 0 through 7 (0 highest). When an interrupt is acknowledged, the highest priority request is decoded and its vector placed onto the bus. A bit of the Interrupt Service register (IS0-IS7) is also set. This bit stays set until the microprocessor issues an End of Interrupt (EOI) command before returning from the service routine. It also stays set if the AEOI (Automatic End of Interrupt) bit is set, until the trailing edge of the last INTA. While the In-Service (IS) bit is set, all further interrupts of the same or lower priority are disabled. Higher levels will generate an interrupt.

After the initialization sequence, IR0 has the highest priority and IR7 the lowest. Priorities may be be changed in the rotating priority mode.

End of Interrupt (EOI)- The In-Service (IS) bit may be reset either automatically following the trailing edge of the last in sequence –INTA pulse (when AEOI bit in ICW1 is set), or by a command word that should be issued to the VL82C59A before returning from a service routine (EOI command). An EOI command is issued twice if in the Cascade mode, once for the master and once for the corresponding slave.

Two forms of an EOI command are used; Specific and Non-Specific. When the VL82C59A is operated in modes which maintain the fully nested structure, it can determine which IS bit to reset on EOI. When a Non-Specific EOI command is sent the VL82C59A will reset the highest IS bit of those that are set. In the fully nested mode the highest IS level was necessarily the last level operated upon. A Non-Specific EOI can be sent with OCW2 (EOI = 1, SL = 0, R = 0).

When a mode may change the fully nested structure, the VL82C59A may not be able to determine the last level responded to. A Specific End of Interrupt must then be issued, which includes IS level to be reset as part of the command. A Specific EOI can be sent with OCW2 (EOI = 1, SL = 1, R = 0, and L0-L2 is the binary level of the IS bit to be reset).

When the IS is masked by an IMR bit, it will not be cleared by a Non-Specific EOI, if the VL82C59A is in the Special Mask Mode.

Automatic End of Interrupt (AEOI) Mode - If AEOI = 1 in ICW4, then the VL82C59A will operate in AEOI mode until changed by ICW4. In this mode, the VL82C59A will perform a Non-Specific EOI operation at the trailing edge of the last interrupt acknowledge pulse. This mode should be used only when a nested multilevel interrupt structure is not required in a single VL82C59A.

The AEOI mode can only be used in a master VL82C59A.

Automatic Rotation (Equal Priority Devices) - In many applications there are several interrupting devices of equal priority. In this mode the device receives the lowest priority. A device requesting an interrupt will wait, in the worst case, until each of seven other devices with higher priority are serviced. If the priority and "in service" status is:

Before Rotate (IR4 the highest priority-requiring service)

	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
"IS" Status	0	1	0	1	0	0	0	0
	Lowest Priority							Highest Priority
Priority Status	7	6	5	4	3	2	1	0

After Rotate (IR4 was serviced):

	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
"IS" Status	0	1	0	0	0	0	0	0
	Highest Priority							Lowest Priority
Priority Status	2	1	0	7	6	5	4	3

There are two ways to accomplish Automatic Rotation using OCW2, the Rotation on Non-Specific EOI Command (R = 1, SL = 0, EOI = 1) and the Rotate in Automatic EOI Mode which is set by (R = 1, SL = 0, EOI = 0) and cleared by (R = 0, SL = 0, EOI = 0).

Specific Rotation (Specific Priority) - The programmer may change priorities by programming the bottom priority and thereby fixing all of the other priorities (e.g., if IR5 is programmed as the bottom priority device, then IR6 will be the highest one).

The Set Priority command is issued in OCW2 where: R = 1, SL = 1; L0-L2 is the binary priority level code of the bottom priority device.

In this mode internal status is updated by software control during OCW2. It is independent of the End of Interrupt (EOI) command. Priority changes may be performed during an EOI command by using the Rotate on Specific EOI command in OCW2 (R = 1, SL = 1, EOI = 1, and L0-L2 = IR level to receive bottom priority).

Interrupt Masks - Each Interrupt Request input may be masked individually by the Interrupt Mask Register (IMR) by programming OCW1. Each bit in the IMR masks one interrupt channel when it is set (1). Bit 0 masks IR0, bit 1 masks IR1, etc. Masking an IR channel has no affect on the other channels operation.

Special Mask Mode - Some applications will require an interrupt service routine to change the system priorities during its execution under program control. The routine may need to inhibit lower priority requests for a portion of its execution, but enable some, for another portion.

If an Interrupt Request is acknowledged and an End of Interrupt command did not reset the IS bit during a service routine, the VL82C59A will inhibit all lower priority requests without a simple routine to enable them.

In the Special Mask Mode, a mask bit set in OCW1 inhibits further interrupts at that level and enables interrupts from all other levels that are not masked.

Any interrupts may be enabled selectively by loading the mask register.

The Special Mask Mode is set by OCW3 when: SSMM = 1, SMM = 1, and cleared where SSMM = 1, SMM = 0.

Poll Command - In this mode the INT output is disabled or the microprocessor internal Interrupt Enable flip-flop is reset, disabling its interrupt input. Service to devices is programmed by software using a Poll command.

The Poll command is issued by setting P = "1" in OCW3. The VL82C59A treats the next –RD pulse to the VL82C59A (i.e., –RD = 0, –CS = 0) as an interrupt acknowledge, sets the appropriate IS bit if requested and reads the priority level. Interrupt is frozen from –WR to –RD.

The word enabled to the data bus during –RD is:

D7	D6	D5	D4	D3	D2	D1	D0
1	—	—	—	—	W2	W1	W0

W0-W2: Binary code of the highest priority level requesting service.

1: Equal to a "1" if there is an interrupt.

This mode is most useful when there is a routine command common to several levels. Then the –INTA sequence is not needed. It is frequently useful to expand the number of priority levels to more than 64.

VL82C59A STATUS

The input status of several internal registers can be read to update user information from the system. The following registers can be read by using OCW3 (IRR and ISR or OCW1(IMR)).

Interrupt Request Register (IRR): 8-bit register which contains the levels requesting an interrupt to be acknowledged. The highest request level is reset from the IRR when an interrupt is serviced. (Not affected by IMR.)

In-Service Register (ISR): 8-bit register which contains the priority levels that are being updated. The ISR is changed when an End of Interrupt Command is sent.

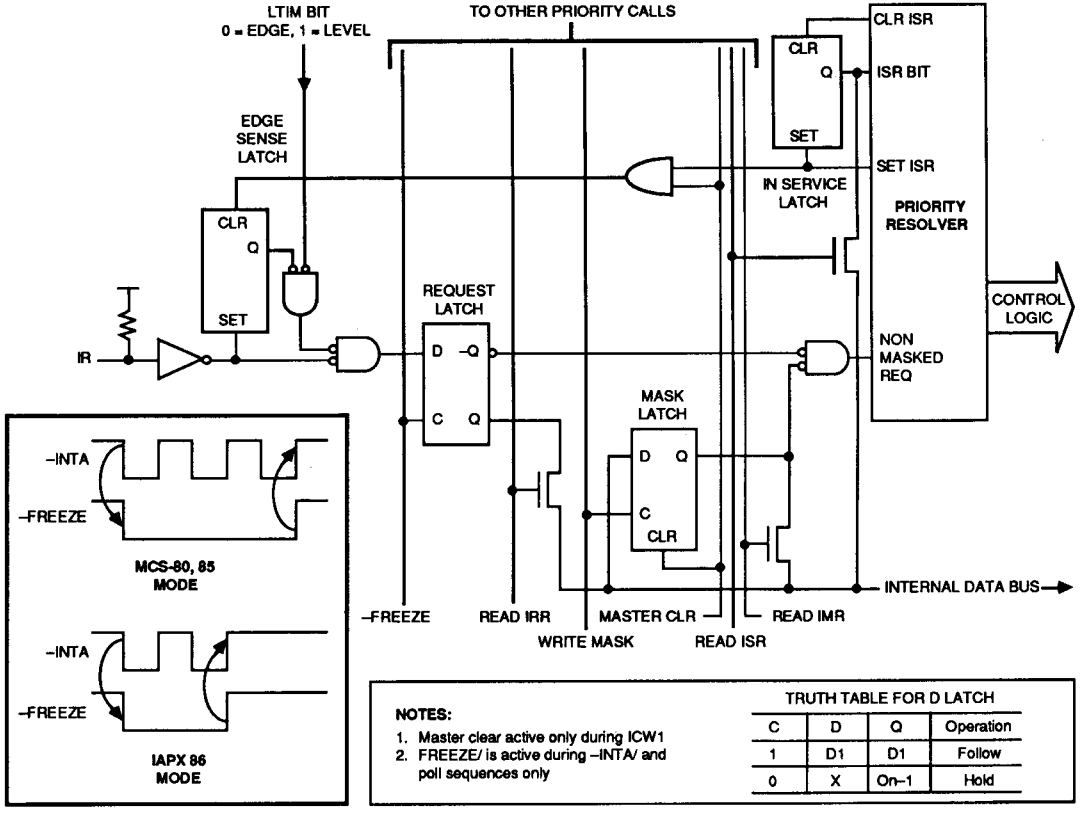
Interrupt Mask Register: 8 bit register which contains the interrupt request lines which are masked.

The IRR may be read when, prior to the –RD pulse, a Read Register Command is sent with OCW3 (RR = 1, RIS = 0).

The ISR may be read when, prior to the –RD pulse, a Read Register Command is sent with OCW3 (RR= 1, RIS - 1).

OCW3 is not written before every status read operation, as long as the status read corresponds with the previous one.

FIGURE 4. PRIORITY CELL–SIMPLIFIED LOGIC DIAGRAM



The VL82C59A retains whether the IRR or ISR has been previously selected by the OCW3. This is untrue when the poll is used.

After initialization, the VL82C59A is set to IRR.

For reading the IMR, no OCW3 is needed. The output data bus will contain the IMR when –RD is active and A0 = 1 (OCW1).

Polling overrides a status read when P = 1, RR - 1 in OCW3.

Edge and Level Triggered Modes - This mode is selected using bit 3 in ICW1.

If LTIM = 0, an interrupt request will be recognized by a positive-going transition on an IR input. The IR input may stay high without generating another interrupt.

If LTIM = 1, an interrupt request can be recognized by a high level on IR input and there is no requirement for edge detection. The interrupt request should be disabled before the EOI command is issued or the CPU interrupt is enabled to preclude a second interrupt from occurring.

Figure 4, shows a basic circuit of the level sensitive and edge sensitive input circuitry of the VL82C59A. The request latch is a "D" type latch, which is transparent.

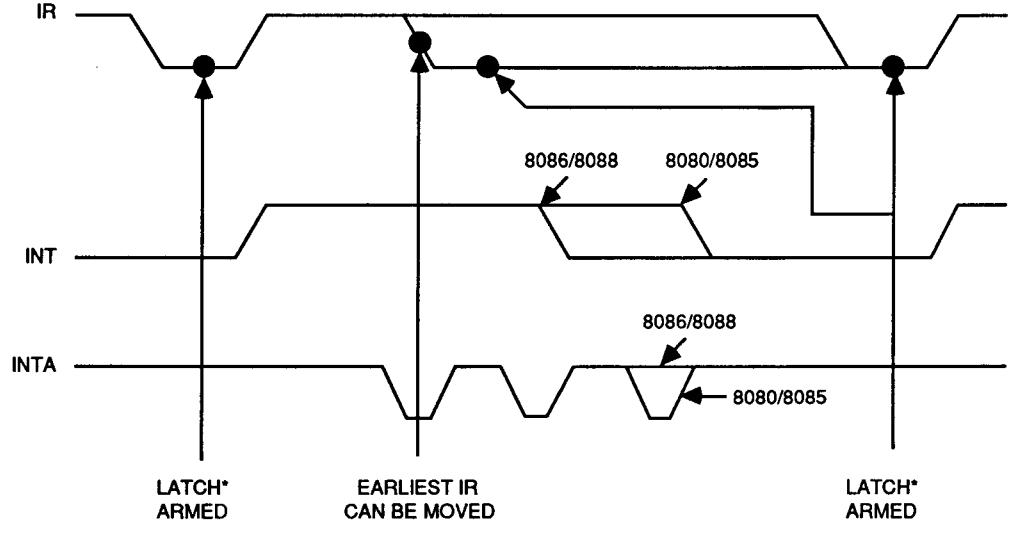
In the edge and level triggered modes, the IR inputs should stay high until after the falling edge of the first INTA. If the IR input goes low before this time, a default IR7 occurs when the CPU responds to the interrupt. This may detect interrupts generated by noise on the IR inputs. The IR7 routine is used for smoothing by simply executing a return instruction thus ignoring the interrupt. If IR7 is needed for other purposes a default IR7 can still be detected by reading the ISR. A normal IR7 interrupt will set the corresponding ISR bit, a default IR7 will not. If a default IR7 routine occurs during a normal IR7 routine, the ISR will remain set. It is necessary to record whether or not the IR7 routine was previously entered. If another IR7 occurs, it is a default.

The Special Fully Nested Mode - This mode can be used for a big system, where cascading occurs, and the priority has to be saved by each slave. Using ICW4, t1qhe fully nested mode will be programmed to the master. This mode is the same as the normal nested mode, except as follows:

A. When an interrupt request from a given slave is in service, the slave is not locked out from the master's priority logic. Further interrupt requests from higher priority IR's within the slave will be recognized by the master and will initiate interrupts to the processor. In the normal nested mode a slave is masked out when its request is in service and no higher requests from the same slave can be handled.

B. When exiting the Interrupt Service routine, the software has to insure that the interrupt serviced was the only one from the slave. This is accomplished by sending a Non-Specific End of Interrupt (EOI) command to the slave, then reading its In-Service register and checking for zero. If empty, a Non-Specific EOI may be sent. If not, no EOI may be sent.

FIGURE 5. IR TRIGGERING TIMING REQUIREMENT



*Edge Triggered Mode Only

Buffered Mode - When the VL82C59A is used in a large system and bus driving buffers are needed, on the data bus (when the cascading mode is used) enabling buffers may cause difficulty.

The buffered mode will structure the VL82C59A to send an enable signal on –SP/–EN to enable the buffers in this mode, when the VL82C59A data bus outputs are enabled, the –SP/–EN output is active.

This change mandates the use of software programming to ascertain whether the VL82C59A is a master. Bit 3 in ICW4 programs the buffered mode, and bit 2 in ICW4 decides whether it is a master or a slave.

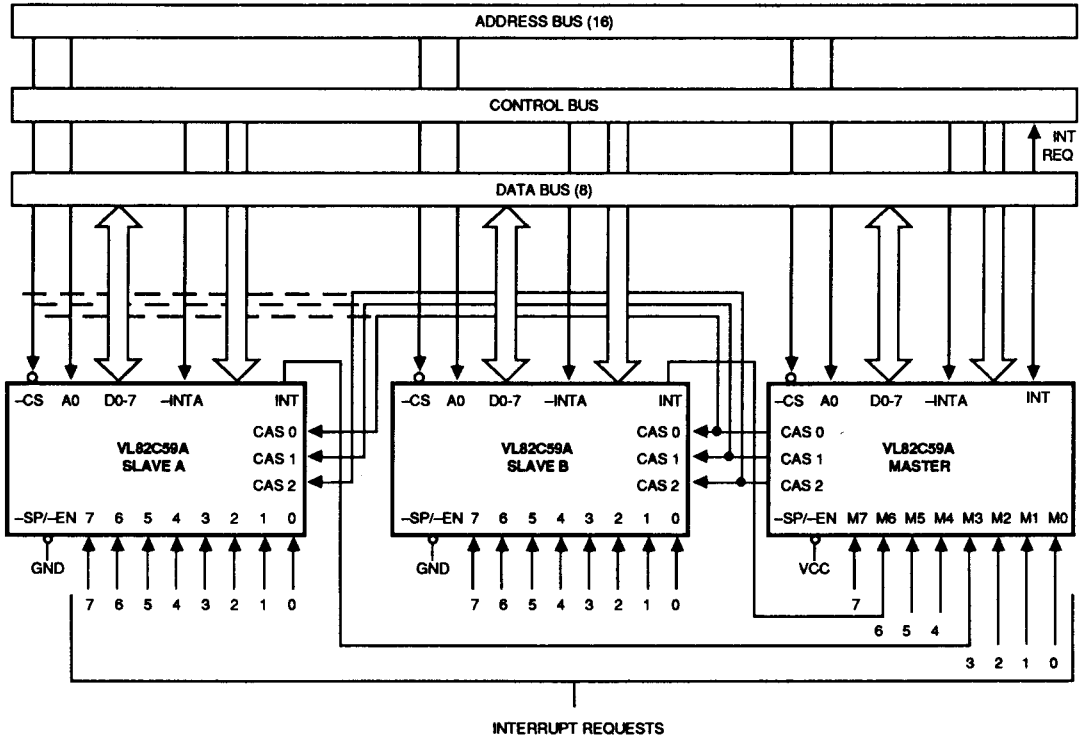
Cascade Mode - The VL82C59A may be interconnected in a system of a master with as many as eight slaves and handle up to 64 priority levels.

The master controls the slaves by the three-line cascade bus. The cascade bus is like chip selects to the slaves during the –INTA. In a cascade configuration, the slave interrupt outputs are connected to the master interrupt request inputs. When a slave request line is asserted and then acknowledged, the master will enable the slave to release the device routine address during bytes 2 and 3 of INTA. Byte 2 is only for 8086/8088-based systems.

The cascade bus lines are normally low and contain the slave address code from the falling edge of the first INTA pulse to the falling edge of the third pulse. All VL82C59As in the system must follow a separate initialization sequence. Each may be programmed to work in a different mode. An EOI command should be issued; once for the master, and once for the slave. An address decoder is needed to assert the Chip Select (CS) input of each VL82C59A.

The cascade lines of the Master VL82C59A are asserted for slave inputs. Non-slave inputs let the cascade line remain inactive (low).

FIGURE 6. CASCADING THE VL82C59A



AC CHARACTERISTICS: TA = 0°C to +70°C, VCC = 5 V ±10%

TIMING REQUIREMENTS

Symbol	Parameter	VL82C59A -08		VL82C59A -10		Units	Conditions
		Min	Max	Min	Max		
tAHRL	A0/–CS Setup to –RD/–INTA Low	10				ns	
tRHAX	A0/–CS Hold after –RD/–INTA High	5				ns	
tRLRH	–RD/–INTA Pulse Width	160				ns	
tAHWL	A0/–CS Setup to –WR Low	0				ns	
tWHAX	A0/–CS Hold after –WR High	0				ns	
tWLWH	–WR Pulse Width	190				ns	
tDVWH	Data Setup to –WR High	160				ns	
tWHDX	Data Hold after –WR High	0				ns	
tJLJH	Interrupt Request Width (Low)	100				ns	Note
tCVIAL	Cascade Setup to Second or Third –INTA Low (Slave Only)	40				ns	
tRHRL	End of –RD to next –RD End of –INTA to next –INTA within an –INTA sequence only	160				ns	
tWHWL	End of –WR to next –WR	190				ns	
tCHCL*	End of Command to Next Command (Not Same Command Type) End of –INTA Sequence to Next –INTA Sequence	400				ns	

*Worst case timing for tCHCL in an actual microprocessor system is typically much greater than 400 ns (i.e. 8085A = 1.6 µs, 8085-A2 = 1 µs, 80C86 = 1 µs, 8086-2 = 625 ns).

Note: This is the low time required to clear the input latch in the edge triggered mode.

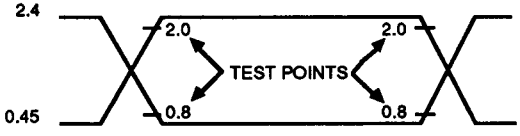
TIMING RESPONSES

Symbol	Parameter	VL82C59A -08		VL82C59A -10		Units	Conditions
		Min	Max	Min	Max		
tRLDV	Data Valid from –RD/–INTA Low		120			ns	1
tRHDZ	Data Float after –RD/–INTA High	10	85			ns	2
tJHIH	Interrupt Output Delay		300			ns	1
tIALCV	Cascade Valid from First –INTA Low (Master Only)		360			ns	1
tRLEL	Enable Active from –RD Low or –INTA low		110			ns	1
tRHEH	Enable Inactive from –RD High or –INTA High		150			ns	1
tAHDV	Data Valid from Stable Address		200			ns	1
tCVDV	Cascade Valid to Valid Data		200			ns	1

TEST CONDITION DEFINITION TABLE

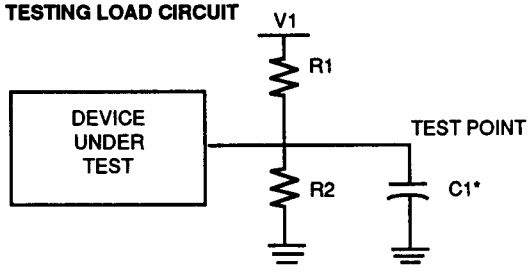
Test Condition	V1	R1	R2	C1
1	1.7 V	523 Ω	Open	100 pF
2	4.5 V	1.8 kΩ	1.8 kΩ	30 pF

TESTING INPUT, OUTPUT WAVEFORM



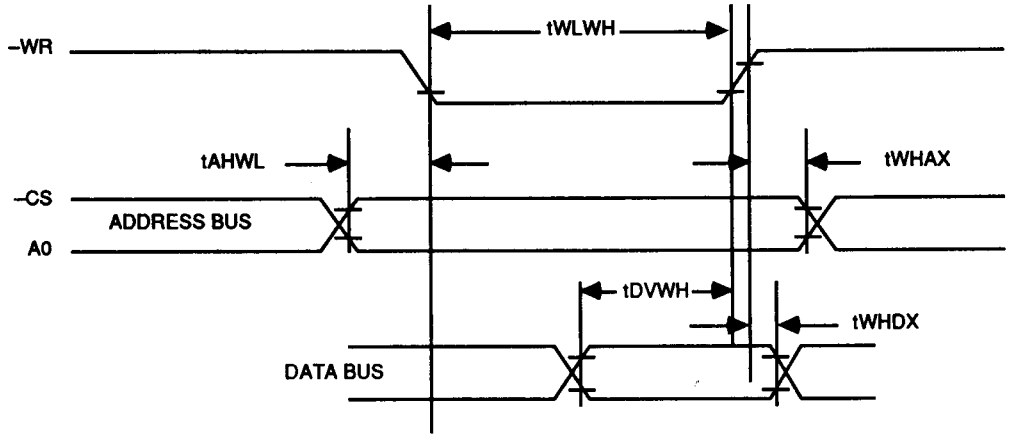
AC testing inputs are driven at 2.4 V for a Logic 1 and 0.45 V for a Logic 0. Timing measurements are made at 2.0 V for a Logic 1 and 0.8 V for a Logic 0.

TESTING LOAD CIRCUIT

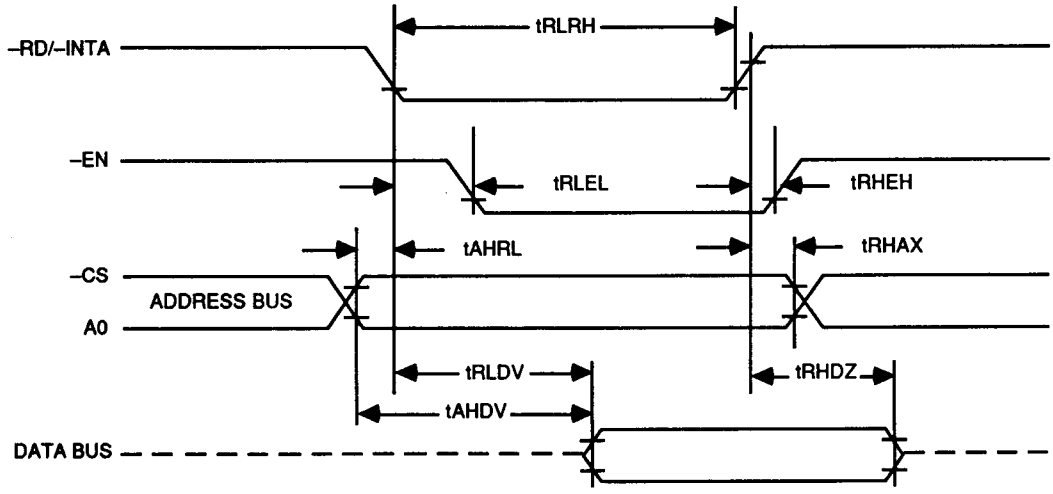


*Includes stray and jig capacitance.

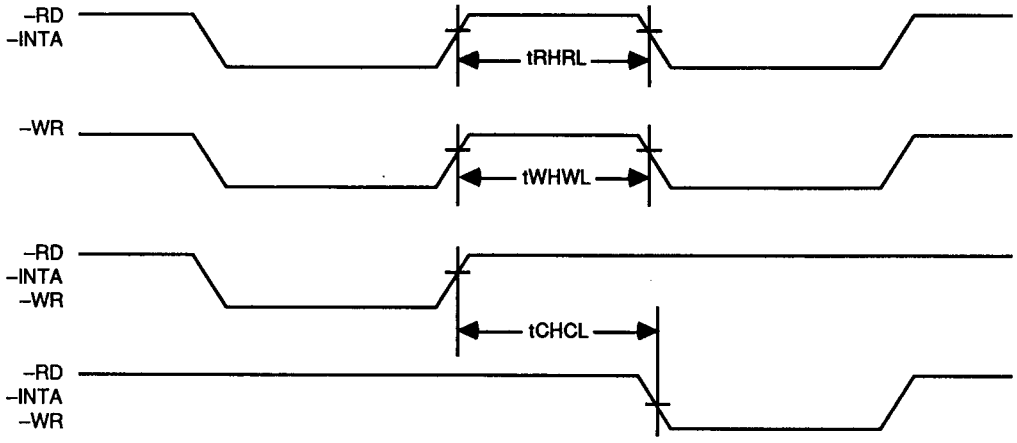
WRITE WAVEFORM



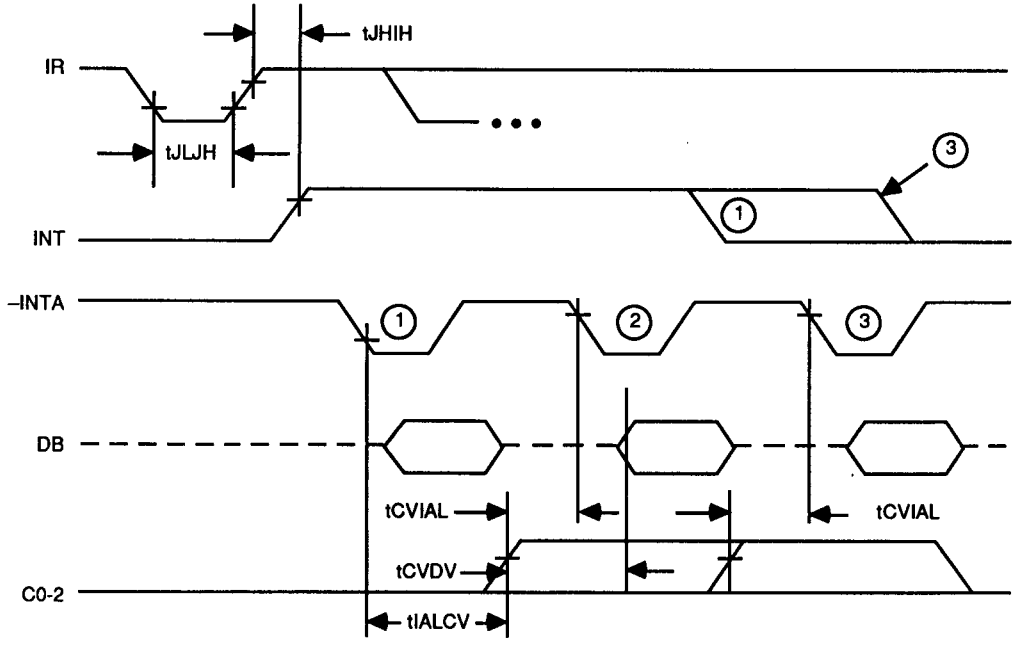
READ/INTA WAVEFORM



OTHER TIMING WAVEFORMS



-INTA SEQUENCE WAVEFORM



Notes: Interrupt output must remain HIGH at least until leading edge of first INTA.

1. Cycle 1 in iAPX 86, iAPX 88 systems, the Data Bus is not active.

ABSOLUTE MAXIMUM RATING

Ambient Temperature Under Bias	0°C to 70° C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin with Respect to Ground	–0.5 V to 7 V
Power Dissipation	1 Watt

Stresses above those listed may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliablility.

DC CHARACTERISTICS: TA = 0°C to 70°C, VCC = 5 V ±10%

Symbol	Parameter	VL82C59A -08		VL82C59A -10		Units	Conditions
		Min	Max	Min	Max		
VIL	Input Low Voltage	–0.5	0.8			V	
VIH	Input High Voltage	2.2	VCC + 0.5			V	
VOL	Output Low Voltage		0.4			V	IOL = 2.5 mA
VOH	Output High Voltage	3.0				V	IOH = –2.5 mA
		VCC –0.4				V	IOH = –100 µA
ILI	Input Leakage Current		±1.0			µA	0 V ≤ VIN ≤ VCC
ILO	Output Leakage Current		±10.0			µA	0 V ≤ VOUT ≤ VCC
ILIR	IR Input Leakage Current		–300			µA	VIN = 0
			+10			µA	VIN = VCC
ICC	Operating Supply Current		5			mA	Note
ICCS	Standby Supply Current		10			µA	VIN = VCC or GND All IR = VCC Outputs Unloaded VCC = 5.5 V

Note: For extended termperature EXPRESS VIH = 2.3 V.

CAPACITANCE: TA = 25° C, VCC = GND = 0 V

Symbol	Parameter	Min	Max	Units	Test Conditions
CIN	Input Capacitance		7	pF	fc = 1 MHz
CI/O	I/O Capacitance		20	pF	Unmeasured pins returned to VSS
COUT	Output Capacitance		15	pF	

Note: Capacitance values guaranteed and sampled, but not 100% tested.