ZARLINK SEMICONDUCTOR

VoiceEdge

VE890 Series

VE8910 Chipset

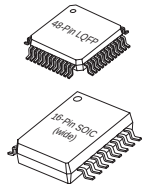
1FXS

A Legerity Voice Solution

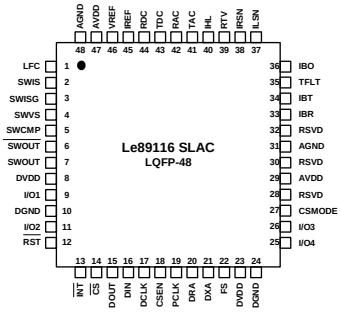
FEATURES

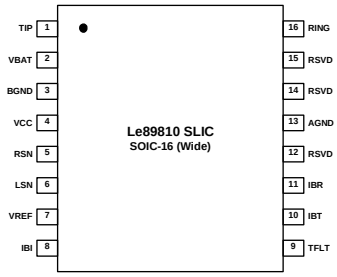
- **Complete 1FXS chipset for VoIP access devices**
- **Implements all the key BORSHT functions**
- **Built-in DC/DC controller configurable for buck-boost or flyback operation**
- **Integrated balanced ringing generator capable of driving 5 REN at 70 V_{PK} or 3 REN at 92 V_{PK}**
- **Low Power Standby with 50 mW typical On-Hook dissipation**
- **Standard 8 kHz and Wideband 16 kHz sample rates**
- **Single hardware design with software support for worldwide markets**
- **VoicePath™ API-II Software**
  - — Significantly reduces development and testing time
  - — Enables modular designs based on the VE8910 and other members of the VE890 Series for 1FXS, 1FXS+1FXO, and 2FXS+1FXO product variants
  - — Allows for a seamless migration between products using a common software architecture
  - — Supported by SDK, development board, and reference designs
- **Support for GR-909/TIA-1063 metallic loop (line) testing using VeriVoice™ Test Suite software**

PACKAGE OPTIONS



PIN ASSIGNMENTS





APPLICATIONS

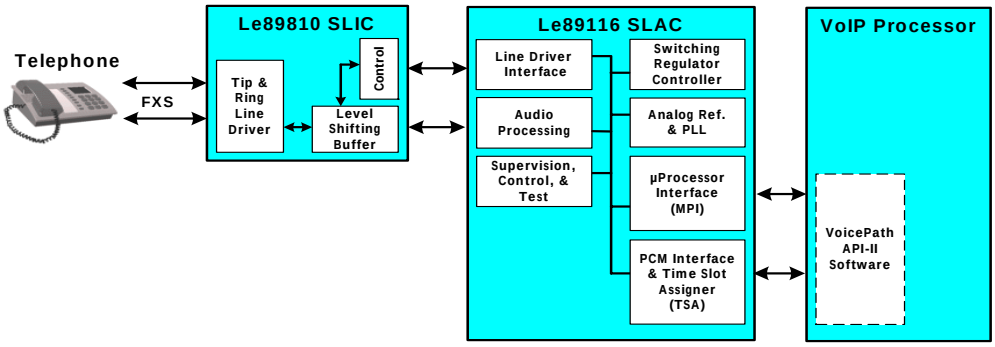
- **Residential and SOHO VoIP CPE, such as ADSL2+/VDSL2 Integrated Access Devices (IADs), Analog Telephone Adapters (ATAs), and VoIP Gateways**

DESCRIPTION

The VE8910 chipset is an integrated, low-cost 1FXS chipset that is optimized for VoIP access devices. The chipset implements a complete BORSHT functionality by providing the necessary voice interface functions to power, ring, signal, and connect one or more telephones. On the digital side, the VE8910 chipset provides standard MPI and PCM interfaces to leading VoIP processors. The VE8910 features low power consumption in all modes of operation; In on-hook Low Power Standby, it typically draws 50 mW, less than half that of its nearest competitor.

The VE8910 chipset is supported by the Zarlink VoicePath™ API-II (VP API-II) software package, which enables designers to program a single hardware circuit for worldwide markets. The VP API-II 'C' code is used to abstract the Zarlink devices from application code while providing functions for controlling, supervising, and testing a set of subscriber lines. The Zarlink VeriVoice™ Test Suite software package provides metallic loop testing based on the Telcordia GR-909 and TIA-1063 recommendations.

FUNCTIONAL BLOCK DIAGRAM



NOTE: On August 3, 2007, Zarlink Semiconductor acquired the products and technology of Legerity Holdings.

Document ID# **081575** Date: **February 4, 2009**
Distribution: **Protected**

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1.0 SOLUTION OVERVIEW

The VE8910 is an integrated telephony chipset with one **F**oreign e**X**change **S**ubscriber (**FXS**) channel for residential VoIP gateways. The FXS circuit supports all the **BORSCHT** (**B**attery feed, **O**ver-voltage support, integrated **R**inging, line **S**upervision, **C**odec, **H**ybrid (2W/4W), and **T**esting) functions necessary for interfacing to legacy analog telephones.

The VE8910 chipset consists of the following:

- Le89116 **SLAC** (FX**S** **L**ine **A**udio **C**ontroller) device
- Le89810 **SLIC** (**S**ubscriber **L**ine **I**nterface **C**ircuit) device
- VoicePath™ API-II software

The SLIC provides the electrical interfaces of the FXS circuits whereas the SLAC provides higher-level functions, such as audio signal conversion and processing, impedance synthesis and call control signal generation and detection. The VoicePath API-II (VP API-II) software initializes the FXS port to its corresponding application or country-specific AC and DC parameters, ringing and other signaling characteristics, and configures the switcher. The VP API-II resides on the customer's VoIP processor and provides high-level control over the telephony functions.

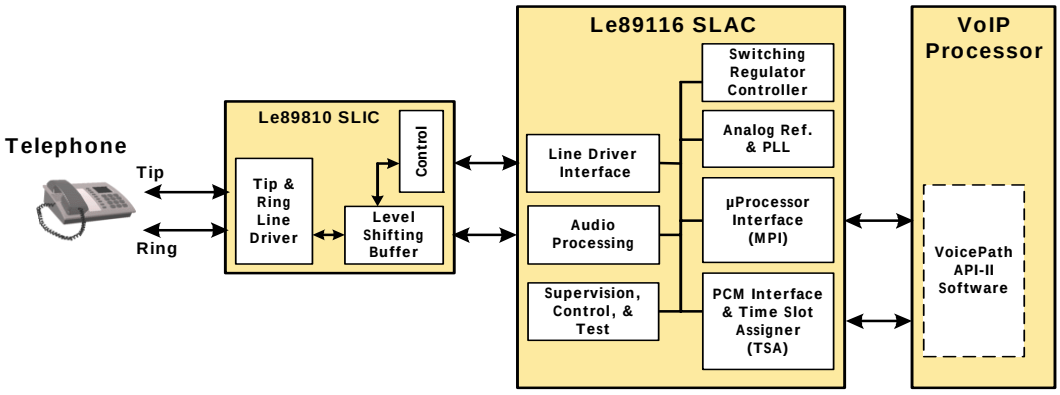
This chipset and VP API-II software reduce system and development cost, component count, and power over competing solutions by achieving a high level of voice integration possible. The programmable, feature rich VE8910 chipset provides a highly functional line interface which meets the requirements of worldwide short loop applications.

The VE8910 chipset is a member of the VE890 Series, which also features the VE8921 (2FXS + 1FXO) and VE8911 (1FXS + 1FXO). Designers can mix multiple members of the VE880 and VE890 Series and have a solution with the right number of FXS and FXO interfaces. Product variants are easily supported due to the modularity of the hardware building blocks and the common software API. For example, the Le89316 SOLAC, a part of the VE8911 chipset, is upwards pin-compatible with the Le89116 SLAC.

The VE8910 chipset performs all the necessary voice telephony functions, from driving the high voltage line to DSP codec functions. All AC, DC, and signaling parameters are fully programmable via the Microprocessor Interface (MPI). The chipset features an integrated high voltage switching regulator controller which generates the high voltages needed for subscriber line driving. Additionally, the VE8910 chipset has line-test support to allow the system to resolve faults to the line or line circuit.

A Windows PC application, VoicePath™ Profile Wizard (VP Profile Wizard), allows the user to select the operating parameters of the FXS channel and to automatically generate the sets of coefficients that are required by the VP API-II for integration with VoIP processor application software. VP API-II offers a seamless migration between products utilizing its common software architecture and interfaces with the Zarlink VeriVoice™ Auditor and the VeriVoice™ Professional line test software.

Figure 1. VE8910 Chipset Block Diagram



2.0 VoicePath™ SDK AND API-II

2.1 VoicePath SDK Overview

The VoicePath Software Development Kit (SDK) is a software package provided to simplify development using Zarlink devices. It consists of:

1. VoicePath API-II or API-II Lite – C source libraries to abstract the VE890 family devices from the application code. The VP API-II contains the full software and requires a Software License Agreement (SLA). The API-II Lite is a subset of the full API and allows for basic functionality for initialization and state / event handling. It does not include tone cadencing or caller ID generation. The API-II Lite does not require an SLA and is suitable for use in open-source applications. This data sheet and associated feature descriptions and specifications require VP API-II version 2.13 or later be used with the VE8910 chipset.
2. VoicePath Profile Wizard – Windows utility used to create data strings required for VP API-II. These data strings are referred to as profiles.
3. Example Hardware Abstraction Layer (HAL) and System Services functions required by VP API-II.
4. Example applications using VP API-II functions. Provided to help the programmer verify correct implementation of the HAL, System Services, and VP API-II function use.
5. Universal VoicePath Demo Board (UVB) – This optional hardware platform is used to demonstrate VE890 chipset capabilities. The UVB may also be used for software development.
6. Zarlink Toolkit – A collection of menu-driven applications to be used in conjunction with the UVB for demonstration and testing. It includes VP-Script, a TCL/TK-based scripting environment, and Mini-PBX, a call control and routing application.

The documentation included in the VoicePath SDK are:

1. *UVB User's Guide*. This document describes the use and operation of the UVB. It includes "Getting Started" using VP-Script and Mini-PBX application.
2. *VP-Script User's Guide*. This manual discusses controlling the UVB and attached reference hardware with the Zarlink VP-Script TCL/TK program for Windows.
3. *VoicePath Profile Wizard User's Guide*. This document describes the use of the Profile Wizard software. This application is used to facilitate the creation and organization of profiles for use with the customer application and the VP API-II.

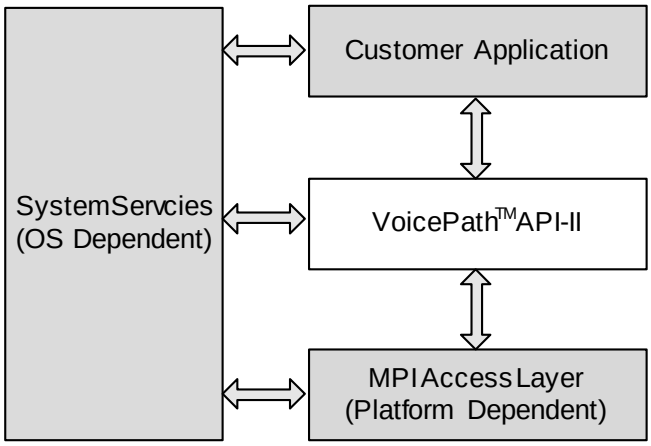
2.2 VoicePath™ API-II Software

2.2.1 Introduction

The Zarlink VoicePath™ Application Programming Interface II (VP API-II) is a 'C' source code module designed to provide a common interface to the Zarlink family of SLIC, DAA, SOLAC and SLAC devices. It provides a high level of abstraction while maintaining the flexibility to allow applications to provide varied voice services. The VP API-II code conforms to the ANSI C standard making it easy to port into any embedded application written in 'C' or 'C++'. This section describes a few of the device and line control capabilities using the VP API-II interface. For a complete list, refer to *VoicePath API-II CSLAC Reference Guide*.

VP API-II uses the layered architecture shown in the following figure. The portion of the diagram in white is Zarlink-provided code, while the gray portions are customer-provided. (Zarlink supplies example "gray" code for the Universal VoicePath Demo Board platform.)

Figure 2. Software Architecture



2.2.2 Features Overview

The features directly supported by VP API-II are dependent upon the underlying SLAC device's capabilities. For the VE8910 chipset, the following features are supported:

- AC and DC Coefficient Programming
- Ringing Parameter (amplitude, frequency, bias, type)
- Tone Generation (frequency and amplitude)
- Highly Programmable Tone and Ringing Cadence
- Caller ID Generation (Types I and II)
- Loop Start Signaling, including Dial Pulse Detection
- Seamless integration of the Zarlink VeriVoice Test Packages for GR-909 Metallic Loop Testing
- Four modes of interrupt support

2.2.3 Configuring VP API-II for the VE8910 Chipset

Two main functions in VP API-II are required in all applications:

1. VpMakeDeviceObject() - Configures a specific device (chip select) to a device context. Provides VP API-II with device specific type (*deviceType*).
2. VpMakeLineObject() - Configures a specific line (channel) to a line and device context. Provides VP API-II with line specific type (*termType*).

When using the VE8910 chipset, the following settings must be used:

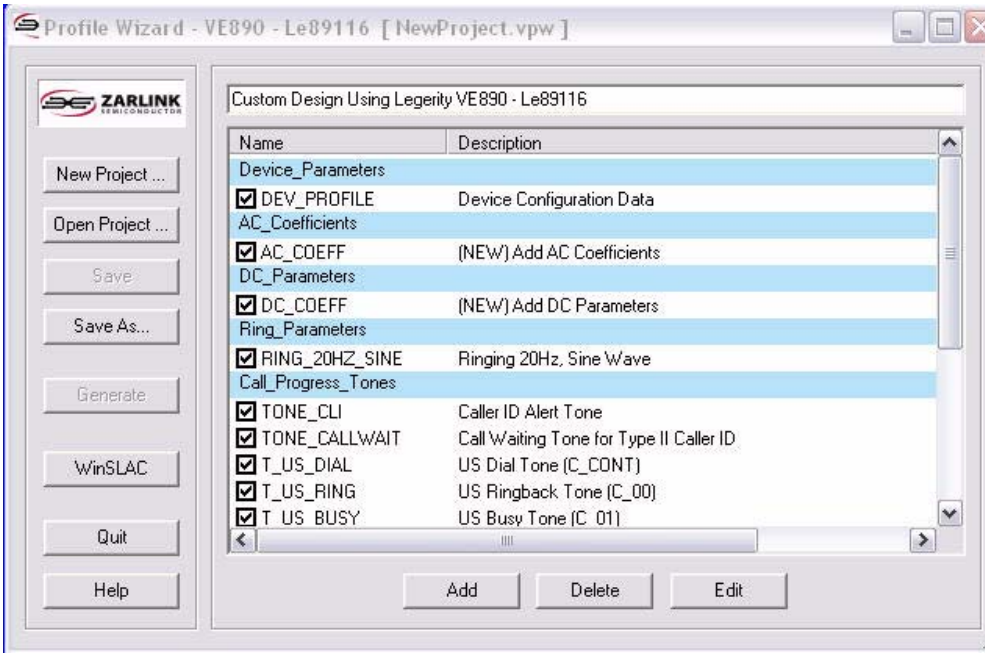
- The value for *deviceType* in VpMakeDeviceObject() must be: **VP_DEV_890_SERIES**
- The value for *termType* in VpMakeLineObject() must be
  - **VP_TERM_FXS_GENERIC** when *channelId* = 0 and Normal Standby operation is desired
  - **VP_TERM_FXS_LOW_PWR** when *channelId* = 0 and Low Power Standby operation is desired. Note that this feature requires that the resistor RLP shown on *SLIC and SLAC Application Circuit,* on page 49 be populated.

Please refer to *VoicePath API-II CSLAC Reference Guide* for additional details.

2.3 VoicePath Profile Wizard

The VP Profile Wizard is a Windows-based application that lets the user select the values of all the Profiles that are supported by the VP API-II. It automatically generates the coefficient files that the API needs to operate. Figure 3 shows a typical screenshot for getting started and creating a new project for the VE8910 chipset and other members of the VE890 Series.

Figure 3. VP Profile Wizard Screen - Creating a New Project



Using the VoicePath Profile Wizard a designer can easily define and generate profiles meeting different country requirements. The VE8910 chipset takes advantage of seven different profiles (see Table 1).

Table 1. VoicePath™ API-II Profiles

Profile Name	Description
Device	The Device Profile provides the Pulse Code Modulation (PCM) bus clock frequency and configuration information, interrupt mode, driver tick rate, maximum number of events / tick, and switching regulator configuration.
AC	The AC Profile is a transmission characteristic profile. The AC Profile holds the internal DSP gain block and filter block commands and data for the FXS channel. Multiple AC Profiles are provided, one for each supported country.
DC	The DC Profile holds the FXS device's DC feed and loop supervision parameters.
Ring	The Ring Profile contains the necessary commands and data to set up the ring generator of an FXS channel. Different profiles can be used to vary the ringing characteristics of a line. Options available in the Ring Profile include ringing waveform, frequency, amplitude, and DC offset.
Tone	The Tone Profile defines the various call progress tones that might be used in the FXS channel. The tones include dial tone, busy, ring-back, and re-order.
Cadence	The Cadence Profile defines the various call progress cadences that might be used in a system. The cadences include stutter dial, busy, ring-back, and reorder.
Caller ID	The Caller ID Profile defines the on- and off-hook signal generation for services such as calling line identification and message waiting indication. This profile abstracts the physical and data link layers of the protocol. FSK and DTMF signaling are supported.

2.4 MPI Access Layer

The MPI Access Layer encapsulates the functions needed to access a SLAC device through its MPI interface. The MPI is the serial communications link between the system's VoIP processor and the SLAC devices in the system. This layer encapsulates the details of the system hardware interface between the host VoIP processor and the Zarlink SLAC devices. This layer is provided by the system designer and is dependent upon the customer's specific hardware design. Zarlink provides example MPI code for use with the Zarlink UVB (Universal VoicePath Demo Board) platform.

Table 2. VP API-II Functions for MPI Access

Function Name	Description
VpMpiCmd()	HAL function to provide buffered MPI command and data to the device, and receive MPI data from the device.

2.5 System Services Layer

System Services encapsulates various services provided by the system software (RTOS or BSP) such as interrupt control, queue management, and timing services. This layer translates between the system services that the VP API-II requires and the underlying hardware/software environment. When porting to a different hardware/software platform, only the Systems Services and the MPI layers are expected to change. Zarlink provides example System Services code for use with the Zarlink UVB.

Table 3. VP API-II Functions for System Services

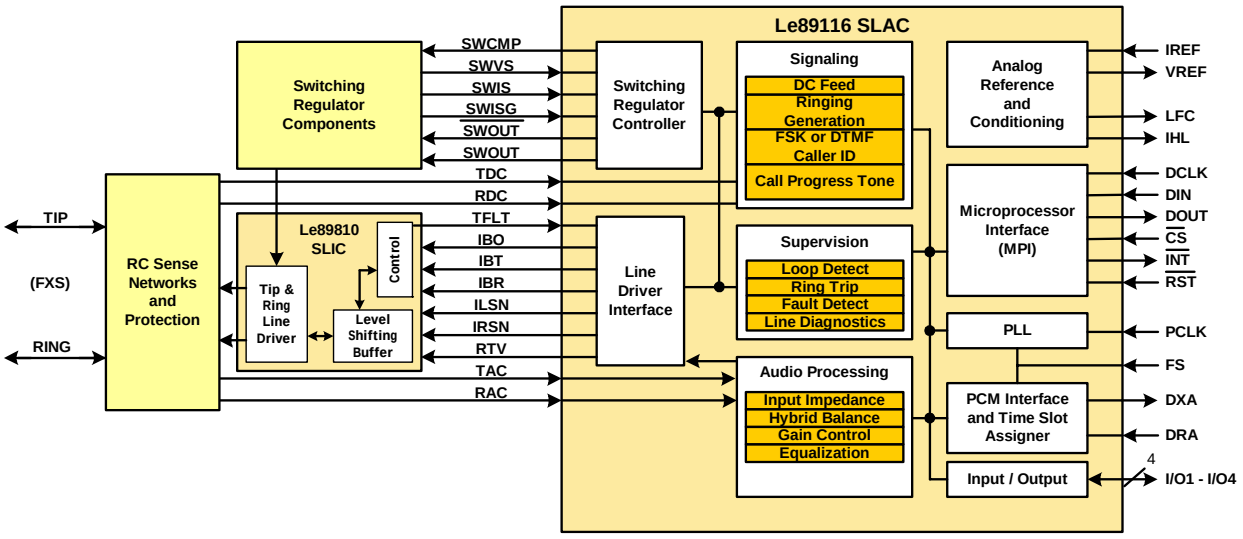
Function Name	Description
VpSysWait()	Delay operator used to suspend program/thread execution. Delay parameter passed in 125 µs steps.
VpSysEnterCritical()	A semaphore operation to provide protected access to device or shared memory. Required only in multi-threaded architectures.
VpSysExitCritical()	A semaphore operation to release protected access to device or shared memory. Required only in multi-threaded architectures.

3.0 FXS

3.1 FXS Channel Overview and Block Diagram

- Performs all **BORSCHT** (**B**attery feed, **O**ver-voltage support, Integrated **R**inging, Line **S**upervision, **C**odec, **H**ybrid (2W/4W), and **T**esting) functions
- Provides high voltage line driving, digital signal processing, and high voltage power generation
- Exceeds GR-909 transmission requirements
- Low Power Standby with 50 mW typical On-Hook consumption
- Single hardware design meets worldwide requirements through software programming of:
  - Ringing waveform, frequency and amplitude
  - DC loop-feed characteristics and current-limit
  - Loop-supervision detection thresholds
  - Off-hook debounce circuit
  - Ground-key and Ring Trip filters
  - Two-wire AC impedance
  - Transhybrid balance impedance
  - Transmit and receive gains
  - Transmit and receive equalization
  - Digital I/O pins
  - A-law/µ-law and linear selection
  - Switching Power Supply
- Supports loop-start signaling
- On-hook transmission
- Smooth polarity reversal
- Overcurrent protection
- Line voltage monitoring
- Relay driver (external catch diode required)
- Wideband 16 kHz and Narrowband 8 kHz sample rates
- Selectable line termination impedances via analog and digital control
- Only 3.3 V logic and single battery supply needed
- Compatible with inexpensive protection networks; accommodates low-tolerance fuse resistors while maintaining longitudinal balance
- Monitors two-wire interface voltages and currents for subscriber line diagnostics
- Can monitor and/or drive Tip and Ring independently
- Self-contained ringing generation and control
  - Programmable Ringing Cadencing
  - Internal battery-backed balanced -- sinusoidal or trapezoidal ringing
  - Integrated Ring Trip filter and software enabled manual or automatic Ring Trip mode
- Flexible tone generation
  - Howler tone generation
  - Call progress tone generation
  - DTMF tone generation
  - Universal Caller ID generation (Types I and II)
- Integrated switching regulator controller
  - Allows for efficiency in all states
  - Line-feed characteristics independent of battery voltage
- Built-in voice-path test modes
- Internal hook buffer allows for up to 10 ms system polling rate

Figure 4. FXS Block Diagram



3.2 Device Profile

3.2.1 Overview

The Device Profile configures device or circuit level parameters for the entire device. This profile is required to enable reliable MPI access to the device, to configure the switching regulator, and to define VP API-II driver parameters. The Device Profile for the VE890 chipset using VP Profile Wizard is shown in Figure 5.

Figure 5. VP Profile Wizard - Device Profile Configuration

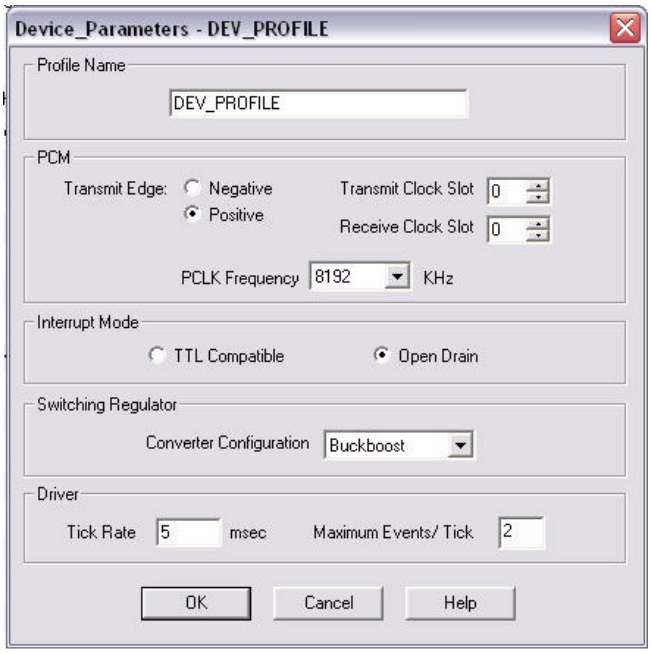


Table 4. VP API-II Functions for Device Profile

Function Name	Description
VpInitDevice()	Resets and initializes device with parameters defined in Device Profile and optionally configures all lines on the device with AC, DC, and Ringing parameters.
VpCalLine()	This function must be called after any of the above FXS functions.

3.2.2 Switching Regulator Controller

The VE8910 chipset supports two options for implementing a DC-DC switching power supply to create the large negative voltage needed to drive the telephone line. The inverting buck-boost topology (see Figure 43, on page 51) is less expensive, but operates over a smaller range of input voltages and has slightly lower performance. The flyback topology (see Figure 44, on page 53) which offers slightly better efficiency and can operate with input voltages as low as +4.75 V, but is more expensive. Each customer can choose the topology most appropriate to his/her application.

The variable output switching regulator is used to generate the VBAT supply voltage needed for the FXS line. An offset voltage (set by the VAS DC feed parameter) is added to the measured Tip-Ring voltage and the resulting signal controls the output of the switching regulator. When loop current is drawn, an additional offset defined as 200 * Iloop is added, to ensure overhead is maintained with up to 100 Ω of total fuse resistance present in the DC feed loop. This architecture enables the switching regulator output voltage to generate the required voltage to feed the line whether in the *On-Hook*, *Off-Hook* or *Ringing* states. The result is maximum power efficiency and minimum power dissipation in all states because the regulator output is always optimum for the current state.

The switching regulator controller on the Le89116 SLAC device allows the negative voltage used by the SLIC to be generated from a single external power supply of typically +12 V. Various combinations of power supply can be configured depending on the requirements of the target application. See the applications section for details of the switcher reference designs. The switcher topology, operating frequency, and the battery voltage levels are set in the Device Profile as shown in Figure 5, on page 9.

3.3 FXS Channel Functional Description

3.3.1 AC Profile

AC Profiles are used to define the input impedance, receive and transmit frequency response, hybrid balance, and initial values for receive and transmit gain. Profile Wizard provides AC FXS Profile examples for over 38 countries including the following:

Table 5. Supported AC FXS Source Impedances

AC Source Impedance	Notes
600 Ω	USA, Argentina, Brazil, Canada, Chile, Hong Kong, India, Korea, Russia, Singapore, and Taiwan. It is also the default selection if no countries are specified.
600 Ω + 1.0 µF	Japan and PBX
270 Ω + (750 Ω // 150 nF)	TBR21 / ES 203 021 (EU countries (not listed elsewhere) + Iceland, Norway, and Switzerland), Israel.
200 Ω + (680 Ω // 100 nF)	China
220 Ω + (820 Ω // 120 nF) and 220 Ω + (820 Ω // 115 nF)	Australia, Austria, Bulgaria, Germany, and South Africa
370 Ω + (620 Ω // 310 nF)	New Zealand and United Kingdom
900 Ω + 2.16 µF	Telcordia GR-57

Notes:

1. *Table 5 provides suggested AC FXS source impedances for the listed countries and standards and are believed to be accurate as of the date of publication of this document. However, standards can and do change from time to time or new ones may be introduced which may differ from the examples provided by Zarlink. Some countries may support more than one standard impedance. Customers are responsible for making sure that they are using the appropriate AC Profiles for their application.*
2. *Profile Wizard makes it easy to add additional countries as long as they are based on the supported impedances.*
3. *The standard files provided with Profile Wizard are for FXS interfaces with two 25 ohm series resistors or PTC's. Please contact Zarlink if alternate series resistor or PTC resistance values are planned.*
4. *Narrowband and Wideband versions of these profiles are available.*

Table 6. VP API-II Functions for AC Profile

Function Name	Description
VpInitDevice()	Resets and initializes device with parameters defined in Device Profile and optionally configures all lines on the device with AC, DC, and Ringing parameters.
VpInitLine()	Resets and initializes line with AC, DC, and Ringing parameters.
VpConfigLine()	Configures line with AC, DC, and Ringing parameters. Similar to VpInitLine() but line is not reset. Values not provided in function call result in line retaining previously set parameters.
VpCalLine()	This function must be called after any of the above FXS functions.

The hardware sections of the device programmed by AC Profiles are described in the following sections.

3.3.1.1 Voice Signal Processor

This block, shown in Figure 6, performs digital signal processing for the transmission and reception of voice. It includes G.711 compression/decompression, filtering, gain scaling, general-purpose tone generators, Caller ID FSK generation, and DTMF generation.

This block performs the codec and filter functions associated with the four-wire section of the subscriber line circuitry in a digital switch. These functions involve converting an analog voice signal into digital PCM samples and converting digital PCM samples back into an analog signal. During conversion, digital filters are used to band-limit the voice signals.

The user-programmable filters perform the following functions:

- Sets the receive and transmit gain
- Performs the transhybrid balancing function

- Permits adjustment of the two-wire termination impedance
- Provides frequency attenuation adjustment (equalization) of the receive and transmit paths

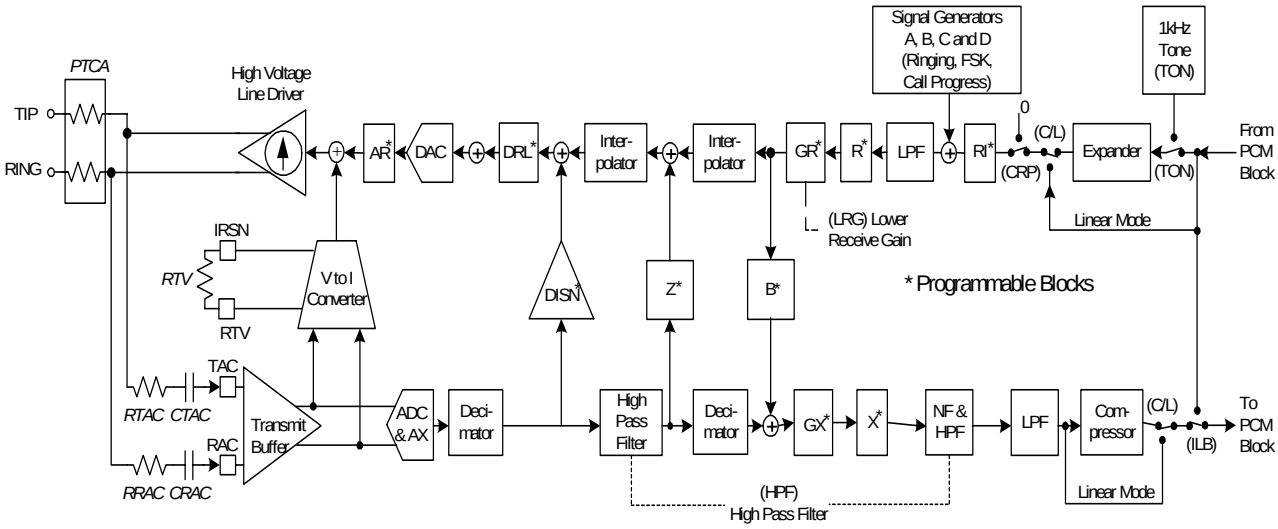
All programmable digital filter coefficients can be calculated using the Zarlink WinSLAC™ software. The PCM codes can be either 16-bit linear two's-complement or 8-bit companded A-law or µ-law.

Besides the codec functions, the integrated voice processing block provides all the sensing, feedback, and clocking necessary to completely control SLIC device functions with programmable parameters. System-level parameters under programmable control include active loop current limits, open circuit feed voltages, and loop supervision thresholds.

The Le89116 SLAC device is architected in such a way as to reduce the real time demands on the host processor. An integrated cadencer/sequencer controls ringing and call progress tone generation. This feature can also generate timed interrupts and substantially reduces the user's need to implement time critical functions.

For subscriber line diagnostics, AC and DC line conditions can be monitored by connecting analog currents and voltages to the voice A/D converter. This gives the system's host processor the ability to configure the system and make system and line tests. Both longitudinal and metallic resistance and capacitance can be measured. This allows identification of leakage resistance, line capacitance, and the presence and status of telephones. These tests are all supported by the Zarlink VeriVoice software.

Figure 6. Voice Signal Processing Block Diagram



3.3.1.2 Impedance Synthesis

The analog impedance synthesis loop is comprised of the SLIC, the AC sense path components, the transmit amplifier, and a voltage to current converter. An external resistor, R_{TV}, synthesizes the nominal impedance in the analog domain. Additional refinement of the impedance is done in the DSP via the Digital Impedance Scaling Network (DISN) and Z-blocks.

The DISN path is comprised of the voice A/D and its first stage of decimation, a DISN, and the voice DAC. The 8-bit DISN synthesizes a portion of the AC impedance which appears in parallel with R_{TV} and is used to modify the impedance set by the external analog network.

The Z Filter is a programmable digital filter providing an additional path and programming flexibility over the DISN in modifying the transfer function of the synthesis loop. Together R_{TV} , DISN, and the Z Filter enable the user to synthesize virtually all required telephony device input impedances.

3.3.1.3 Frequency Response Correction and Equalization

The voice signal processor contains programmable filters in the receive (R) and transmit (X) directions that may be programmed for line equalization and to correct any attenuation distortion caused by the Z Filter.

3.3.1.4 Transhybrid Balancing

The voice signal processor's programmable B Filter is used to adjust transhybrid balance. The filter has a single pole Infinite Impulse Response (IIR) section and an eight-tap Finite Impulse Response (FIR) section, both operating at 16 kHz.

3.3.1.5 Gain Adjustment

The transmit path of the FXS has two programmable gain blocks. Gain block AX is an analog gain of 0 dB or 6.02 dB (unity gain or gain of 2.0), located immediately before the A/D converter. GX is a digital gain block that is programmable from 0 dB to +12 dB, with a worst-case step size of 0.1 dB for gain settings below +10 dB, and a worst-case step size of 0.3 dB for gain settings above +10 dB. The filters provide a net gain in the range of 0 dB to 18 dB. The receive voice path has three programmable gain blocks. GR is a digital loss block that is programmable from 0 dB to 12 dB, with a worst-case step size of 0.1 dB. DRL is a digital loss block of 0 dB or 6.02 dB. AR is an analog gain of 0 dB or 6.02 dB (unity gain or gain of 2) or a loss of 6.02 dB (gain of 0.5), located immediately after the D/A converter. This provides an attenuation in the range of 0 dB to 18 dB.

The gain adjustment block can also be accessed by a VP API-II function directly, without using an AC Profile.

Table 7. VP API-II Functions for Gain Adjustment

Function Name	Description
VpSetRelGain()	Adjusts transmit and/or receive gain up to +/-6 dB. Relative gain of 1 (0 dB) defined as initial value programmed by AC Profile. Note that the supplied AC Profiles have initial FXS gains of -6 dBr receive and 0 dBr transmit

3.3.1.6 Transmit Signal Processing

In the transmit path (A/D) of the FXS, the AC Tip - Ring analog input signal is sensed by the TAC and RAC pins, buffered, amplified by the analog AX gain and sampled by the A/D converter, filtered, companded (for A-law or µ-law), and made available to the PCM blocks. If linear format is selected, the 16-bit data will be transmitted in two consecutive time slots starting at the programmed time slot. The B, X, and GX digital filter blocks are user-programmable digital filter sections.

The first high-pass filter is for DC rejection, and the second high pass and notch filters reject low frequencies such as 50 Hz or 60 Hz. In Wideband mode, the second high pass and notch filters are bypassed.

3.3.1.7 Receive Signal Processing

In the receive path (D/A) of the FXS port, the digital signal is expanded (for A-law or µ-law), filtered, interpolated, converted to analog, and driven onto TIP and RING by the SLIC. The AR, DRL, DISN, Z, R, and GR blocks are user-programmable filter sections.

3.3.2 Speech Coding

3.3.2.1 Linear and Compressed

The A/D and D/A conversion follows either the A-law or the µ-law standard as defined in ITU-T Recommendation G.711. Alternate bit inversion is performed as part of the A-law coding. Linear code is an option on both the transmit and receive sides of the device. Two successive time slots are required for linear code operation. The linear code is a 16-bit two's-complement number which appears sign bit first on the PCM highway.

3.3.2.2 Wideband Codec Mode

The Le89116 SLAC can be operated in a Wideband mode under software API control. In the Wideband mode, the nominal voice bandwidth is doubled to 150 Hz to 6800 Hz to provide better voice quality. The AC Profiles in the Le89116 SLAC must be reprogrammed from the values used in Narrowband mode. In the Wideband mode, the increased data rate is processed by accessing a second set of timeslots equally spaced in the frame. While linear is the usual codec mode, A-law or µ-law companding may also be used in Wideband mode.

Table 8. VP API-II Functions for Speech Coding

Function Name	Description
VpSetOption()	VP_OPTION_ID_TIMESLOT -- Programs transmit and receive timeslot. VP_OPTION_ID_CODEC -- Programs speech coding mode.
VpGetOption()	VP_OPTION_ID_TIMESLOT -- Retrieves current values of transmit and receive timeslot. VP_OPTION_ID_CODEC -- Retrieves current speech coding mode.

3.3.3 DC Profile

DC Profiles are used to define the feed and loop supervision conditions of the line. The DC Profile for the VE890 chipset using VP Profile Wizard is shown in Figure 7.

Figure 7. VP Profile Wizard - DC Profile Configuration

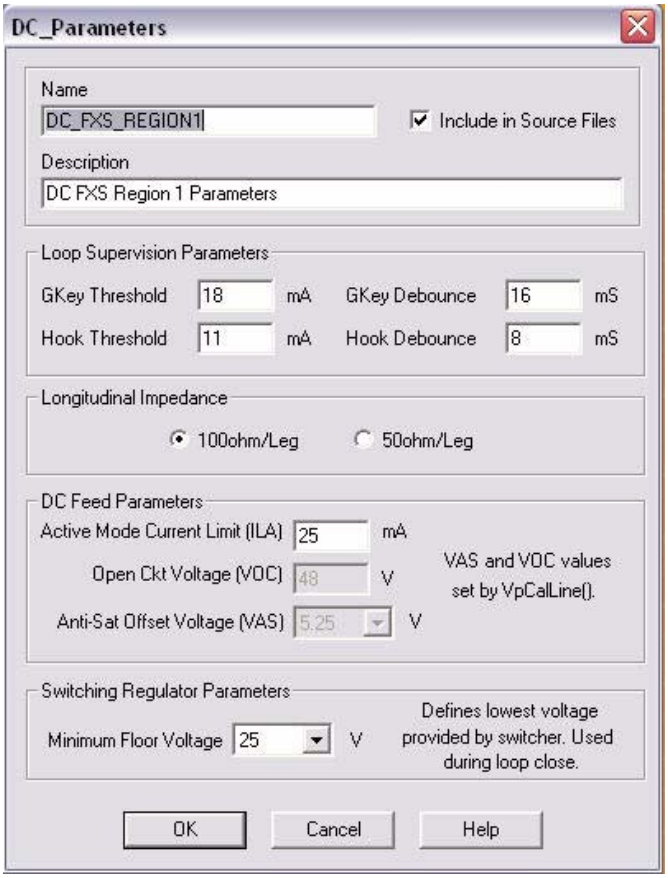


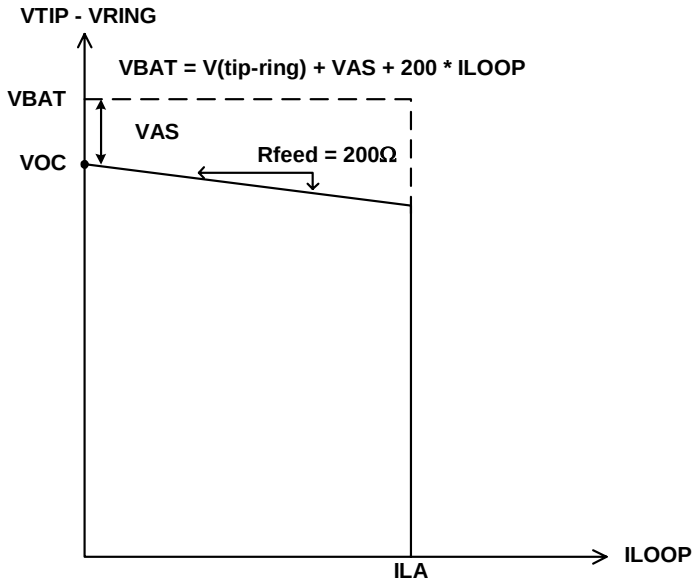
Table 9. VP API-II Functions for DC Profile

Function Name	Description
VpInitDevice()	Resets and initializes device with parameters defined in Device Profile and optionally configures all lines on the device with AC, DC, and Ringing parameters.
VpInitLine()	Resets and initializes line with AC, DC, and Ringing parameters.
VpConfigLine()	Configures line with AC, DC, and Ringing parameters. Similar to VpInitLine() but line is not reset. Values not provided in function call result in line retaining previously set parameters.
VpCalLine()	This function must be called after any of the above FXS functions.

DC feed is active in the VP_LINE_STANDBY, VP_LINE_ACTIVE, VP_LINE_TALK, VP_LINE_OHT, VP_LINE_TIP_OPEN, and all equivalent polarity reversal states. The *Idle* and *Active* feed characteristics appear between Tip and Ring in all states except VP_LINE_TIP_OPEN, where the characteristic appears from Ring to ground in that state. VAS is chosen to ensure that sufficient headroom is available for the amplifiers when On-Hook to support On-Hook transmission with the programmed open circuit (VOC) voltage. Values programmed in device for VAS, VOC, and ILA are determined during VpCalLine() to ensure circuit performance.

The DC Profile produces a DC feed curve at Tip and Ring when the fuse resistors are inside the feedback loop formed by the RTDC and RRDC feedback network. Refer to Figure 8.

Figure 8. DC Feed V/I Characteristics



3.3.4 Ring Profile

The Ring Profile is used to define the type of ringing, ringing frequency, amplitude, offset, ring trip threshold, and ringing current limit. The Ring Profile for the VE890 chipset using VP Profile Wizard is shown in Figure 9.

Figure 9. VP Profile Wizard - Ring Profile Configuration

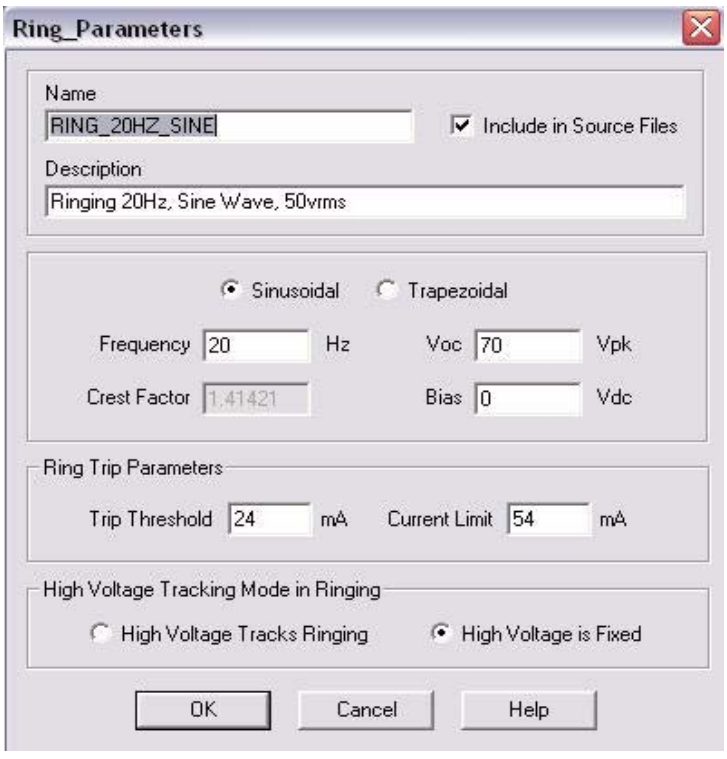


Table 10. VP API-II Functions for Ring Profile

Function Name	Description
VpInitDevice()	Resets and initializes device with parameters defined in Device Profile and optionally configures all lines on the device with AC, DC, and Ringing parameters.
VpInitLine()	Resets and initializes line with AC, DC, and Ringing parameters.
VpConfigLine()	Configures line with AC, DC, and Ringing parameters. Similar to VpInitLine() but line is not reset. Values not provided in function call result in line retaining previously set parameters.
VpCalLine()	This function must be called after any of the above FXS functions.

The primary hardware section of the device programmed by Ring Profiles is Signal Generator A. Signal generators are used for several purposes and will be discussed in section *Tone Profile*, on page 15.

3.3.5 Tone Profile

Tone Profiles provide the capability to program up to four simultaneous tones on the line. The Tone Profile for the VE890 chipset using VP Profile Wizard is shown in Figure 10.

Figure 10. VP Profile Wizard - Tone Profile Configuration

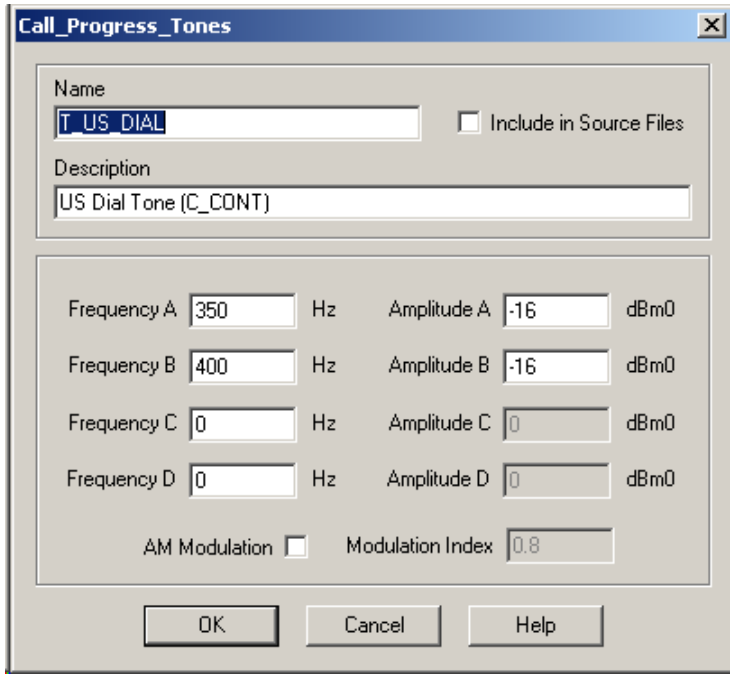


Table 11. VP API-II Functions for Tone Profile

Function Name	Description
VpSetLineTone()	Starts a tone on the line. The tone can be cadenced or “always on”.

Tone generation is performed using highly programmable device signal generators (discussed in *Signal Generation*, on page 16. As discussed later, the signal generators are used for several other VP API-II functions to meet system level requirements.

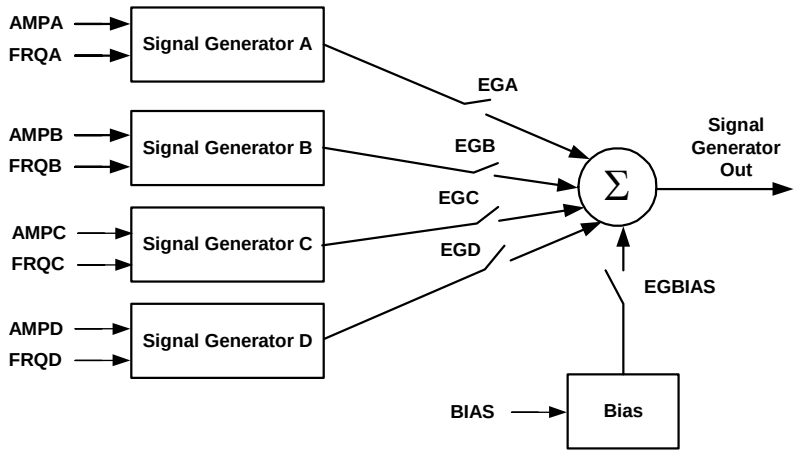
3.3.5.1 Signal Generation

Up to four digital signal generators are available for the FXS channel (see Figure 11). The signal generators are summed into the output path, as shown in Figure 6, on page 11. The Bias generator produces a DC bias that can be used to provide DC offset during ringing or DC test signals during diagnostics. This generator is automatically enabled when entering the VP_LINE_RINGING state (when ringing is applied to the line). Mentioned previously, the Signal Generators are used by several VP API-II operations.

Table 12. VP API-II Functions Using Signal Generators

Function Name	Description
VpSetLineTone()	Provides simultaneous generation of up to four tones. Note that with Tone Cadencing, tones can be enabled/disabled individually to provide Special Indication Tone (SIT).
VpSetLineState()	VP_LINE_RINGING and VP_LINE_RINGING_POLREV -- Uses Signal Generator A (and B for trapezoidal type ringing) with user selected frequency, offset, amplitude, and type.
VpSendSignal()	VP_SENDSIG_DTMF_DIGIT -- Generates a DTMF digit on the line.
VpInitCid()	Sending Caller ID (FSK and DTMF message data supported) on an FXS line. Providing Type II CID Alerting tone.
VpSendCid()	
VpContinueCid()	

Figure 11. FXS Signal Generators



Signal Generator A is also used by the Zarlink VeriVoice Test Package to produce slow ramps. This allows a complex sequence of diagnostic test voltages to be generated in a controlled manner without generating unwanted transients on the line.

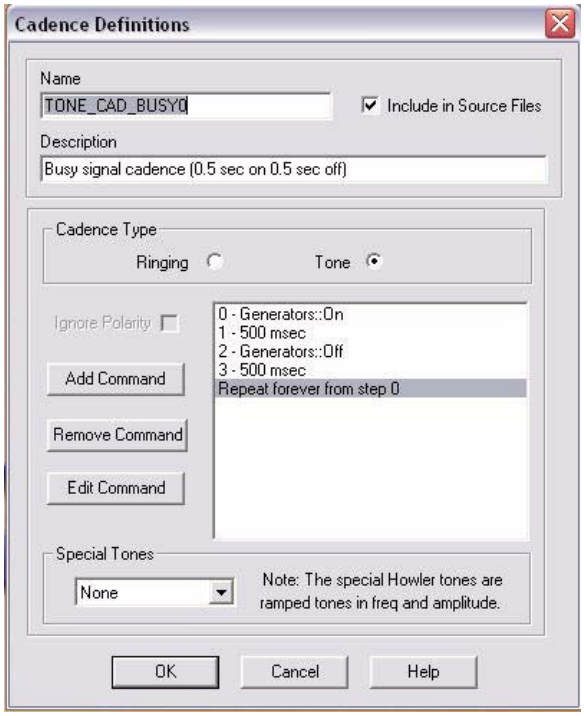
Each generator has independent frequency and amplitude parameters. The frequency accuracy is basically the same as the crystal accuracy of the system.

The EGA/B/C/D bits are controlled by the VP API-II Cadencing engine, described next.

3.3.6 Cadencing

VP API-II Cadencing is a highly flexible set of operators the user selects to implement any country-specific ringing or tone cadence requirements including Special Information Tones (SIT) and howler tones. Figure 12, on page 17 shows how to define cadences for call progress tones and ringing generation with VP Profile Wizard.

Figure 12. VP Profile Wizard - Cadence Profile Example Definition



The VP API-II Cadencer supports the following operations:

1. Time -- Delays (in a non-blocking fashion) program execution.
2. Generator Control -- Enable/Disable selection on a per-generator basis.
3. Branch -- Forces the cadencing to return to a previous step with "repeat" for *n* number of times. If *n* == 0, repeat forever.
4. Line State -- Sets line to specific VP API-II Line State.
5. Send CID -- Starts Caller ID (CID) on the line while continuing to run cadence. Used for Type I Caller ID when CID occurs after first regular ringing cycle in order to achieve a precise delay between the first and second rings.
6. Wait On Caller ID -- Starts Caller ID on the line and suspends currently running cadence. Used for Type I Caller ID when CID occurs prior to the first regular ringing cycle.

Table 13. VP API-II Functions Using Cadencing

Function Name	Description
VpSetLineTone()	Provides tone cadencing for up to four tones. Also supports country-specific howler tone cadencing (AUS, UK, NTT) with ramp frequency and amplitude.
VpSetLineState()	VP_LINE_RINGING and VP_LINE_RINGING_POLREV for Ringing Cadence.
VpInitRing()	User function to provide Ringing Cadence. Also allows use selection of Caller ID Profile associated with Ringing.

3.3.7 Caller ID Generation

The Caller ID block uses Generators C and D to generate phase-continuous 1200 baud FSK tones for on- or off-hook information such as Calling Line ID and Visual Message Waiting Indication. The duration of each (bit) tone is fixed at 0.833 ms (1200 baud).

Bell 202 frequencies are used in the US market, and the ITU V.23 frequencies are used in most other international markets. The signal generator amplitude may need to be adjusted depending on the programmed loss plan. Data transmission levels are normally specified as -13.5 dBm +/-1.5 dB. The default amplitude is -7 dBm0.

Exact preamble and mark sequences are generated by adjusting the framing mode and sending the appropriate number of characters. The VP API-II abstracts this into a simple driver level interface. VP Profile Wizard enables the user to select the Caller

ID parameters and build them into the Caller ID Profile, which generates the necessary coefficients and instructions for the API. Please see example in Figure 13 below.

Figure 13. VP Profile Wizard - Type I Caller ID Profile Example Definition

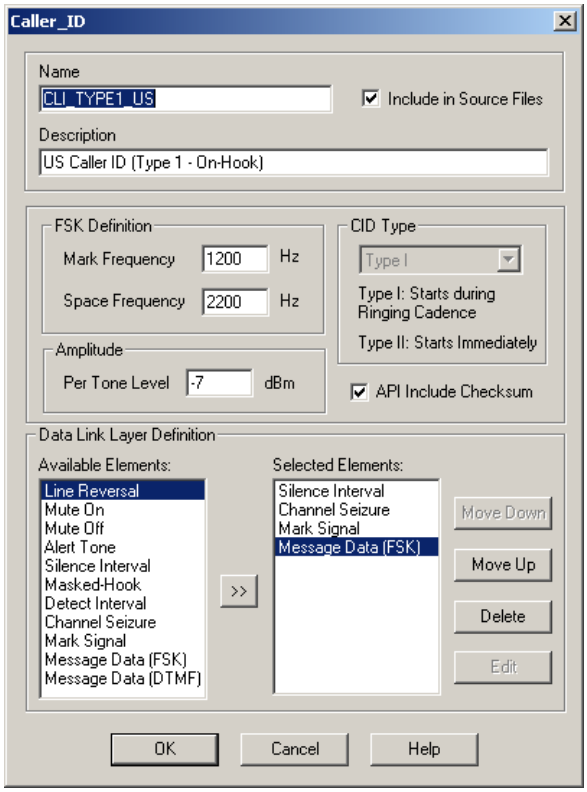


Table 14. VP API-II Functions to Support Caller ID

Function Name	Description
VpInitRing()	User function to provide Caller ID Profile associated with Ringing.
VpSendCid()	Configures and starts Caller ID immediately. Used for Type II Caller ID.
VpInitCid()	Input for Caller ID Message Data up to 32 bytes.
VpContinueCid()	Input for Caller ID Message Data up to 16 bytes. Called after VpInitCid() or VpSendCid() when event VP_LINE_EVID_CID_DATA is generated.

3.4 FXS Channel VP API-II Operation States

3.4.1 Calibration

Calibration of certain battery and line parameters is necessary to meet datasheet specifications.

Table 15. VP API-II Functions for Calibration

Function Name	Description
VpCalLine()	Runs non-blocking calibration routines necessary to meet datasheet specifications. When complete, generates VP_EVID_CAL_CMP event. This function must be called after any FXS line initialization function is executed.

3.4.2 Line State Control

The Signaling Control blocks process the Line State information to perform related control functions such as DC feed, ringing generation, and line test for each channel.

Eight system states are possible for the operation of the FXS channel on the VE8910 chipset: *Shutdown, VP_LINE_DISCONNECT, VP_LINE_STANDBY, VP_LINE_TIP_OPEN, VP_LINE_OHT, VP_LINE_ACTIVE, VP_LINE_TALK, VP_LINE_RINGING*, and reverse polarity of each state.

Table 16. VP API-II Functions for Line State Control

Function Name	Description
VpSetLineState()	Sets line to state specified. After VpInitDevice() or VpInitLine(), the default line state is VP_LINE_DISCONNECT.

3.4.2.1 Shutdown

Shutdown is the power-up and hardware reset state of the device. The System State register is in *Shutdown*, the voice channel is deactivated and the switching regulator is off. No transmission or signaling is possible. Note that *Shutdown* is not a VP API-II line state, but rather a device state upon power up and before the start of execution of the VP API-II software.

3.4.2.2 VP_LINE_DISCONNECT

In the *VP_LINE_DISCONNECT* state, the SLIC outputs are shut off providing a high impedance to the line. This state can be used for denial of service. The switching regulator is active and outputs the programmed SWFV floor voltage. The voice channel is normally deactivated, but can be activated and used with the converter configuration command to monitor the voltages on Tip or Ring for line diagnostics.

3.4.2.3 VP_LINE_STANDBY

The *VP_LINE_STANDBY* state is used when On-Hook. This state behaves differently based on the FXS line termination type selected in *Configuring VP API-II for the VE8910 Chipset,* on page 5.

If the termination type *VP_TERM_FXS_GENERIC* is selected, the DC feed is active, and hook supervision functions are enabled. The loop feed polarity is controlled by the API. The high voltage switching regulator only generates the voltage needed to support the DC line voltage defined by the DC feed. The DC feed drives Tip and Ring to the programmed VOC. Voice transmission is disabled to save power.

If the termination type *VP_TERM_FXS_LOW_PWR* is selected, a special Low Power Standby state is supported to reduce on-hook power consumption to about 50 mW, while still being able to detect off-hook transitions. In this mode, the DC feed is not active and an external voltage is presented to the Ring lead through the resistor RLP. The line voltage is monitored so that any transitions to off-hook state can be detected. Voice transmission is disabled.

3.4.2.4 VP_LINE_OHT

In the *VP_LINE_OHT* states, the DC feed is activated and voice transmission is enabled. *VP_LINE_OHT* allows the transmission of Caller ID information. Hook supervision functions are operating. The switching regulator only generates the negative high voltage needed to support the DC line voltage defined by the DC feed. In this way, power dissipation is minimized.

3.4.2.5 VP_LINE_ACTIVE, VP_LINE_TALK

In the *VP_LINE_ACTIVE* and *VP_LINE_TALK* states, the DC feed is activated. Voice transmission is enabled in *VP_LINE_TALK* and disabled in *VP_LINE_ACTIVE*. *VP_LINE_TALK* allows the transmission of Caller ID information for Type II Caller ID. Hook supervision functions are operating. The switching regulator only generates the negative high voltage needed to support the DC line voltage defined by the DC feed. In this way, power dissipation is minimized.

3.4.2.6 VP_LINE_RINGING

In the *VP_LINE_RINGING* state, the voice DAC is used to apply the ringing signal generated from Signal Generator A and the Bias generator to the SLIC. Internal feedback maintains a low (200 Ω) system output impedance during ringing. The current limit is increased in the *Ringing* state and is programmable via the parameter, ILR. In order to minimize line transients, entry and exit

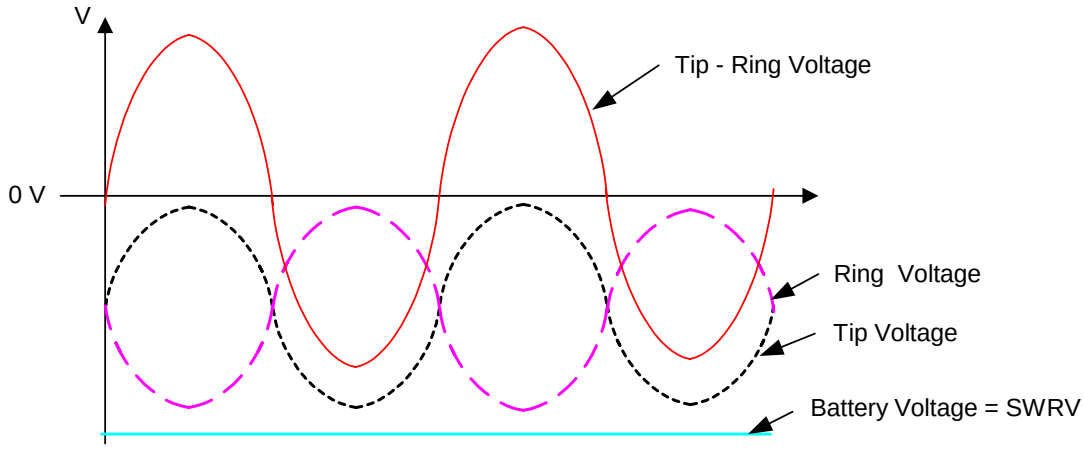
from the *VP_LINE_RINGING* states are intelligently managed by the Le89116 SLAC device. When ringing is requested by the user, the corresponding signal generators are started but not applied to the subscriber line until the ringing voltage is equal to the on-hook Tip-Ring voltage. This algorithm, known as *Ring Entry*, assures that there is a smooth line transition when entering the *VP_LINE_RINGING* state. *Ring Entry* is guaranteed to occur within one period of the programmed ringing frequency. *Ring Exit i*s an analogous procedure whereby the ringing signal is not immediately removed from the line after a Ring Trip or new state request. The ringing signal will persist until its voltage is equal to the required line voltage. The peak ringing voltage that can be generated is equal to |SWRV| - 5 V, in fixed ringing mode. This is automatically calculated by VP Profile Wizard.

While in the *VP_LINE_RINGING* state, the integrated switching regulator may be programmed to behave in one of two ways: tracking or fixed. In Tracking mode, a flyback regulator is used in order to generate just enough headroom to support the instantaneous ringing voltages. In Fixed Regulator mode, an inverting buck-boost switching regulator is used to generate a fixed user-programmed voltage. Note that these two modes require different external switching power supply components. See *Device Profile*, on page 9 for switching regulator modes.

3.4.2.7 Balanced Ringing

Internal balanced ringing drives the subscriber line with balanced ringing voltage waveforms (see Figure 14). In the balanced ringing mode, the ringing signal is driven differentially, thus maximizing the ringing signal swing. In this mode, the SLIC appears to the subscriber line as a voltage source with an output impedance of 200 Ω. The maximum ringing signal possible in the balanced mode is 92 V peak, corresponding to the maximum AC + DC voltages.

Figure 14. Balanced Ringing with Fixed Supply Derived from a Buck-Boost Regulator



3.5 FXS Supervision Processing

Applications can use either an event generation method for monitoring line status, or polling.

Table 17. VP API-II Functions for Line Status Monitoring

Function Name	Description
VpGetEvent()	Typically used to implement event driven method to monitor line status. Provides event queue such that a single event reported for each instance function is called (when an event is active).
VpGetLineStatus()	Typically used to implement polling method to monitor line status.
	• VP_INPUT_HOOK -- Hook Status with mask during Dial Pulse.
	• VP_INPUT_RAW_HOOK -- Real time hook status. Changes during Dial Pulse
	• VP_INPUT_GKEY -- Real time ground key status.

3.5.1 Switch Hook Detection

The FXS supervision circuits of the Le89116 SLAC device provides debounced off-hook indications to an external processor via the MPI. The supervision circuit compares a scaled version of the Tip-Ring current to a programmed off-hook threshold, TSH. The output of the comparator is debounced by a programmable debounce timer, DSH. A debounced *Off-Hook* indication generates an interrupt to the user's host processor.

3.5.2 Ring Trip Detection

Ring Trip is the process of sensing a subscriber's off-hook event during *Ringing*. This is accomplished by sensing the rise in loop current which occurs when a phone goes Off-Hook. The Le89116 SLAC device can detect *Ring Trip* when the ringing signal is purely AC and/or when the ringing signal has a DC bias on it. To do so, the *Ring Trip* algorithm is automatically altered internally by the Le89116 SLAC device based on the user-programmed parameters.

The *Ring Trip* detector uses the Tip-Ring current as an input. This current is rectified so that AC + DC *Ring Trip* can be detected. The output of the rectified signal is compared to a programmable *Ring Trip* threshold and the output digitally debounced. The output is blanked upon ring entry to avoid false Ring Trips.

The *Ring Trip* detection circuit provides debounced *Ring Trip* indications to an external processor via the MPI. The *Ring Trip* circuit compares a scaled version of the Tip-Ring current to a programmed *Ring Trip* Threshold, RTTH. The output of the comparator is processed by the *Ring Trip* algorithm on a cycle by cycle basis to provide immunity to false *Ring Trips*. In addition, spending more than 66% of the time in ringing current limit will generate a trip indication. A positive *Ring Trip* occurs if a trip indication is present for two complete ring cycles, and an interrupt can be raised to the host VoIP processor. For AC-only ringing, the signal is half-wave rectified.

3.6 FXS Line Testing

The VE8911 chipset provides the ability for the user to perform some of the Telcordia GR-909 / TIA-1063 diagnostic testing for the FXS. In Test mode, a variety of input signals can be read from the voice A/D converter. These signals include the switching regulator voltage and the line DC and AC voltages. Two software packages are available from Zarlink for FXS line testing:

3.6.1 VeriVoice™ Auditor

VeriVoice™ Auditor is a basic outward line testing package with pass / fail results. It includes the following tests:

- Line Voltage: Checks for hazardous and foreign AC and DC voltages.
- Receiver Off-Hook: Checks for longitudinal fault, off-hook resistive fault and receiver off-hook.
- Ringer Equivalence Number (REN): Tests the impedance of the line and returns a fail if the REN is too low or high.
- Resistive Fault: Measures three-element resistance.
- GR-909 / TIA-1063: Performs all of the GR-909 outward tests in the correct sequence.

3.6.2 VeriVoice™ Professional

VeriVoice™ Professional is a more advanced test suite featuring the same outward line tests as VeriVoice™ Auditor, but with measured results (not just pass / fail), enhanced REN test, and the following additional inward self tests:

- Regular REN: Provides REN on Tip or Ring to ground as well as Tip to Ring based on impedance
- Electronic REN: Provides REN Tip to Ring, Tip to ground and Ring to ground based on capacitance
- Loopback: Enables receive-to-transmit signal loopback using two different methods
- DC Voltage: Verifies that the line circuit has the ability to drive the voltage ranges required for the normal operation of the line circuit.
- Read Battery Condition: Reads the battery voltages connected to the line circuit.
- Get Loop Conditions: Measures voltages between Tip and Ring, Tip to ground, Ring to ground, and VBAT to ground. Also measures metallic and longitudinal line currents in supported states.

3.7 Analog Reference Circuits

The analog reference circuit generates a reference voltage and reference current for use by the analog portion of the Le89116 SLAC. The reference current is generated through the external resistor RREF, which is typically 75.0 KΩ. The external capacitor, CREF is typically a 1.0 µF or a 4.7 µF ceramic and provides filtering on the reference voltage.

4.0 DIGITAL INTERFACES

4.1 Digital Interfaces Functional Description

The VE8910 chipset interfaces with a PCM backplane and can be controlled over a serial MPI interface. It supports most required PCM clock frequencies from 1.024 MHz to 8.192 MHz, plus four general purpose I/O pins, one of which may be used to drive a relay.

Voice data is interfaced via a PCM highway with time slot assignment capability and control information is communicated over the Microprocessor Interface (MPI). The PCM/MPI interface is flexible and allows a wide range of DCLK (MPI data clock) and PCLK (PCM data clock) frequencies. PCM/MPI interface also allows use of the $\overline{\text{INT}}$ interrupt pin to signal pending interrupts to the external controller.

4.2 Digital Interfaces Features

- MPI and PCM interfaces
  - Selectable PCM clock (PCLK) frequencies: 1.024 MHz, 1.536 MHz, 2.048 MHz, 3.072 MHz, 4.096 MHz, 6.144 MHz, and 8.192 MHz
  - PCM Frame Sync (FS) frequency is set at 8 kHz
- Internal relay driver
  - 3.3 V or 5 V, 150 mW. Please note that an external catch diode is required to protect against inductive kick-back
- Four general purpose I/O pins

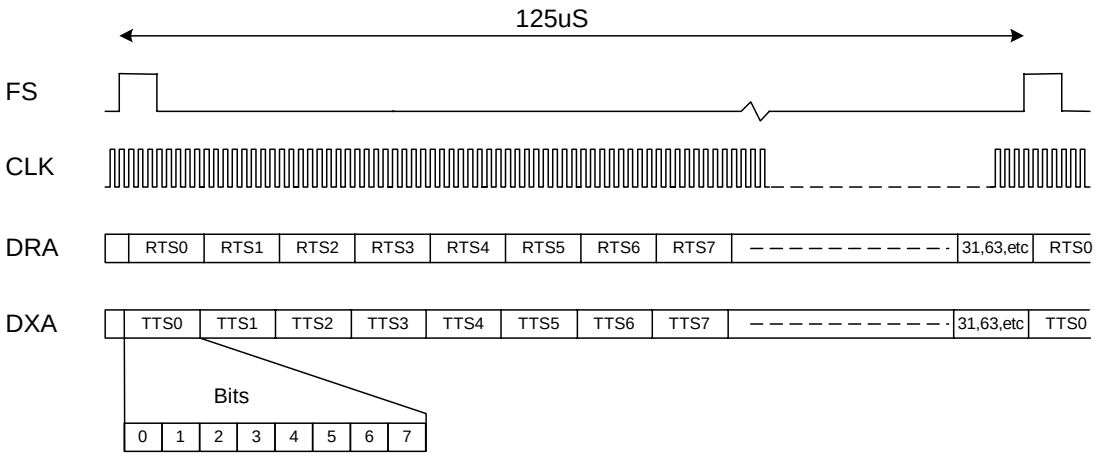
4.3 PCM/MPI Interface and Time Slot Assigner (PCM)

The PCM/MPI Interface and Time Slot Assigner (PCM) is a synchronized serial mode of communication between the system and the Le89116 SLAC device. In PCM mode, data can be transmitted/received on a serial PCM highway. This highway uses Frame Synch (FS) and PCLK as reference.

Data is transmitted out of the DXA pin and received on the DRA pin. The Le89116 SLAC device transmits/receives single 8-bit time slot (A-law/µ-law) compressed voice data or two contiguous time slot 16-bit two's complement linear voice data. The PCLK is a data clock supplied to the device that determines the rate at which the data is shifted in/out of the PCM ports. The FS pulse identifies the beginning of a transmit/receive frame and all time slots are referenced to it. For the Le89116 SLAC device, the frequency of the FS signal is 8 kHz. In Wideband mode, two evenly spaced sets of time slots are exchanged in each frame. The PCLK frequency can be a number of fixed frequencies as defined by the VP API-II. Please refer to *VP Profile Wizard - Device Profile Configuration,* on page 9 for an example setting of the Transmit and Receive Clock Slots, PCM Transmit Edge, and PCLK Frequency.

The VP API-II allows the time slots to be offset to eliminate any clock skew in the system. The Transmit Clock Slot and Receive Clock Slot fields are each three bits wide to offset the time slot assignment by 0 to 7 PCLK periods. The Transmit and Receive Clock Slot is a global command that is applied at the device level. Thus, for each channel, two time slots must be assigned—one for transmitting voice data and the other for receiving voice data. Figure 15 shows the PCM highway time slot structure.

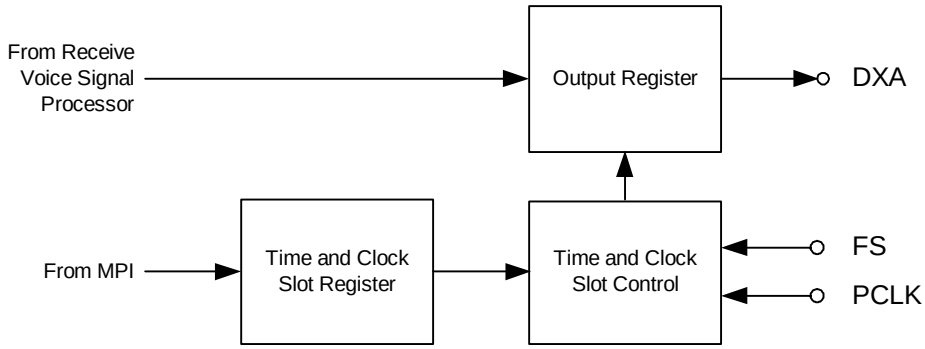
Figure 15. PCM Highway Structure



4.3.1 Transmit PCM Interface

The Transmit PCM interface receives an 8-bit compressed code (A-law/µ-law) or a 16-bit two's complement linear code from the voice signal processor (compressor). The transmit PCM interface logic (Figure 16) controls the transmission of the data onto the PCM highway through the output port selection circuitry and the time and clock slot control block. The data can be transmitted on either edge of the PCLK, as selected in VP Profile Wizard shown in Figure 5.

Figure 16. Transmit PCM Interface



The VP API-II allows the time slot of the selected channel to be programmed. The Transmit Time Slot Register is 7 bits wide and allows up to 128 8-bit time slots in each frame, depending on the value of the PCLK frequency, the encoding scheme, and whether Narrowband or Wideband modes are selected. Refer to Table 18 below for the maximum number of available channels. Please note that linear mode requires two back-to-back time slots to transmit one voice channel. The data is transmitted in bytes with the most significant bit first. Wideband mode requires twice the number of transmit time slots as Narrowband mode.

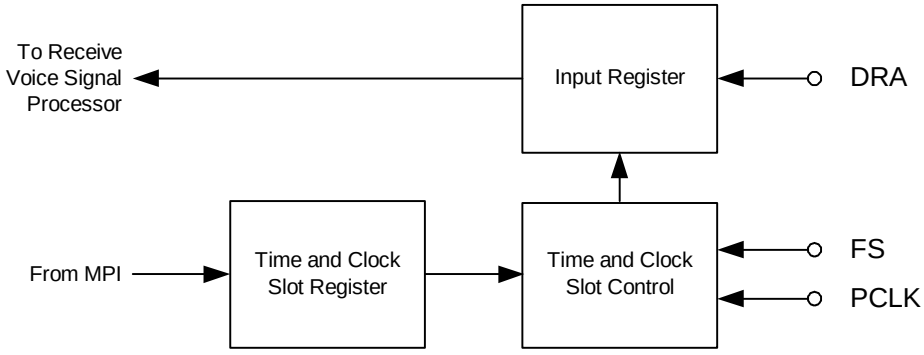
Table 18. Maximum Number of Transmit or Receive Channels

Audio Mode	Encoding	1.024 MHz	2.048 MHz	4.096 MHz	8.192 MHz
Narrowband (8 kHz sampling)	8-bit compressed µ-law/A-law	16	32	64	128
	16-bit linear	8	16	32	64
Wideband (16 kHz sampling)	16-bit linear	4	8	16	32

4.3.2 Receive PCM Interface

The receive PCM interface logic (Figure 17) controls the reception of data bytes from the PCM highway. 8-bit compressed (A-law/µ-law) or 16-bit two's complement linear data is formatted and passed to the voice signal processor (expander).

Figure 17. Receive PCM Interface

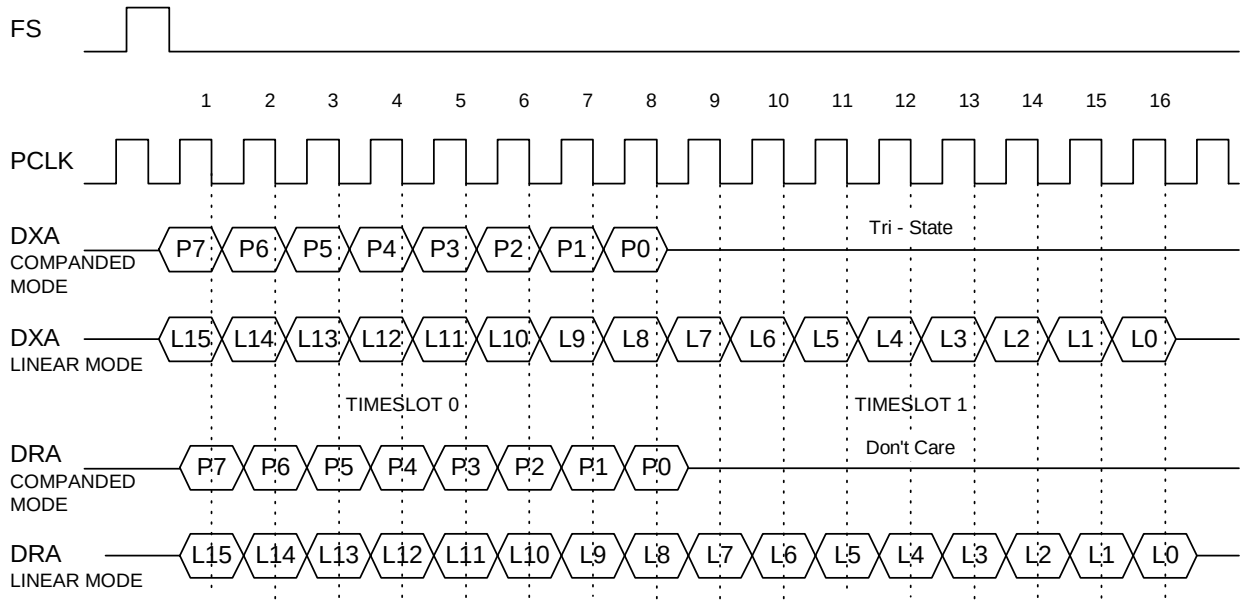


The VP API-II allows the time slot of the selected channel to be programmed. The Receive Time Slot Register is 7 bits wide and allows up to 128 8-bit time slots in each frame. Refer to Table 18 above for the maximum number of available channels. Please note that linear mode requires two back-to-back time slots to transmit one voice channel. The data is transmitted in bytes

with the most significant bit first. Wideband mode requires twice the numbers of receive time slots as Narrowband mode. Please refer to *VP-API-II Functions for Speech Coding, on page 12* for more details about setting the codec mode and transmit and receive time slots.

Figure 18, on page 24 illustrates data flow on the PCM highway.

Figure 18. PCM Data Flow Transmit and Receive Data

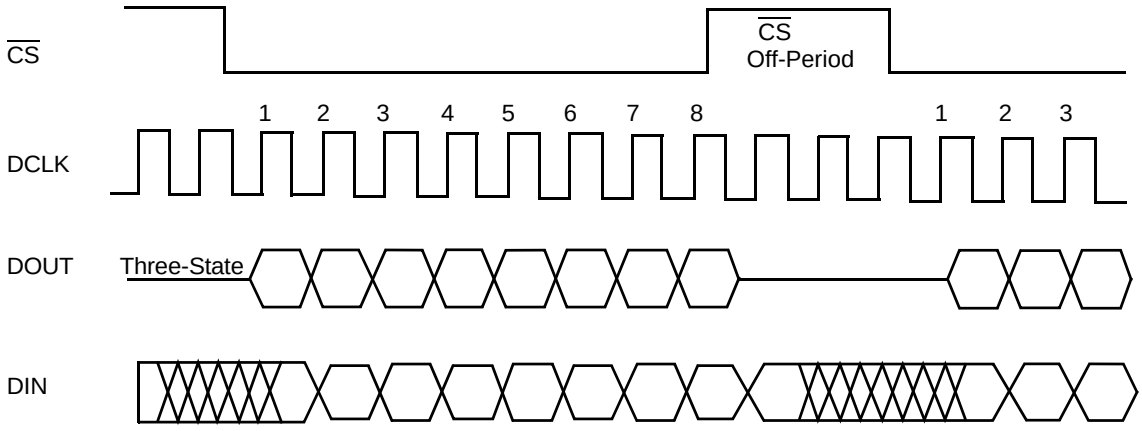


4.4 Microprocessor Interface (MPI)

The Microprocessor Interface (MPI) block communicates with external VoIP processors over a synchronous serial interface. It passes user control information to the other blocks, and it passes status information back to the external host.

The MPI physically consists of a serial data input (DIN) serial data output (DOUT), a data clock (DCLK), a chip select ($\overline{CS}$) and an interrupt signal ($\overline{INT}$) (see Figure 19). The serial input consists of 8-bit commands that can be followed with additional bytes of input data, or can be followed by the Le89116 SLAC device sending out bytes of data. All data input and output is MSB (D7) first and LSB (D0) last. All data bytes are read or written one at a time, with $\overline{CS}$ going high for at least a minimum off period before the next byte is read or written. Only a single channel should be enabled during read commands. There are two other pins that can be used in conjunction with chip select $\overline{CS}$ to qualify the selection for commands. The CSEN and CSMODE pins can be used as additional qualifiers to permit a host controller to select more than one SLAC device with only one chip select and another GPIO.

Figure 19. Microprocessor Interface Timing



All commands that require additional input data to the device must have the input data as the next N words written into the device (for example, framed by the next N transitions of $\overline{CS}$). All unused bits must be programmed to 0 to ensure compatibility with future parts. All commands that are followed by output data will cause the device to output data for the next N transitions of $\overline{CS}$ going low. The Le89116 SLAC device will not accept any commands until all the data has been shifted out. The output values of unused bits are not specified.

An MPI cycle is defined by transitions of $\overline{CS}$ and DCLK. If the $\overline{CS}$ lines are held in the high state between accesses, the DCLK may run continuously with no change to the internal control data. Using this method, the same DCLK can be run to a number of Le89116 SLAC devices and the individual $\overline{CS}$ lines will select the appropriate device to access. Between command sequences, DCLK can stay in the high state indefinitely with no loss of internal control information regardless of any transitions on the $\overline{CS}$ lines. Between bytes of a multi byte read or write command sequence, DCLK can also stay in the high state indefinitely. DCLK can stay in the low state indefinitely with no loss of internal control information, provided the $\overline{CS}$ line remains at a high level. If the system controller has a single bi-directional serial data pin, the DOUT pin of the Le89116 SLAC device can be connected to its DIN pin.

If a low period of $\overline{CS}$ contains less than 8 positive DCLK transitions, it is ignored. If it contains 8 to 15 positive transitions, only the last 8 transitions matter. If it contains 16 or more positive transitions, a hardware reset in the part occurs. If the chip is in the middle of a read sequence when $\overline{CS}$ goes low, data will be present at the DOUT pin even if DCLK has no activity.

The CSEN and CSMODE pins are XORed together and act as an enable to the $\overline{CS}$ signal. See the state table below for the logic. Normal MPI Mode operation is possible with both pins tied high or low. For two-device operation, the first device would have CSMODE grounded and the second device would have CSMODE raised to VCC. To talk to device one in this two device configuration, the controller takes CSEN to ground prior to taking $\overline{CS}$ low. After communicating with device A, $\overline{CS}$ is high, and at that time CSEN can be raised to VCC to enable communication with device B. When $\overline{CS}$ goes low, device B receives the command and device A ignores it. The advantage of this special mode is that the CSEN signal can be a slow signal, while CS must be intimately timed with the Start and Stop of DCLK. This special mode is compatible with many DSP's made by Texas Instruments.

Figure 20. Normal MPI Mode Device Connection

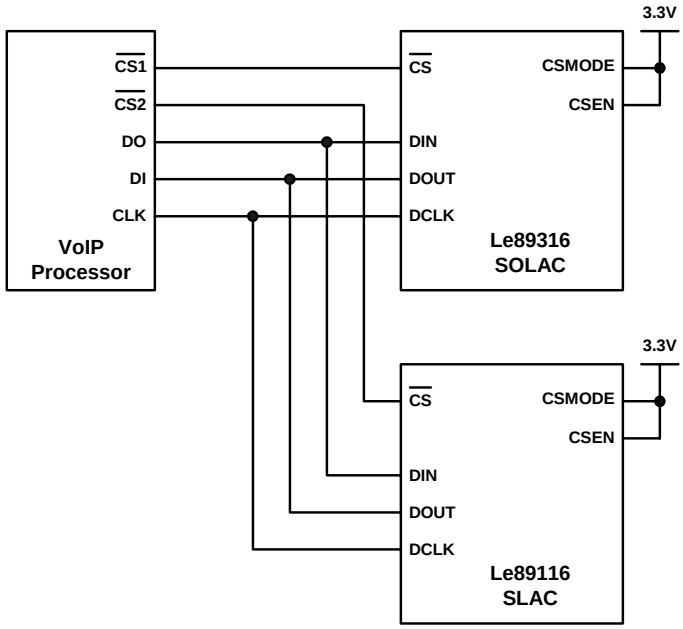
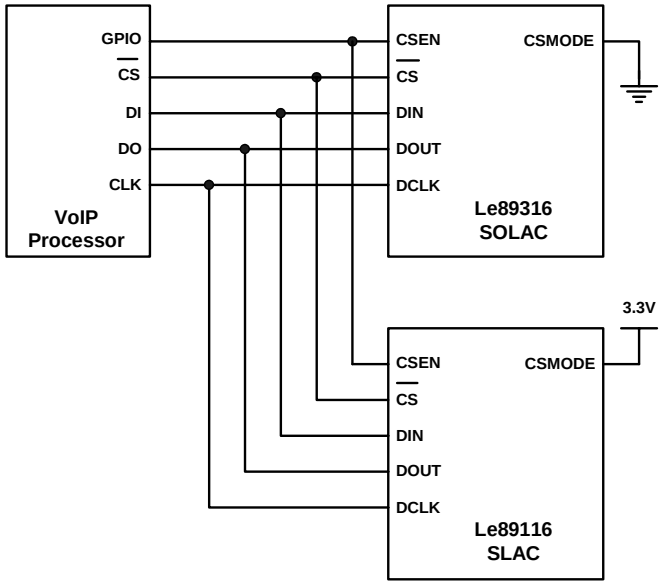


Table 19. Normal MPI Mode Truth Table

CSEN	CSMODE	$\overline{CS}$	Action	MPI
0	0	0	Chip accepts or outputs data on DIN/DOUT using DCLK	Normal MPI action
0	1	0	Chip ignores DIN/DOUT during DCLK	No MPI action
1	0	0	Chip ignores DIN/DOUT during DCLK	No MPI action
1	1	0	Chip accepts or outputs data on DIN/DOUT using DCLK	Normal MPI action
X	X	1	Chip ignores DIN/DOUT during DCLK	No MPI action

Figure 21. CSMODE "Special Mode" Device Connection



4.5 Interrupt Servicing

The Le89116 SLAC device has a well-defined interrupt structure. Interrupts are caused only when a status bit is unmasked and the status bit is subsequently set or toggles (depending on the interrupt). The interrupts can also be masked by the software.

4.6 Input / Output Block

This block controls general-purpose pins that can be configured by the user as inputs, outputs, or relay drivers. Four CMOS-compatible I/O pins (I/O1, I/O2, I/O3, I/O4) are provided for the device. I/O1 can act either as a standard digital input, as a CMOS output, or can be configured as a 3.3 V relay driver (an external protection diode is required) . I/O2 is a standard digital I/O pin that can also generate interrupts when configured as an input. All I/O pins are accessed through the VP API-II.

Table 20. VP API-II Functions for Configuring I/O Lines

Function Name	Description
VpSetOption()	**VP_DEVICE_OPTION_ID_DEVICE_IO** - Used to configure pins individually as input or output. Parameter *directionPins_31_0* used to set pin as input (0) or output (1). Bit in *directionPins_31_0* corresponding to I/O is (I/O1 = 0x1, I/O2 = 0x2, I/O3 = 0x4, I/O4 = 0x8). Other bits in *directionPins_31_0* are ignored. Configuring output type done by setting corresponding bit location in *outputTypePins_31_0* with **VP_OUTPUT_DRIVEN_PIN** (driven). Note that when writing a '1' to a driven pin results in voltage being present on the corresponding I/O pin.
VpGetOption()	**VP_DEVICE_OPTION_ID_DEVICE_IO** - Retrieves current I/O pin configuration. When calling VpGetOption(), an event (Response Category, Event ID **VP_LINE_EVID_RD_OPTION**) is generated and must be processed by the host application. Host application then calls VpGetResults() with pointer to structure of type VpOptionDeviceIoType that is filled in by VP API-II with current I/O configuration data.

Table 21. VP API-II Functions for Write/Read I/O Lines

Function Name	Description
VpDeviceIoAccess()	Parameter *accessMask_31_0* provides bit field access to I/O1-I/O4 as (I/01 = 0x01, I/02 = 0x02, I/03 = 0x04, I/04 = 0x08). Access is by 'OR' combination, so *accessMask_31_0* = 0x0F provides access to all lines simultaneously. Parameter accessType indicates read (**VP_DEVICE_IO_READ**) or write (**VP_DEVICE_IO_WRITE**) operation. For write operation, *deviceIOData_31_0* is used to set lines to '0' or '1'. Bit mask is same as *accessMask_31_0* (I/O1 is set to value in *deviceIOData_31_0* location 0x1, I/O in *deviceIOData_31_0* location 0x2, and so on.). All other parameters (*accessMask_63_32* and *deviceIOData_63_32*) are ignored for the VE8910 chipset)

5.0 ELECTRICAL SPECIFICATIONS

5.1 Absolute Maximum Ratings

Stresses above those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

5.1.1 Absolute Maximum Ratings – Le89810 SLIC

Junction Operating and Storage Temperature	–40 °C < T_J < +145 °C
Ambient Temperature, under Bias	0 °C < T_A < +70 °C
VCC with respect to AGND	–0.4 V_{DC} to + 4.0 V_{DC}
BGND with respect to AGND	+0.4 V_{DC} to – 0.4 V_{DC}
VBAT with respect to BGND	+0.4 V_{DC} to – 105 V_{DC}
TIPD or RINGD with respect to BGND (continuous)	VBAT to + 1.0 V_{DC}
TIPD or RINGD with respect to BGND (10 ms, F = 0.1Hz)	VBAT – 5 V_{DC} to + 5.0 V_{DC}
TIPD or RINGD with respect to BGND (1 µs, F = 0.1Hz)	VBAT – 10 V_{DC} to + 8.0 V_{DC}
TIPD or RINGD with respect to BGND (250 ns, F = 0.1Hz)	VBAT – 15 V_{DC} to + 12 V_{DC}
Current from Tip to Ring	± 150 mA
Package Thermal Resistance In 16-pin SOIC Wide package	θ_{JA} 80 °C/W
ESD Immunity (Human Body Model)	JESD22 Class 1C compliant

5.1.2 Absolute Maximum Ratings – Le89116 SLAC

Junction Operating and Storage Temperature	–40 °C < T_J < +125 °C
Ambient Temperature, under Bias	0 °C < T_A < +70 °C
AVDD with respect to AGND	–0.4 V_{DC} to + 4.0 V_{DC}
AVDD with respect to DVDD	–0.4 V_{DC} to + 0.4 V_{DC}
DVDD with respect to DGND	–0.4 V_{DC} to + 4.0 V_{DC}
AGND with respect to DGND	–0.05 V_{DC} to + 0.05 V_{DC}
Digital pins with respect to DGND	–0.4 V_{DC} to the smaller of +4.0 V_{DC} or DVDD + 0.4 V_{DC}
I/O1current sink to DGND	70 mA
Latch up immunity (any pin)	± 100 mA
Package Thermal Resistance In 48-pin LQFP package	θ_{JA} 65 °C/W
ESD Immunity (Human Body Model)	JESD22 Class 1C compliant

5.1.3 Package Assembly

These 'green' package devices are assembled with enhanced environmentally compatible lead (Pb), halogen and antimony free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer Pb-free board assembly processes. The peak soldering temperature should not exceed 245 ºC during printed circuit board assembly. Refer to IPC/JEDEC J-Std-020B Table 5-2 for the recommended solder reflow temperature profile.

5.2 Operating Ranges

Zarlink guarantees the performance of this device over commercial (0 ºC to 70 ºC) temperature ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Telcordia GR-357-CORE Component Reliability Assurance Requirements for Telecommunications Equipment.

5.2.1 Recommended Operating Conditions - Le89810 SLIC

Ambient Temperature	0 °C < T_A < +70 °C
Ambient Relative Humidity	15 to 85 %
Analog Supply VCC with respect to AGND	+3.3 V_{DC} ± 5 %
VBAT Supply with respect to BGND	-15 V_{DC} to - 100 V_{DC}
BGND with respect to AGND	±100 mV_{DC}
Voltage at any pin that interfaces to the Le89116 SLAC	AGND to 3.465 V_{DC}
Analog Pins	AGND – 0.3 V_{DC} to 3.465 V_{DC}

5.2.2 Recommended Operating Conditions - Le89116 SLAC

Ambient Temperature	0° C < T_A < +70° C
Ambient Relative Humidity	15 to 85 %
Analog Supply AVDD	+3.3 V_{DC} ± 5%
Digital Supply DVDD	+3.3 V_{DC} ± 5%
DVDD with respect to AVDD	±50 mV_{DC}
DGND	0 V_{DC}
AGND with respect to DGND	±10 mV_{DC}
BGND with respect to AGND/DGND	±100 mV_{DC}
Voltage Reference Capacitor: VREF to AGND	4.7 µF ± 20% or higher
Current Reference Resistor: IREF to AGND	75.0 kΩ ± 1%
Digital Pins	DGND to 3.465 V_{DC}
Analog Pins	AGND – 0.3 V_{DC} to AVDD +0.3 V_{DC}

5.3 Electrical Characteristics

FXS Test Conditions

Unless otherwise noted, test conditions are:

- Typical values are for TA = 25 ºC and nominal supply voltages. Minimum and maximum values are over the temperature and supply voltage ranges shown in *Operating Ranges*, on page 28, except where noted.
- FXS Measurements are based on the SLAC test circuit shown in Figure 22 and the SLIC test circuit shown in Figure 23, on page 30
- VBAT = -57 V_{DC} for Idle (On-Hook), On-Hook Transmission (OHT) and OHT with Reverse Polarity line states
- VBAT = -30 V_{DC} for Talk (Off-Hook) line state and the DC feed programmed to ILA = 26 mA, VOC = 48 V_{DC}, VAS = 9 V_{DC}, and ILR = 60 mA
- AC and DC load resistance R_L = 600 Ω
- 0 dBm0 = 0 dBm (600 Ω) = 0.7746 V_{RMS}. Digital gains GX0 and GR0 to achieve 0 dBr relative levels are:
  - GX0 = +6.797 dB (7A20h) A-law or linear and
    GX0 = +6.737 dB (2A20h) µ-law to set A/D transmit gain to 0 dB
  - GR0 = -1.793 dB (6AA0h) A-law or linear and
    GR0 = -1.720 dB (3AA0h) µ-law to set D/A receive gain to 0 dB
- Default (unity) gain in X, R, DRL, AX and AR blocks
- Default coefficients in DISN, Z- and B-Filters
- Ringing Tests have two conditions: C1, and C2:
  - C1 Ringing 92 V_{PK} (65 V_{RMS}) 0 V_{DC} offset and 2333 Ω in series with 24 µF load (3 REN), VBAT = -100 V_{DC}
  - C2 Ringing 70 V_{PK} (50 V_{RMS}) 0 V_{DC} offset and 1386 Ω in series with 40 µF load (5 REN), VBAT = -75 V_{DC}

Figure 22. SLAC Test Circuit

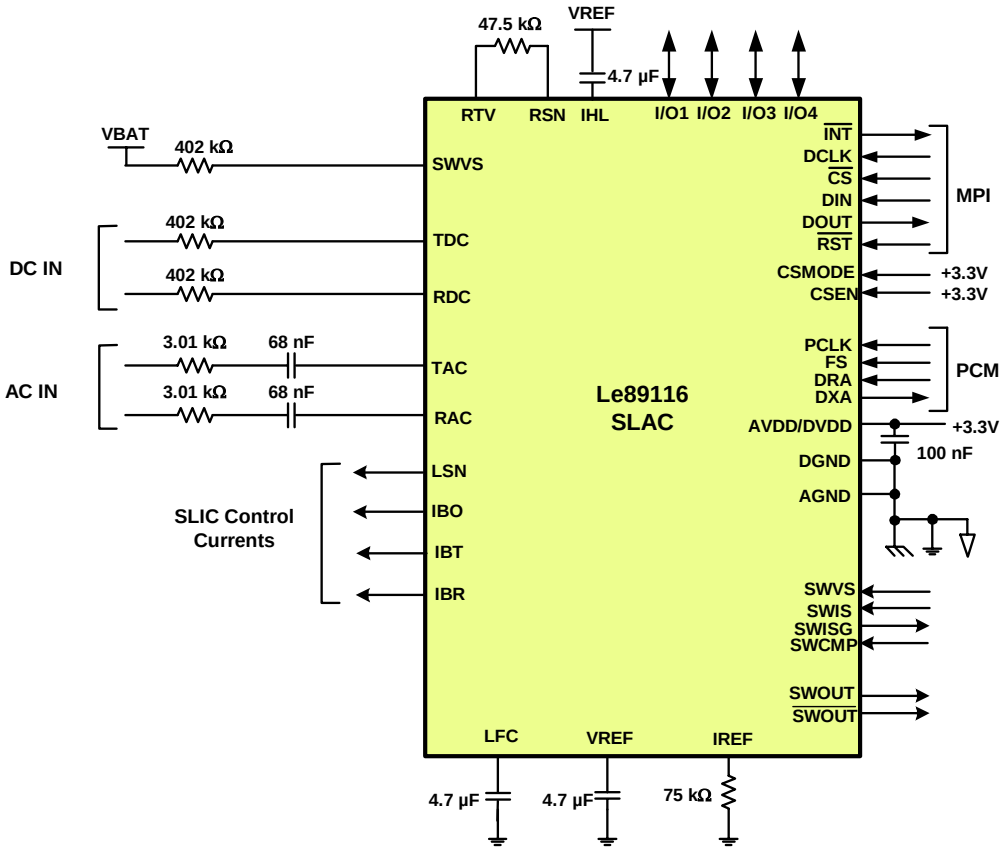
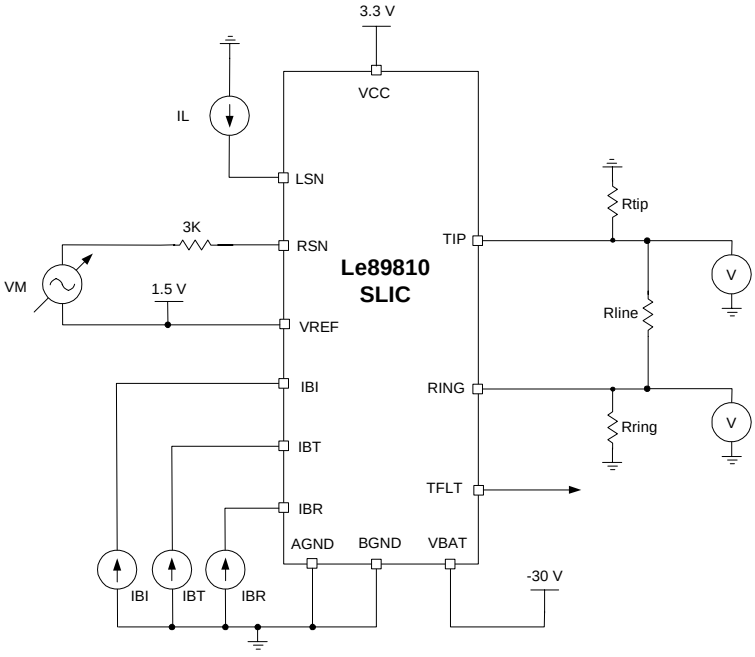


Figure 23. SLIC Test Circuit



5.3.1 Supply Currents and Power Dissipation – Le89810 SLIC

Le89810 Line State	Condition	I_{CC} mA	I_{BAT} mA (Note 1)	Package Power mW (Note 2)	Note
		Typ	Typ	Typ	
Shutdown	Power-up condition with switcher off	0.1	0.0	0.3	3.
Disconnect	Switcher on, but no DC feed to the line	0.8	0.12	9.5	
Low Power Standby (On-Hook / Idle)	Switcher on with limited feed to the line	1.7	0.3	23	
Standby (On-Hook / Idle)		1.7	0.8	51	
OHT or OHT Pol. Rev.		3.1	1.7	107	
Talk (Off-Hook)		3.2	27.8	436	
Ringing	C1 (65 V_{RMS} into 3 REN)	6.1	26	958	4.
	C2 (50 V_{RMS} into 5 REN)	5.1	32	952	4.

Notes:

1. *Measured output of switching regulator feeding into VBAT pin*
2. *Package power dissipation does not include power delivered to the load*
3. *Shutdown is a device state and not a VP API-II line state*
4. *Ringing signal must be cadenced to produce an average power that can be handled by the SLIC package*

5.3.2 Supply Currents and Power Dissipation - Le89116 SLAC

Le89116 Line State	Condition	I_{DD} mA (Note 1)	Package Power mW (Note 2)	Note
		Typ	Typ	
Shutdown	Disconnect, Supplies off	6	20	3., 4.
Disconnect	Disconnect, Supplies on	9.5	31	5.
Low Power Standby (On-Hook / Idle)	Supplies on, On-Hook	10	33	
Standby (On-Hook / Idle)	On-Hook	14	46	
OHT or OHT Pol. Rev.	On-Hook Transmission	25	83	
Talk (Off-Hook)	Off-Hook	25	83	
Ringing	Case C1 or C2	26	86	

Notes:

1. *I_{DD} supply current is the sum of I_{AVDD} and I_{DVDD} for the package*
2. *Package power dissipation does not include power delivered to the load*
3. *Shutdown is the power-up state of the device and not a VP API-II line state*
4. *VBAT supply is off in the Shutdown state*
5. *VBAT supply is active in the FXS Disconnect state*

5.3.3 Le89810 SLIC Loop Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit	Note
On-Hook Characteristics						
Open Circuit Tip to Ring Voltage		-52	-48	-44	V_{DC}	2.
Ringing Voltage Range				92	V_{PK}	1.
Programmed Ringing Voltage Accuracy	R_L = open	-7		+7	%	1.
V_{AB}, Ringing DC offsets	R_L = open, V_{RING} = 0 V	-7		+7	V	1.
Ringing harmonic distortion	Case C1		3	5	%	
Ringing current limit accuracy	R_L = 300 Ω	-10		10	%	1.
Ringing source impedance			200		Ω	1.
AC Ring Trip accuracy	EGBIAS = 0	-15		+15	%	3.
Ring Trip delay	Periods of ringing	1		3	cycles	1.
Ring Frequency Range		15		67	Hz	
Ring Drive	Case C1 ($65V_{RMS}$)			3.0	REN	
	Case C2 ($50V_{RMS}$)			5.0	REN	
Off-Hook Characteristics						
Tip to Ring Line Current, I_{LA}	2 Kft. 26 AWG local loop	20		40	mA	
I_{LA}, Loop-current accuracy, Active state	I_L in constant-current region	-10		+10	%	2.
TDC, RDC input offset current		3.3	3.7	4.1	µA	1.
Switch-hook accuracy		-15% -2mA		+15% +2mA	%	
Switch-hook threshold range	1 mA steps	8		14	mA	

Notes:

1. *This parameter is guaranteed by characterization or correlation to other tests. Typical values not tested in production.*
2. *Calibration is required to achieve these values.*
3. *If the ringing current in the loop is near the current limit more than 50% of the time, a Ring Trip will occur regardless of the average current.*

5.3.4 Le89116 SLAC DC Characteristics

Symbol	Parameter Descriptions	Min	Typ	Max	Unit	Note
V_{IL}	Digital Input Low voltage			0.8	V	
V_{IH}	Digital Input High voltage	2.0				
I_{IL}	Digital Input leakage current	–7		+7	µA	1.
I_{AIL}	Analog input leakage current	–1		+1		
V_{HYS}	Digital Input hysteresis	0.16	0.25	0.34	V	1.
V_{OL}	Digital Output Low voltage I/O_1 (I_{OL} = 50 mA) I/O_{2-4} (I_{OL} = 4 mA) I/O_{2-4} (I_{OL} = 8 mA) Other digital outputs (I_{OL} = 2 mA)			 0.8 0.4 0.8 0.4	V	2.
V_{OH}	Digital Output High voltage I/O_{1-4} (I_{OH} = 4 mA) I/O_{1-4} (I_{OH} = 8 mA) Other digital outputs (I_{OH} = 400 µA)	 V_{CCD} – 0.4 V V_{CCD} – 0.8 V 2.4			V	2.
I_{OL}	Digital Output leakage current (High-Z state) 0 < V < DVDD	 –7		 +7	µA	
V_{REF}	VREF output open circuit voltage	1.43	1.5	1.57	V	
C_{IREF}	IREF pin maximum load capacitance			20	pF	1.
C_I	Digital Input capacitance			10		1.
C_O	Digital Output capacitance			10		1.
$PSRR_1$	AVDD, DVDD Power supply rejection ratio (1.02 kHz, 100 mV_{RMS}, either path, GX = GR = 0 dB)	30			dB	

Notes:

1. *Guaranteed by characterization or correlation to other tests. Typical values are not tested in production.*
2. *The GPIO outputs are resistive for less than a 0.8 V_{DC} drop. Total current must not exceed absolute maximum ratings.*

5.3.5 Switching Regulator Controller

Description	Test Conditions	Min	Typ	Max	Unit	Note
Switcher Input Voltage VSWBB (Buck-Boost Mode)		10	12	16	V_{DC}	
Switcher Input Voltage VSWFL (Flyback Fixed Mode)		4.75	12	8.0	V_{DC}	
Switcher Input Voltage VSWFL (Flyback Tracking Mode)		8.1	12	16	V_{DC}	
SWIS shutdown threshold	Referenced to SWIG		79		mV	
SWIS input bias current		-10		10	µA	
SWIS shutdown delay	V_{SWIS} > 100 mV	12		88	ns	1., 2.
SWCMP output current		-200		200	µA	
SWCMP operating range		0.4		2.6	V	
SWVS to SWCMP gain		0.4		40	V/nA	
SWVS to SWCMP bandwidth		100			kHz	
SWVS input offset current		3.3	3.7	4.1	µA	3.
LFC output impedance			80		kΩ	
SWRV output voltage accuracy	SWRV = -95 V_{DC}	-4		+4	V_{DC}	1.

Notes:

1. *Guaranteed by characterization or correlation to other tests. Typical values are not tested in production*
2. *Time from SWIS exceeding threshold difference from SWISG to SWOUT passing though VDD/2*
3. *Analog input pad leakage can add to this value- see specification under DC Characteristics. Requires ABV calibration*

5.3.6 External Signal Sense Accuracy

Description	Test Conditions	Min	Typ	Max	Unit	Note
Metallic AC coupled voltage		- 4		+ 4	%	1.
Switcher input at SWVS	VBAT = -95 V_{DC}	- 5%		+ 5%	V	1., 2.
Tip voltage to ground	-26 V_{DC} applied between Tip/ Ring and Ground	- 6%		+ 6%	V	1.,2.
Ring voltage to ground		- 6%		+ 6%	V	
Metallic DC line voltage	-1.5 V_{DC} applied to Tip and - 21.5 V_{DC} applied to Ring	- 7%		+ 7%	V	
Metallic loop current	VBAT = -30 V_{DC} , ± 130 µA applied at IM	-1.5 mA - 5%		1.5 mA + 5%	mA	1.
Total longitudinal current		-2.5 mA - 5%		2.5 mA + 5%	mA	1.
Voice DAC (Full loopback)	0 dBm reference signal	-1.0		+1.0	dB	

Notes:

1. *The % limits are defined as the % of the actual voltage on Tip / Ring. The offset and percentage errors are independent and combine as RMS errors.*
2. *This is measured in production by first calibrating offset voltage and applying the listed test voltages on Tip and/or Ring. Accurately measuring smaller voltages requires care in offset calibration.*

5.3.7 FXS Transmission Characteristics - Narrowband Codec Mode

Description	Test Conditions	Min	Typ	Max	Unit	Note
TAC - RAC overload level	Active state, GX = AX = 0 dB	3.4			V_{PK}	1. 2.
Transmit level, A/D	0 dBm, 1014 Hz		0		dBm0	
Receive level, D/A	0 dBm0, 1014 Hz		0		dBm	
Gain accuracy, D/A	0 dBm0, 1014 Hz	–0.5		+0.5	dB	
Gain accuracy, A/D	0 dBm0, 1014 Hz	–0.5		+0.5		
Attenuation distortion	300 to 3000 Hz	–0.25		+0.25		1.
Single frequency distortion				–46		3., 6.
Second harmonic distortion, D-A	GR = 0 dB			–55		6.
Idle channel noise V_{TIPD} - V_{RINGD} DXA, Digital out	DRA, Digital input = 0 A-law, 0 dBr DRA, Digital input = 0 µ-law, 0 dBr V_{TIPD} - V_{RINGD} = 0 VAC A-law, 0 dBr V_{TIPD} - V_{RINGD} = 0 VAC µ-law, 0 dBr			–71 19 –65 19	dBm0p dBrnC0 dBm0p dBrnC0	4. 1., 4. 4. 1., 4.
End-to-end absolute group delay	B = Z = 0; X = R = 1, C/L = 0			678	µs	1., 5.
Two-wire return loss	200 to 3400 Hz	26			dB	1.
Longitudinal to Metallic balance TIP - RING or DXA	200 to 3400 Hz	46			dB	1.
DRA to Longitudinal signal generation	300 to 3400 Hz	40				1.
Longitudinal current capability, TIP or RING	Active state	8.5			mArms	1.
Longitudinal impedance at TIP or RING	0 to 100 Hz		100		Ω/pin	1.

Notes:

1. *This parameter is guaranteed by characterization or correlation to other tests. Typical values not tested in production.*
2. *Overload level is defined when THD = 1%.*
3. *0 dBm0 input signal, 300 to 3400 Hz measurement at any other frequency, 300 Hz to 3400 Hz.*
4. *No single frequency component in the range above 3800 Hz may exceed a level of –55 dBm0.*
5. *The End-to-End Group Delay is the absolute group delay of the echo path with the B Filter turned off.*
6. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*

5.3.8 FXS Transmission Characteristics - Wideband Codec Mode

Description	Test Conditions	Min	Typ	Max	Unit	Note
TAC - RAC overload level	Active state GX = AX = 0 dB	3.4			V_{PK}	1., 2.
Transmit level, A/D	0 dBm, 1014 Hz		0		dBm0	
Receive level, D/A	0 dBm0, 1014 Hz		0		dBm	
Gain accuracy, D/A or A/D	0 dBm0, 1014 Hz	–0.5		+0.5	dB	
Attenuation distortion	100 Hz to 6.0 kHz	–0.25		+0.25		1.
Single frequency distortion	50 Hz to 7.0 kHz			–46		3., 6.
Second harmonic distortion, D-A	GR = 0 dB			–55		6.
Idle channel noise, 7 kHz Flat V_{TIPD} - V_{RINGD} DXA, Digital out	 DRA, Digital input = 0 A-law, 0 dBr DRA, Digital input = 0 µ-law, 0 dBr V_{TIPD} - V_{RINGD} = 0 VAC A-law, 0 dBr V_{TIPD} - V_{RINGD} = 0 VAC µ-law, 0 dBr			 -67 23 -67 23	 dBm0p dBrnC0 dBm0p dBrnC0	 4. 1., 4. 4. 1., 4.
End-to-end absolute group delay	B = Z = 0; X = R = 1, C/L = 0			678	µs	1., 5.
Two-wire return loss	50 to 7000 Hz	20			dB	1.
Longitudinal to Metallic balance TIPD - RINGD or DXA	50 to 7000 Hz	46			dB	1.
DRA to Longitudinal signal generation	300 to 7000 Hz	40				1.
Longitudinal current capability, TIPD or RINGD	Active state	8.5			mArms	1.
Longitudinal impedance at TIPD or RINGD	0 to 100 Hz		100		Ω/pin	1.

Notes:

1. *This parameter is guaranteed by characterization or correlation to other tests. Typical values not tested in production.*
2. *Overload level is defined when THD = 1%.*
3. *0 dBm0 input signal, 50 to 7000 Hz measurement at any other frequency, 50 to 7000 Hz.*
4. *No single frequency component in the range above 7600 Hz may exceed a level of –55 dBm0.*
5. *The End-to-End Group Delay is the absolute group delay of the echo path with the B Filter turned off.*
6. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*

5.4 Typical FXS Transmission Plots

The following graphs illustrate typical VE890 FXS transmission graphs using a W&G PCM-4 tester. The measured responses for 600 ohms and TBR21/ETSI ES 203 021 complex AC impedances both with normal headroom are shown and are compared to the corresponding ITU Q.552 templates.

5.4.1 FXS Return Loss

Figure 24. Two-Wire Return Loss

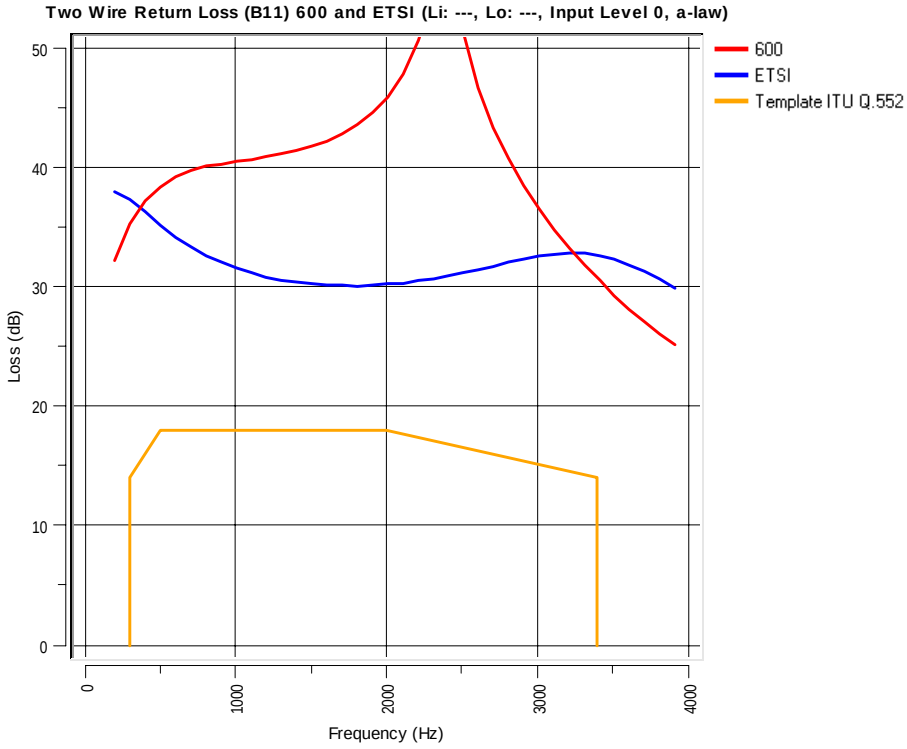
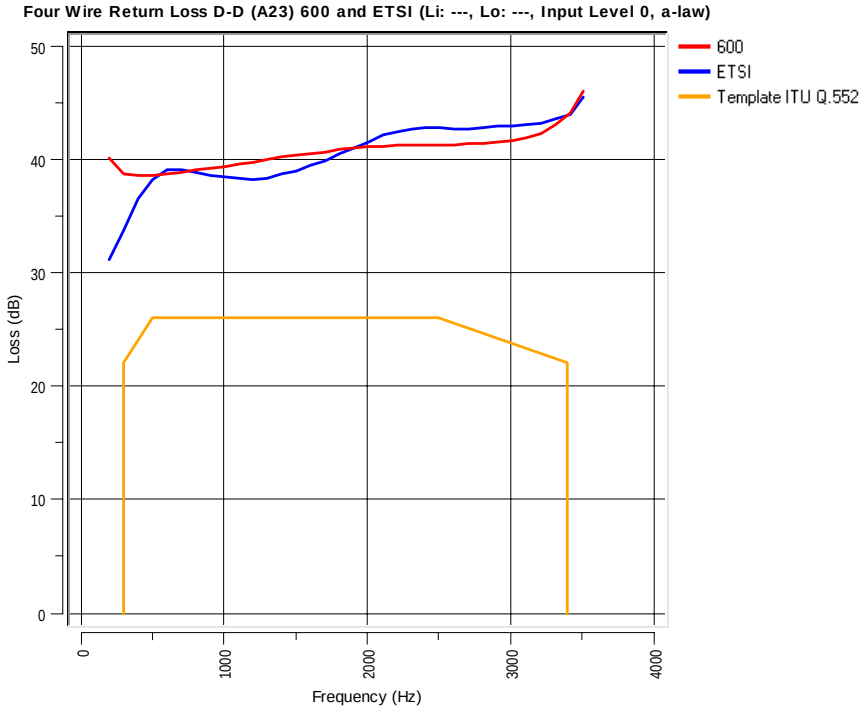


Figure 25. Four-Wire Return Loss



5.4.2 FXS Attenuation Distortion and Gain

Figure 26. Receive Path Attenuation Distortion

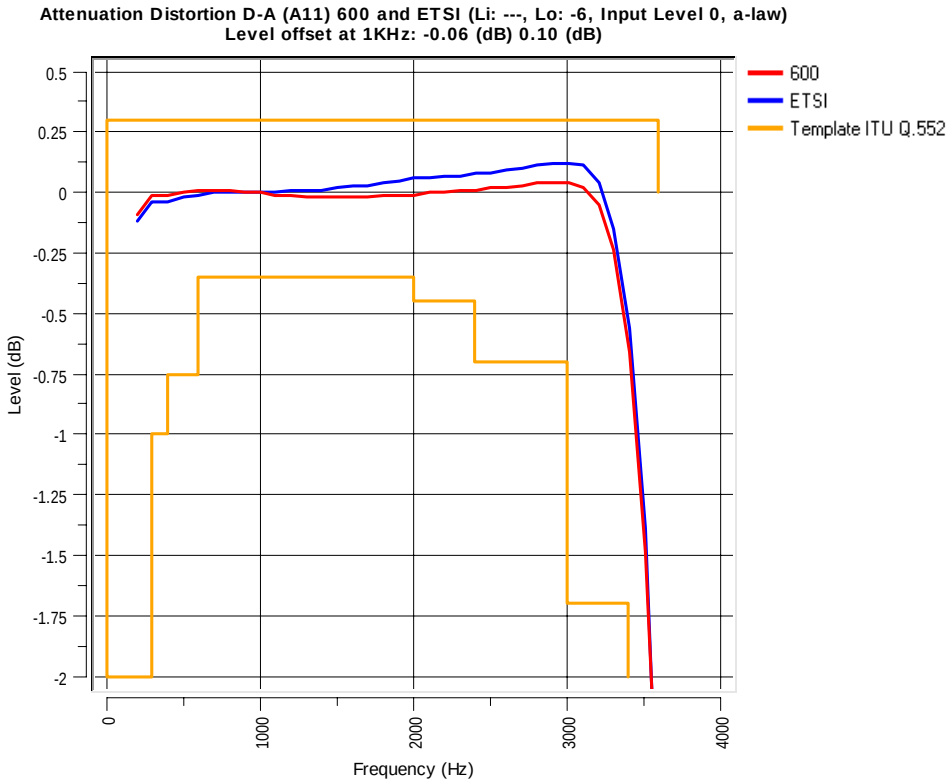
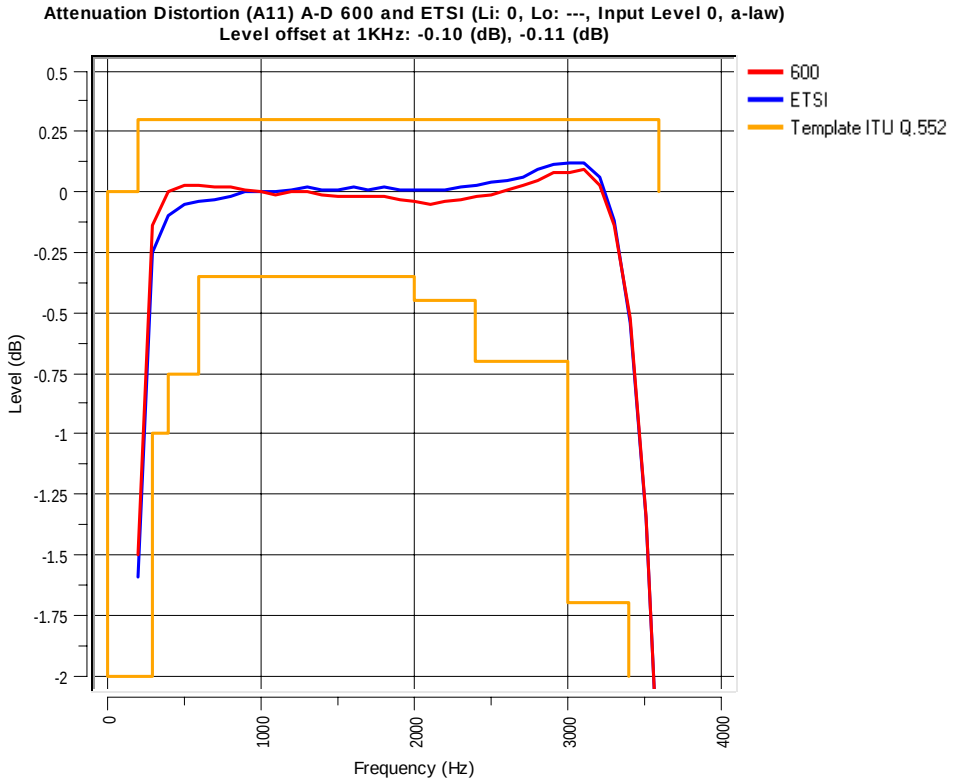


Figure 27. Transmit Path Attenuation Distortion



5.4.3 FXS Gain Tracking and Noise

Figure 28. Receive Path Gain Tracking

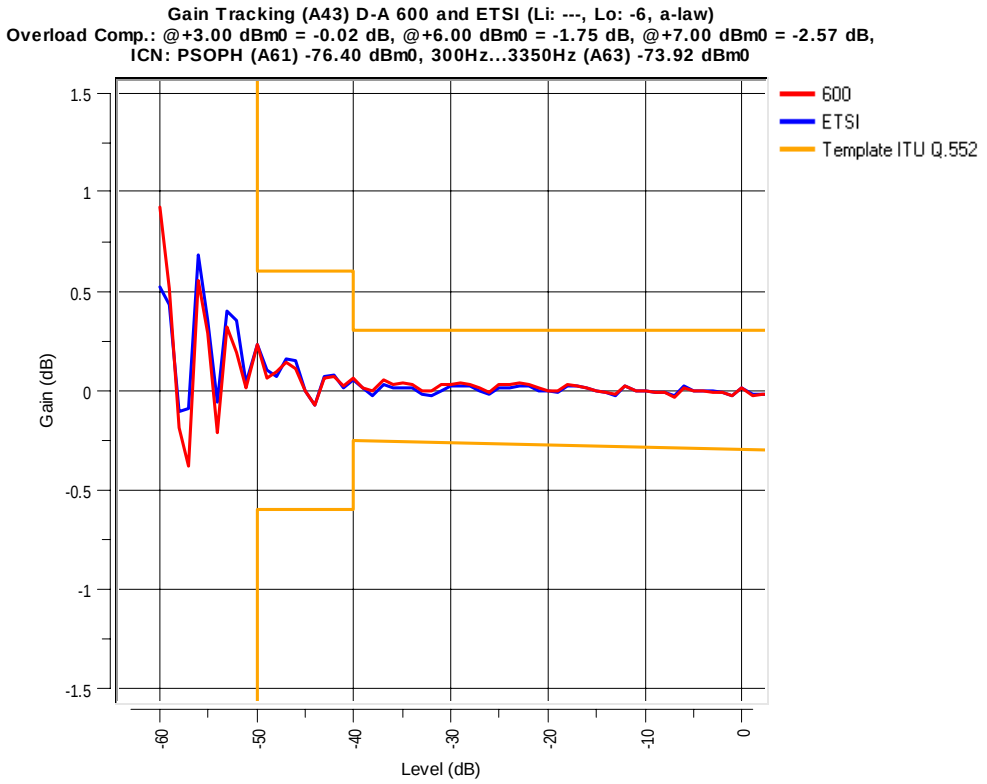
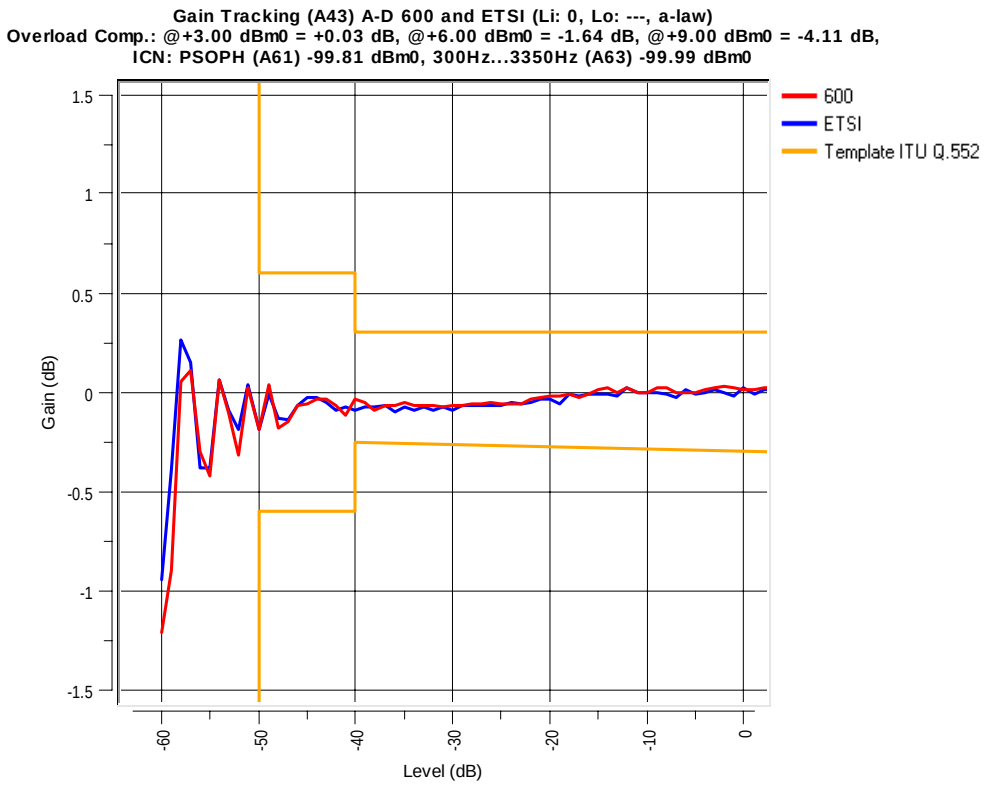


Figure 29. Transmit Path Gain Tracking



5.4.4 FXS Total Distortion and Harmonic Distortion

Figure 30. Receive Path Total Distortion

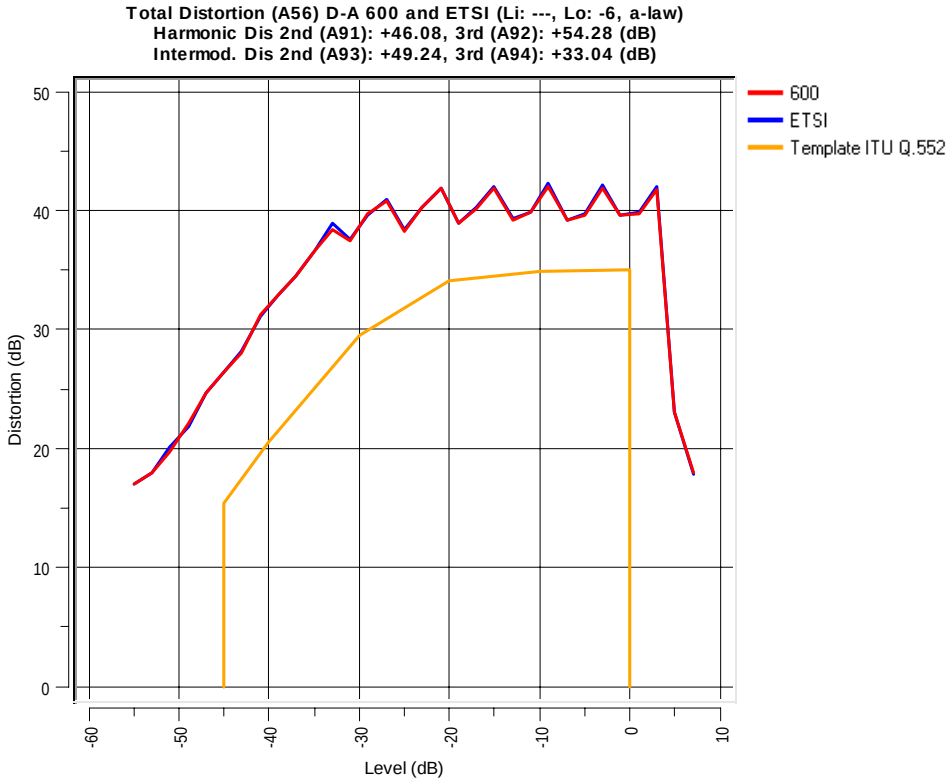
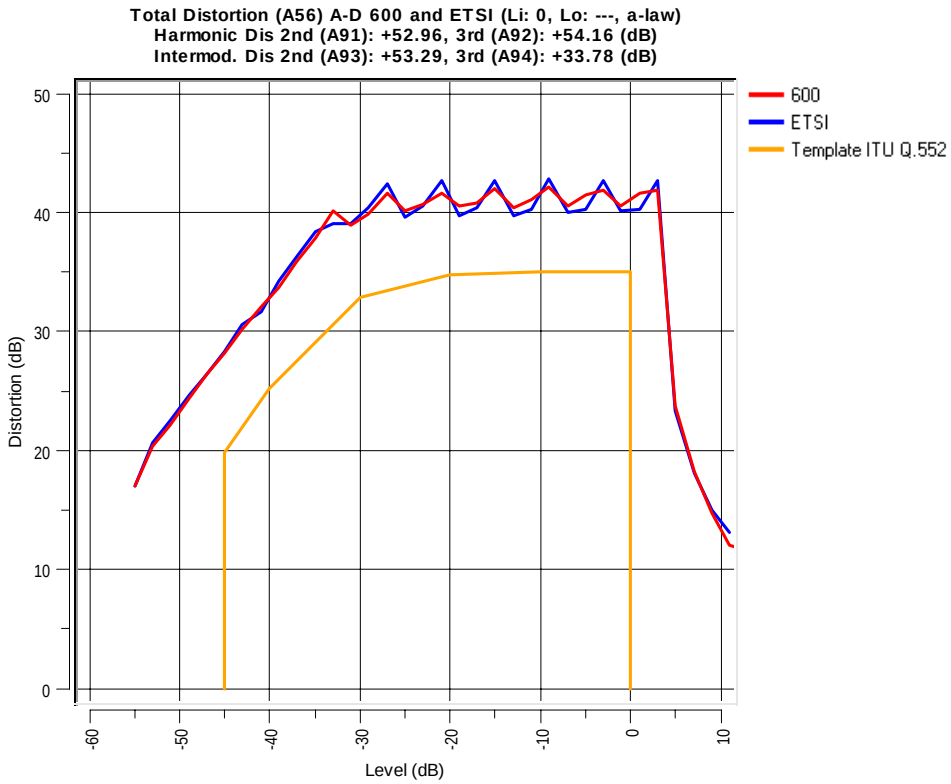
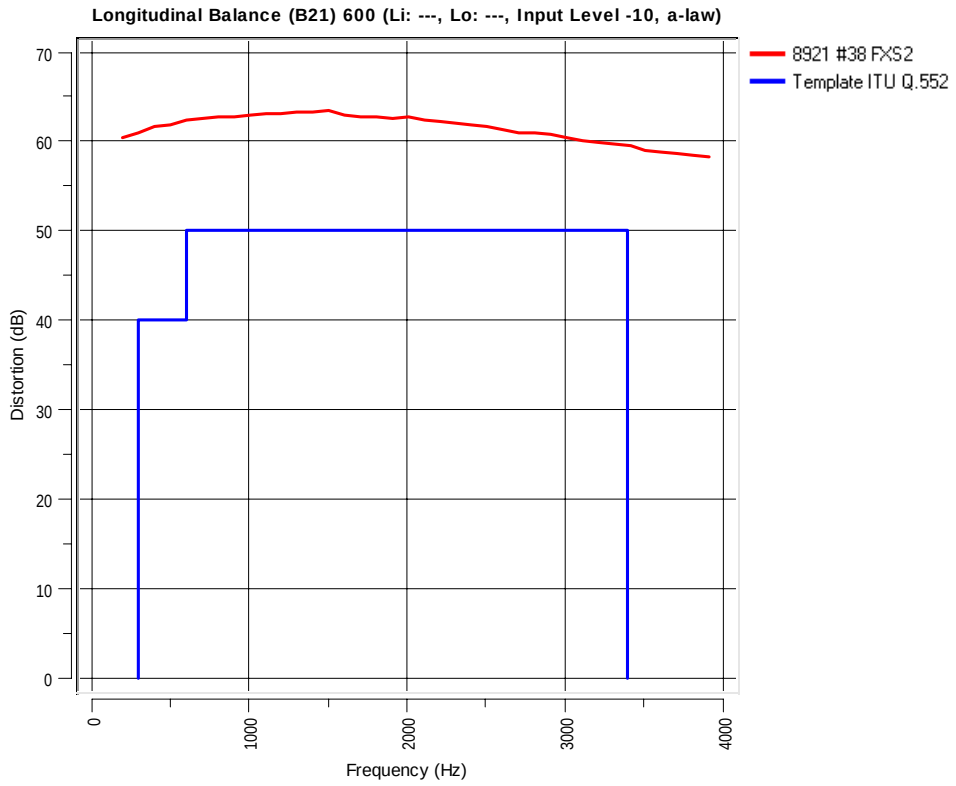


Figure 31. Transmit Path Total Distortion



5.4.5 FXS Longitudinal Balance

Figure 32. Longitudinal Balance



5.5 Switching Characteristics and Waveforms

The following are the switching characteristics over operating range, unless otherwise noted. Minimum and maximum values are valid for all digital outputs with a 115 pF load. (See Figure 33 and Figure 34 for the MPI timing diagrams.)

5.5.1 Microprocessor Interface

No.	Symbol	Parameter	Min	Typ	Max	Unit	Note
1	t_{DCY}	Data clock period	122			ns	
2	t_{DCH}	Data clock HIGH pulse width	48				
3	t_{DCL}	Data clock LOW pulse width	48				
4	t_{DCR}	Rise time of clock			25		
5	t_{DCF}	Fall time of clock			25		
6	t_{ICSS}	Chip select setup time, Input mode	30		t_{DCY} –10		
7	t_{ICSH}	Chip select hold time, Input mode	0		t_{DCH} –20		
8	t_{ICSL}	Chip select pulse width, Input mode		$8t_{DCY}$			
9	t_{ICSO}	Chip select off time, Input mode	2500				
10	t_{IDS}	Input data setup time	25				
11	t_{IDH}	Input data hold time	20				
12	t_{OLH}	I/O1, I/O2 output latch valid			2500		
13	t_{OCSS}	Chip select setup time, Output mode	30		t_{DCY} –10		
14	t_{OCSH}	Chip select hold time, Output mode	0		t_{DCH} –20		
15	t_{OCSL}	Chip select pulse width, Output mode		$8t_{DCY}$			
16	t_{OCSO}	Chip select off time, Output mode	2500				
17	t_{ODD}	Output data turn on delay			50		1.
18	t_{ODH}	Output data hold time	3				2.
19	t_{ODOF}	Output data turn off delay			50		
20	t_{ODC}	Output data valid			50		
21	t_{RST}	Reset pulse width	50			µs	

Notes:

1. *The first data bit is enabled on the falling edge of $\overline{CS}$ or the falling edge of DCLK, whichever occurs last.*
2. *This parameter is guaranteed by characterization or correlation to other tests.Typical values not tested in production.*

Figure 33. Microprocessor Interface (Input Mode)

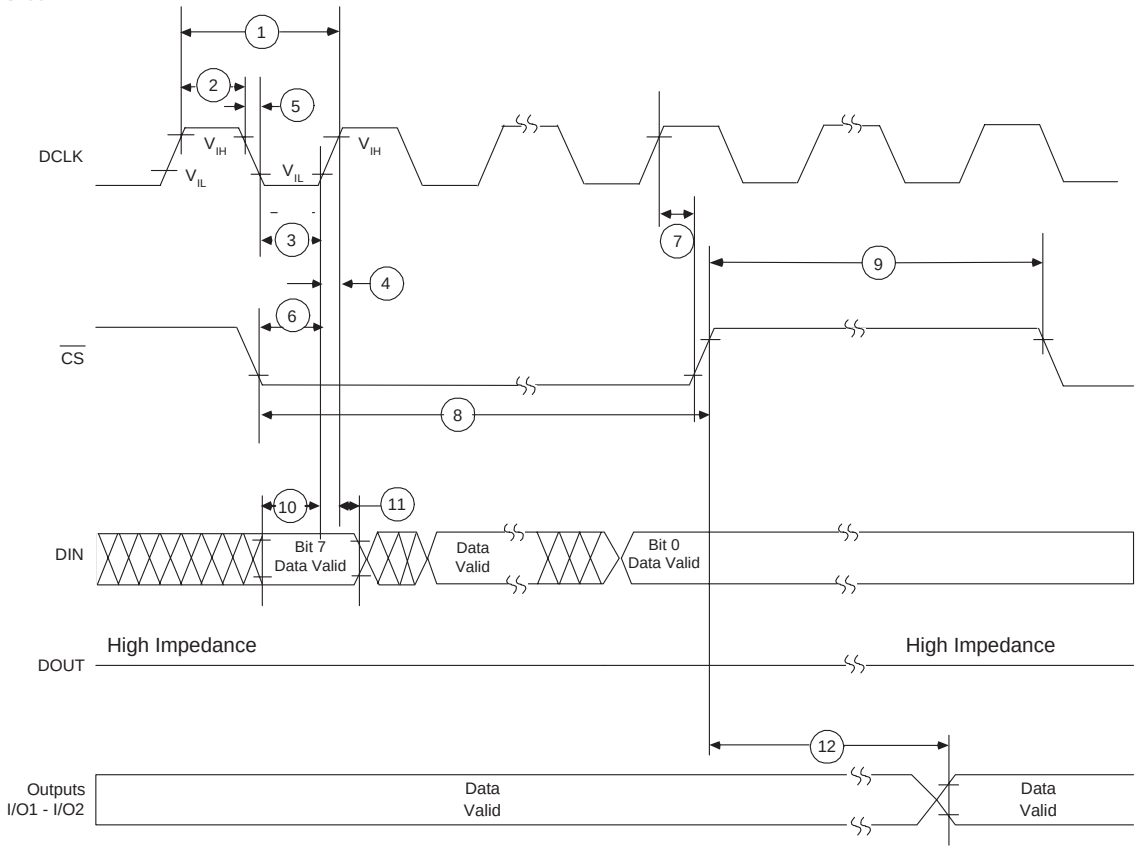
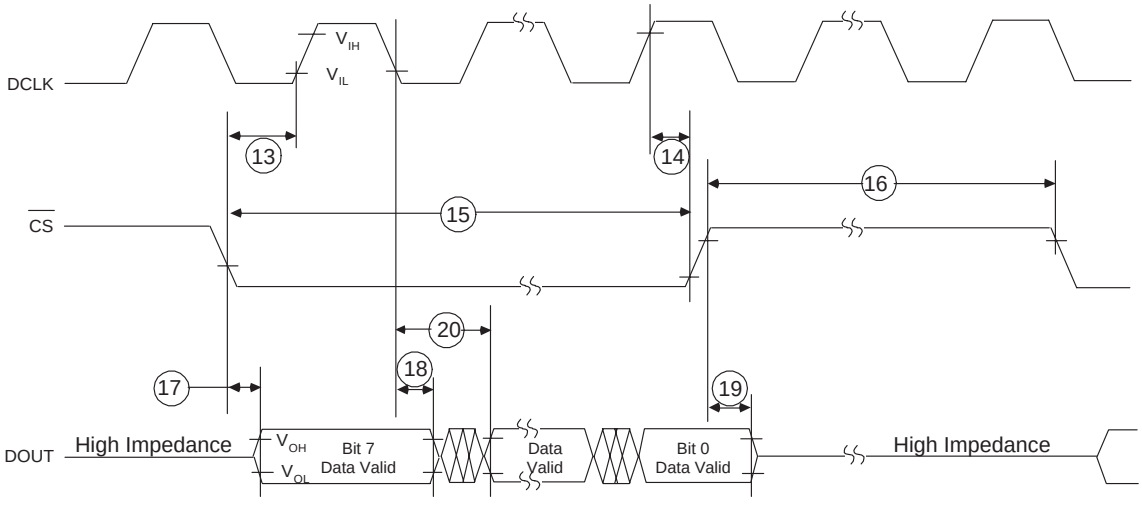


Figure 34. Microprocessor Interface (Output Mode)



5.5.2 PCM Interface

PCLK shall not exceed 8.192 MHz.
(See Figure 1. through Figure 37 for the PCM interface timing diagrams.)

No.	Symbol	Parameter	Min.	Typ	Max	Unit	Note
22	t_{PCY}	PCM Clock (PCLK) period	122		977	ns	1.
23	t_{PCH}	PCLK HIGH pulse width	48				
24	t_{PCL}	PCLK LOW pulse width	48				
25	t_{PCF}	PCLK fall time			15		
26	t_{PCR}	PCLK rise time			15		
27	t_{FSS}	FS setup time	25		t_{PCY}–30		
28	t_{FSH}	FS hold time	50				
29	t_{FST}	Allowed PCLK or FS jitter time - Narrowband	–50		50		1.
29	t_{FST}	Allowed PCLK or FS jitter time - Wideband	–25		25		1.
30	t_{DXD}	PCM data output delay	5		70		
31	t_{DXH}	PCM data output hold time	5		70		
32	t_{DXZ}	PCM data output delay to high Z	10		70		
33	t_{DRS}	PCM data input setup time	25				
34	t_{DRH}	PCM data input hold time	5				

Note:

1. *The PCLK frequency must be an integer multiple of the frame sync (FS) frequency. Frame sync is expected to be an accurate 8 kHz pulse train. The actual PCLK rate depends on the CSEL bit setting in the Chip Configuration register. The minimum frequency is 1.024 MHz and the maximum frequency is 8.192 MHz. If PCLK has jitter, care must be taken to ensure that all setup, hold, and pulse width requirements are met.*

Figure 35. PCM Highway Timing for XE = 0 (Transmit on Negative PCLK Edge)

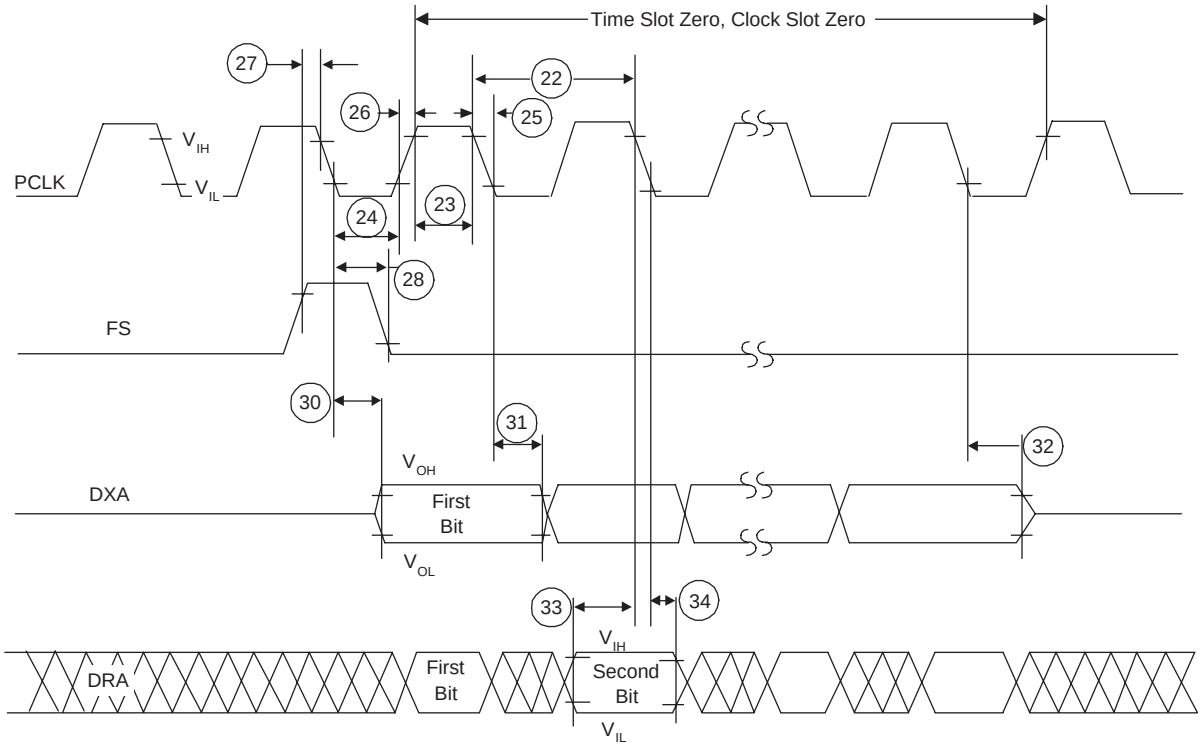


Figure 36. PCM Highway Timing for XE = 1 (Transmit on Positive PCLK Edge)

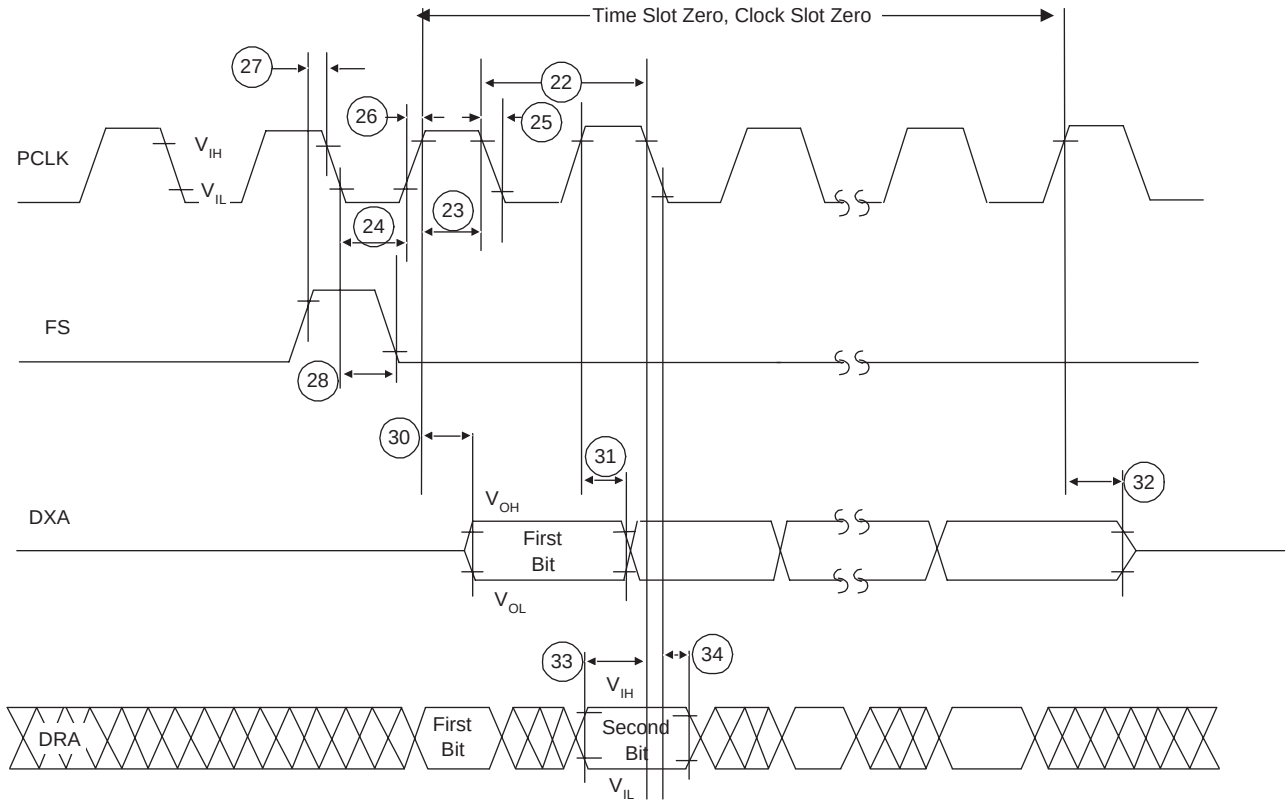


Figure 37. PCM Clock Timing

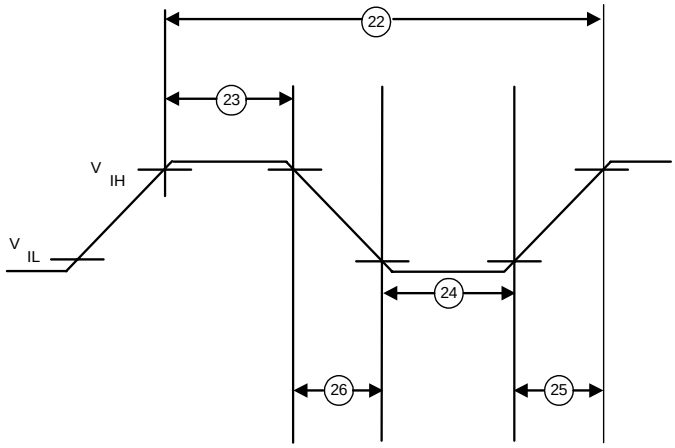
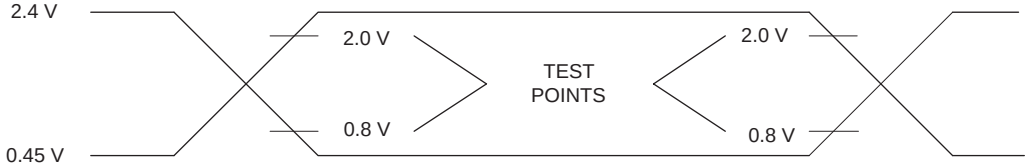


Figure 38. Input and Output Waveforms for AC Tests



5.5.3 Switcher Output Timing

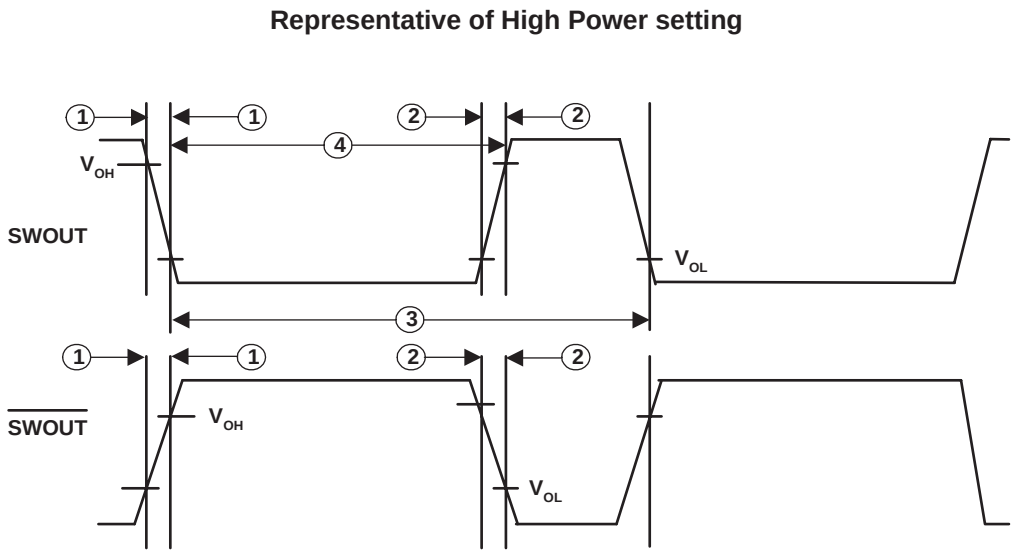
(See Figure 39 for the SWOUT, $\overline{SWOUT}$ timing diagram.)

No.	Symbol	Parameter	Min	Typ	Max	Unit	Notes
1	Tfall	Output Fall Time		30		ns	1., 2.
2	Trise	Output Rise Time		30		ns	1., 2.
3LP	TPeriod	Period for Low Power Mode		41.667		µs	1., 3.
4LP	Tmax	Max On-Time for Low Power Mode		1.830	1.845	µs	1., 4.
3MP	TPeriod	Period for Medium Power Mode		10.417		µs	1., 4.
4MP	Tmax	Max On-Time for Medium Power Mode		1.830	1.845	µs	1., 4.
3HP	TPeriod	Period for High Power Mode		2.604		µs	1., 5.
4HP	Tmax	Max On-Time for High Power Mode		1.830	1.845	µs	1., 5.
	Duty Cycle LP	Duty Cycle Low Power Mode	0		8.8	%	1., 3.
	Duty Cycle MP	Duty Cycle Medium Power Mode	0		17.6	%	1., 4.
	Duty Cycle HP	Duty Cycle High Power Mode	0		70.3	%	1., 5.
		SWISY leading edge blanking period		120		ns	1.

Notes:

1. *Guaranteed by characterization or correlation to other tests. Not tested in production.*
2. *Measured with an RC load on SWOUT or $\overline{SWOUT}$ of 330 pF in series with 180 Ω to ground.*
3. *Switching Regulator Control Register is loaded with low power mode 01h flyback mode settings.*
4. *Switching Regulator Control Register is loaded with medium power mode 02h flyback mode settings.*
5. *Switching Regulator Control Register is loaded with high power mode 03h flyback mode settings.*

Figure 39. Switcher Output Waveforms SWOUT, $\overline{SWOUT}$



6.0 DEVICE DESCRIPTIONS

The pins of the VE8910 chipset devices are listed and described in this section.

6.1 Le89116 FXS Line Audio Controller (SLAC)

Figure 40. Le89116 SLAC Pin Diagram (LQFP-48)

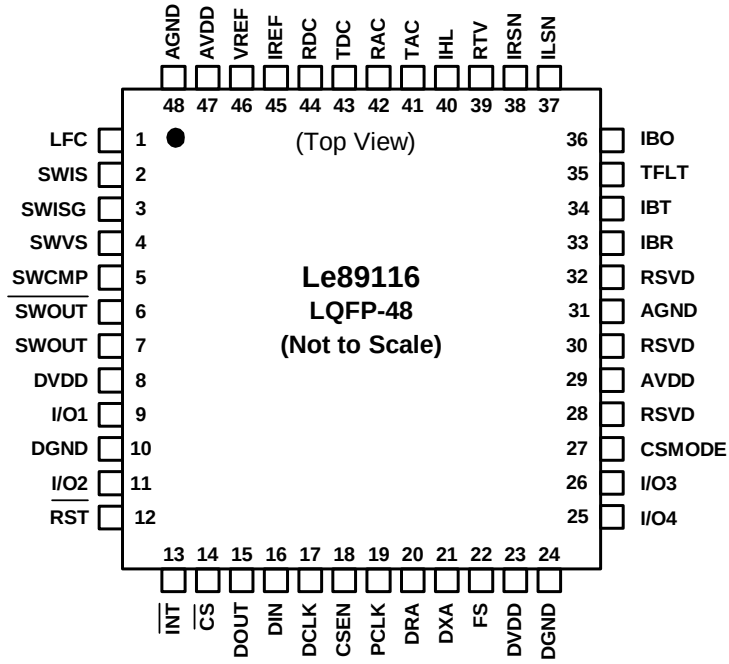


Table 22. Le89116 SLAC Pin Descriptions

Pin	Name	Type	Description
1	LFC	Output	Connection for longitudinal filter capacitor
2	SWIS	Input	Current sense input for switching regulator controller
3	SWISG	Input	Ground reference for switching regulator over current alarm
4	SWVS	Input	Voltage sense for switching regulator controller
5	SWCMP	Output	Compensation connection for switching regulator controller
6	$\overline{\text{SWOUT}}$	Output	Inverted pulse output for gate drive to switching regulator FET
7	SWOUT	Output	Pulse output for gate drive to switching regulator transistor or FET
8	DVDD	Power	Digital power supply input
9	I/O1	I/O	General purpose Input/ Output (Can directly drive a 3.3 V, 150 mW relay; requires an external catch diode across the relay coils)
10	DGND	Power	Digital ground
11	I/O2	I/O	General purpose Input/ Output
12	$\overline{\text{RST}}$	Input	Device hardware reset
13	$\overline{\text{INT}}$	Output	Interrupt
14	$\overline{\text{CS}}$	Input	MPI Chip Select

Table 22. Le89116 SLAC Pin Descriptions (Continued)

Pin	Name	Type	Description
15	DOUT	Output	MPI Data Output
16	DIN	Input	MPI Data Input
17	DCLK	Input	MPI Clock
18	CSEN	Input	Connect to ground for normal mode, used in multiple device mode select
19	PCLK	Input	PCM Clock
20	DRA	Input	PCM Data Receive
21	DXA	Output	PCM Data Transmit
22	FS	Input	PCM Frame Sync
23	DVDD	Power	Digital power supply input
24	DGND	Power	Digital ground
25	I/O4	I/O	General purpose Input/ Output
26	I/O3	I/O	General purpose Input/ Output
27	CSMODE	Input	Mode input for multiple devices
28	RSVD	Open	Reserved. Make no connections to this pin
29	AVDD	Power	Analog power supply input
30	RSVD	Open	Reserved. Make no connections to this pin
31	AGND	Power	Analog ground
32	RSVD	Open	Reserved. Make no connections to this pin
33	IBR	Output	SLIC Ring amplifier current bias
34	IBT	Output	SLIC Tip amplifier current bias
35	TFLT	Input	Thermal fault input
36	IBO	Output	SLIC input stage current bias
37	ILSN	Output	Longitudinal control current output to the SLIC
38	IRSN	Output	Metallic output to SLIC current summing node
39	RTV	Output	Drive output for two-wire AC impedance scaling resistor
40	IHL	Output	Filters DC feed after capacitor
41	TAC	Input	Tip lead AC sense
42	RAC	Input	Ring lead AC sense
43	TDC	Input	Tip lead DC sense
44	RDC	Input	Ring lead DC sense
45	IREF	Input	Current Reference
46	VREF	Output	Analog Voltage Reference
47	AVDD	Power	Analog power supply input
48	AGND	Power	Analog ground

6.2 Le89810 1FXS SLIC Device

Figure 41. Le89810 SLIC Pin Diagram (SOIC-16W)

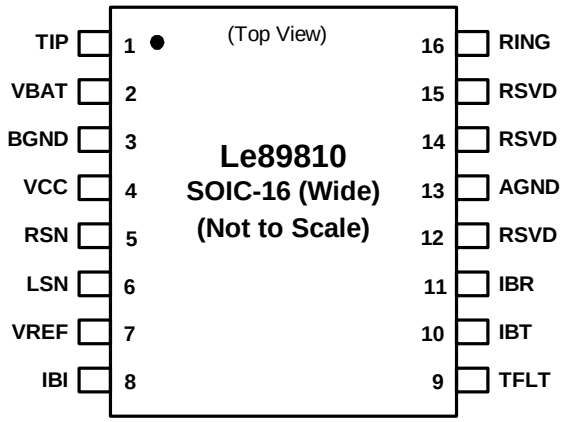


Table 23. Le89810 SLIC Pin Descriptions

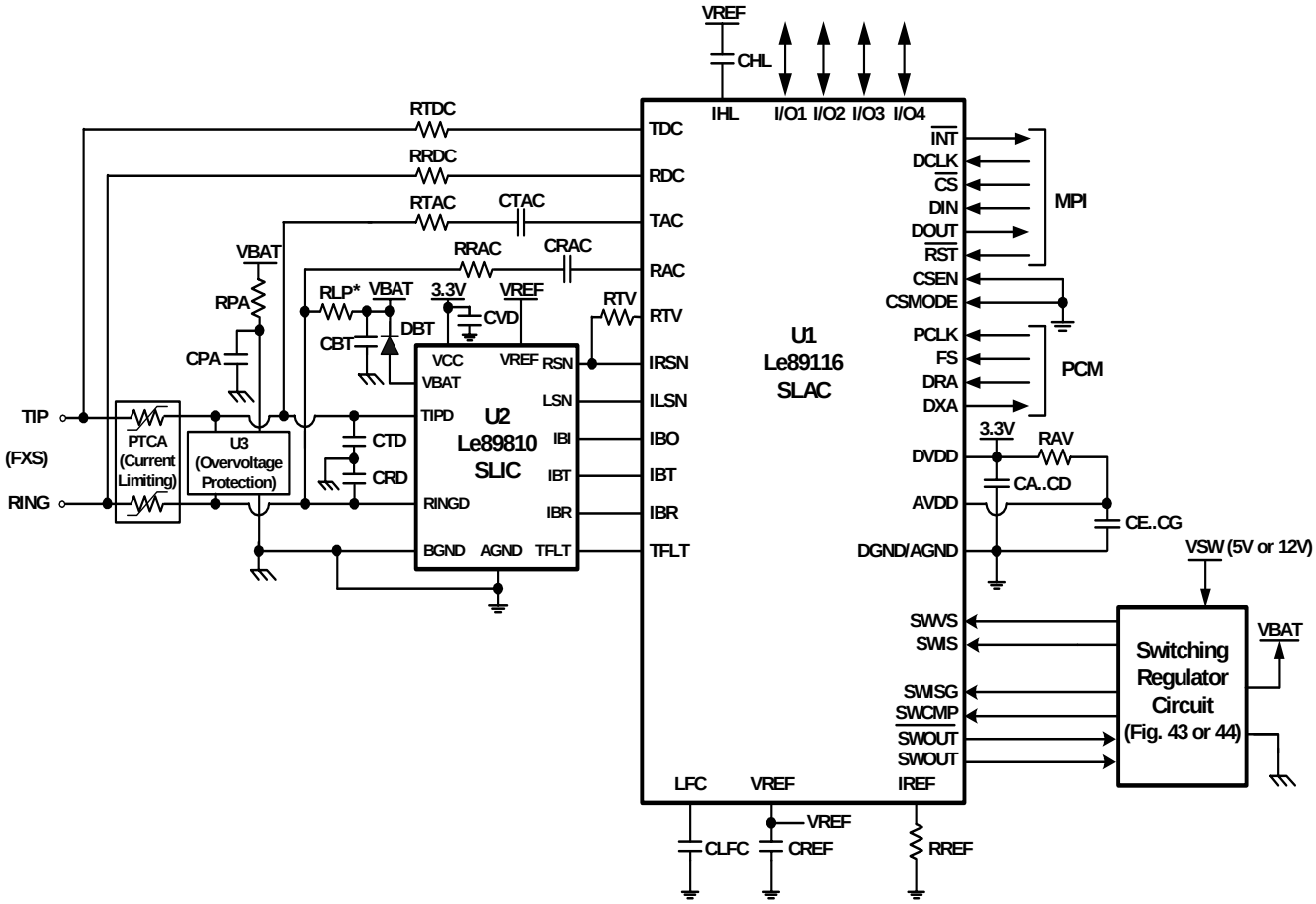
Pin	Name	Type	Description
1	TIP	Output	TIP-lead (A) output to the 2-wire line
2	VBAT	Power	Tracking negative battery supply. Provides power for the line driver
3	BGND	Power	Battery (power) ground
4	VCC	Power	Low voltage power supply
5	RSN	Input	Receive metallic current summing node
6	LSN	Input	Longitudinal current summing node
7	VREF	Power	Buffered reference voltage provided by the Le89116 SLAC device
8	IBI	Input	Input stage bias current
9	TFLT	Output	Thermal Shutdown indicator output
10	IBT	Input	Tip amplifier bias current
11	IBR	Input	Ring amplifier bias current
12	RSVD	Open	Reserved. Make no connections to this pin
13	AGND	Power	Analog ground. Must be shorted with BGND
14	RSVD	Open	Reserved. Make no connections to this pin
15	RSVD	Open	Reserved. Make no connections to this pin
16	RING	Output	RING-lead (B) output to the 2-wire line

7.0 APPLICATIONS

7.1 SLIC and SLAC Application Circuit

Figure 42, on page 49 shows a simplified application circuit with the Le89810 SLIC and the Le89116 SLAC devices. The switching regulator circuit is shown separately. It may be either a buck-boost (Figure 43, on page 51) for lower cost or a flyback (Figure 44, on page 53) for higher efficiency and/or a lower VSW voltage input.

Figure 42. SLIC and SLAC Application Circuit



7.1.1 SLIC and SLAC Application Circuit Bill of Materials

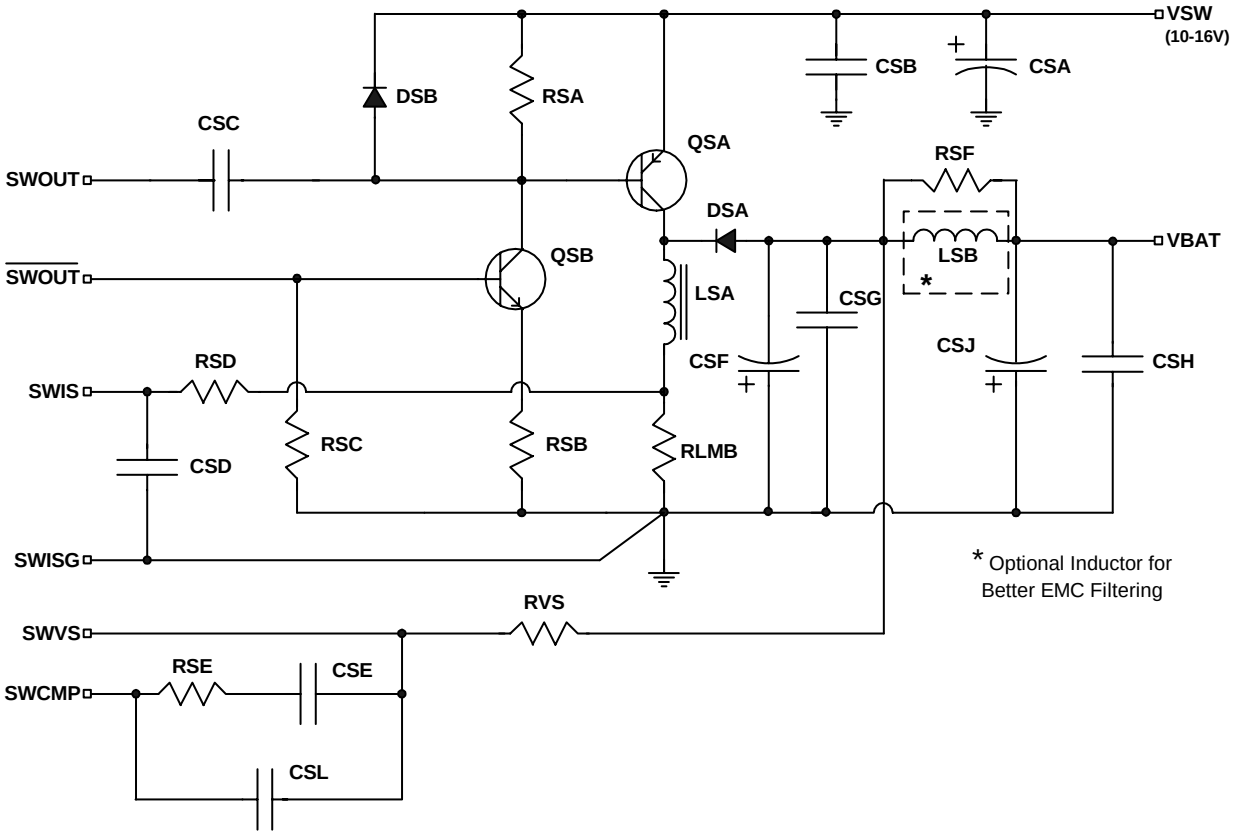
Qty.	Item	Type	Value	Tol.	Rating	Size	Notes
5	CA, CE, CHL, CLFC, CREF	Ceramic Capacitor	4.7 µF, X5R	20%	6.3 V	0603	
5	CB, CC, CF, CG, CVD	Ceramic Capacitor	0.1 µF, X7R	20%	6.3 V	0402	
2	CBT, CPA	Ceramic Capacitor	0.1 µF, X7R	20%	100 V	0805	1.
1	CD	Ceramic Capacitor	0.01 µF, X7R	10%	16 V	0402	
2	CRAC, CTAC	Ceramic Capacitor	0.068 µF, X7R	10%	100 V	1206	1.
2	CRD, CTD	Ceramic Capacitor	0.022 µF, X7R	10%	100 V	0805	1.
1	DBT	Diode	BAS21		0.2 A/ 200 V	SOT-23	
1	PTCA	Dual PTC Thermistor	25 Ω	20%	250 V		2.
1	RAV	Resistor	10 Ω	5%	1/10 W	0603	3.
1	RLP	Resistor	150 KΩ	1%	1/8 W	0805	3.
1	RPA	Resistor	0 KΩ	5%	1/8 W	0805	4.
2	RPT, RPR	Resistor	24.9 Ω	1%	1/4 W	1206	2.
2	RRAC, RTAC	Resistor	3.01 kΩ	1%	1/8 W	0805	
2	RRDC, RTDC	Resistor	402 KΩ	1%	1/4 W	1206	
1	RREF	Resistor	75.0 KΩ	1%	1/10 W	0603	
1	RTV	Resistor	47.5 KΩ	1%	1/10 W	0603	
1	U1	IC, FXS Line Audio Controller (SLAC)	Zarlink Le89116QVC			LQFP-48	
1	U2	IC, Subscriber Line Interface Circuit (SLIC)	Zarlink Le89810BSC			SOIC-16 (Wide)	
1	U3	IC, Programmable TVS SLIC Protector	ST LCP1531RL or Bourns TISP61089BD			SOIC-8	5.

Notes:

1. *Upgrade to 200 V-rated capacitors if VBAT is greater than 75 V_{DC} (i.e. ringing voltage greater than 50 V_{RMS})*
2. *Populate either PTCA or RPR and RPT, but not both line items. PTCA is recommended for applications requiring 250VAC power cross protection according to standards such as ITU-T K.21 (Basic Level) or Telcordia GR-1089 (Intra-building). Recommended PTCA selections are Semitel SCT250B, Vishay 2381 673 61259, Epcos B59825T1120A062, and Bourns CMF-SD25-10.*
3. *Optional - populate for Low Power Standby support*
4. *Change to 4.7 KΩ if using a full-tracking flyback switcher*
5. *A lower-cost fixed voltage protection solution is available for cost-sensitive applications with a maximum ringing of 50 V_{RMS}. Please consult Zarlink for more details.*

7.2 12 V Inverting Buck-Boost Switching Regulator Circuit Example

Figure 43. 12 V Inverting Buck-Boost Switching Regulator Circuit



7.2.1 Buck-Boost Switching Regulator Circuit Performance

Input Range:	10 to 16 V_{DC}
Supply Efficiency:	The efficiency will vary with load and with input voltage. For a nominal 12 V_{DC} input, the efficiency range is typically 50% to 75% under load
Typical Switcher Input Power (P_{SW}): ($VSW=12V_{DC}$)	Disconnect with supplies on, but no DC feed to line: 14 mW Low Power Standby (Idle/On-Hook): 48 mW Standby (Idle / On-Hook): 108 mW OHT or OHT Pol. Rev.: 270 mW Talk (Off-Hook): I_{LA} = 26 mA, VBAT = -30 V_{DC}, RL = 600 Ω : 1.20 W Ringing, 40 V_{RMS} into a 1 REN load: 1.09 W Ringing, 50 V_{RMS} into a 5 REN load (case C2): 3.58 W
Output Regulation (Versus Load):	0.3% with 12 V_{DC} input, 95 V_{DC} output load varied from 0 to 30 mA
Output Accuracy:	-4 V_{DC} to +4 V_{DC} from the fixed ringing voltage setting
Output Ripple:	Two components of ripple are present. The peak to peak ripple occurs fundamentally at the switcher frequency and is due to ESR. This component of the output ripple is less than 75 mV peak to peak. An additional component is superimposed on the sawtooth ESR ripple. This component is a very high frequency "spike" signal which has an amplitude of less than 150 mV peak to peak
Operating Frequency:	Disconnect, Low Power Standby and Standby: 24 kHz All other states: 96 kHz

7.2.2 12 V Inverting Buck-Boost Switching Regulator Circuit Bill of Materials

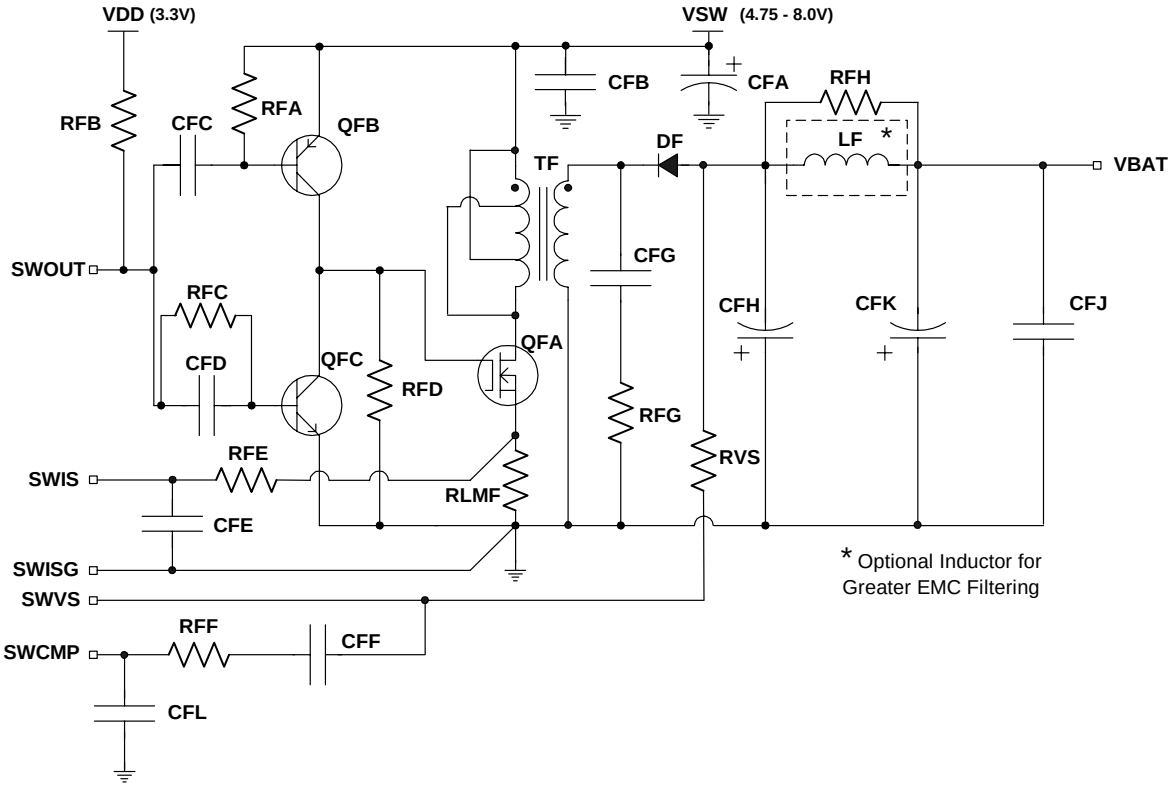
Qty.	Item	Type	Value	Tol.	Rating	Size	Notes
1	CSA	Electrolytic Capacitor	100 µF, Low Impedance, 105 °C	20%	25 V	6.3x11 mm	Panasonic EEU-FC1E101S, Capxon KF101M025E110 or equivalent
1	CSB	Ceramic Capacitor	0.1 µF, X7R	20%	25 V	0603	
1	CSC	Ceramic Capacitor	0.022 µF, X7R	10%	25 V	0402	
1	CSD	Ceramic Capacitor	820 pF, C0G or X7R	10%	16 V	0402	
1	CSE	Ceramic Capacitor	0.033 µF, X7R	10%	16 V	0402	
1	CSF	Electrolytic Capacitor	22 µF, Low Impedance, 105 °C	20%	100 V	8x11.5 mm	1., Panasonic EEU-FC2A220, Capxon GF220M100F115 or equivalent
2	CSG, CSH	Ceramic Capacitor	0.1 µF, X7R	20%	100 V	0805	1.
1	CSJ	Electrolytic Capacitor	0.47 µF, General Purpose, 105 °C	20%	100 V	5x11 mm	1.
1	CSL	Ceramic Capacitor	4.0 pF, C0G	10%	50 V	0402	
1	DSA	Ultra-Fast Recovery Rectifier	ES1D or MURS120		1 A/200 V	SMA	
1	DSB	Diode	LL4148		0.2 A/ 100 V	LL-34	
1	LSA	Inductor	47 µH	20%	2.7 A	12x12x8 mm	Coiltronics DRQ125-470-R, Gotrend GSDRH127PT-470M or equivalent
1	LSB	Inductor	470 µH	20%	> 60 mA	1007 or 1210	2., Taiyo Yuden CBC2518T471M or equivalent
1	QSA	PNP Power Transistor	Diodes ZXTP2013G or DZT953-13		-5 A/- 100 V	SOT-223	3.
1	QSB	NPN Transistor	MMBT3904		0.2 A/40 V	SOT-23	
1	RLMB	Current Sense Resistor	0.030 Ω	1 or 2%	1/2 W	1206 or 2010	Susumu RL1632T-R030-G, Vishay WSL1206R0300FEA18 or equivalent
1	RSA	Resistor	200 Ω	5%	1/10 W	0603	
1	RSB	Resistor	150 Ω	5%	1/10 W	0603	
1	RSC	Resistor	100 KΩ	5%	1/10 W	0603	
1	RSD	Resistor	1.0 KΩ	5%	1/10 W	0603	
1	RSE	Resistor	1.0 MΩ	5%	1/10 W	0603	
1	RSF	Resistor	20 Ω	5%	1/4 W	1206	2.
1	RVS	Resistor	402 KΩ	1%	1/8 W	0805	

Notes:

1. *Capacitor ratings shown for VBAT under 75 V_{DC}. Upgrade to 160 V-rated devices if VBAT is greater than 75 V_{DC} (i.e. ring voltage greater than 50 V_{RMS})*
2. *Populate either LSB or RSF, but not both. Use LSB if better EMC filtering is required.*
3. *Upgrade to Diodes ZXTP2014G or UTC UP1855L if VBAT is greater than 75 V_{DC} (i.e. ring voltage greater than 50 V_{RMS})*

7.3 5 V Flyback Fixed Tracking Switching Regulator Circuit Example

Figure 44. 5 V Flyback Switching Regulator Circuit Example (Fixed Tracking)



7.3.1 Flyback Switching Regulator Performance

Input Range: 4.75 to 8.0 V_{DC} or 8.1 to 16 V_{DC}

Tracking Type: Fixed tracking for lower cost (CFH and CFK are electrolytic capacitors) and full tracking for greater efficiency (CFH ceramic and CFJ and CFK replaced with a single ceramic capacitor)

Supply Efficiency: The efficiency will vary with load and with input voltage. For a nominal 12 V_{DC} input, the efficiency range is typically 50% in Disconnect and Standby modes and 65% to 80% in other modes.

Typical Switcher Input Power (P_{SW}): ($VSW=5V_{DC}$, Fixed Tracking)

Disconnect with supplies on, but no DC feed to line: 20 mW
Low Power Standby (Idle / On-Hook): 50 mW;
Standby (Idle / On-Hook): 105 mW
OHT or OHT Pol. Rev.: 220 mW
Talk (Off-Hook): I_{LA} = 26 mA, VBAT = -30 V_{DC}, RL = 600 Ω : 1.2 W
Ringing, 65 V_{RMS} into a 3 REN load: 3.8 W

Output Regulation: Versus Load: 0.15 % with 12 V_{DC} input and -95 V_{DC} output load varied from 0 to 30 mA
Versus Input: 0.15 % for input varying from 10 to 16V_{DC} with -55 V_{DC} output and a 2000 Ω load

Output Accuracy: -4 V_{DC} to +4 V_{DC} from the fixed ringing voltage setting

Output Ripple: Two components of ripple are present. The peak ripple occurs fundamentally at the switcher frequency and is due to ESR. This component of the ripple is less than 75 mV peak to peak. An additional component is superimposed on the sawtooth ESR ripple. This component is a very high frequency "spike" signal which has an amplitude of less than 150 mV peak to peak

Operating Frequency: Disconnect, Low Power Standby, and Standby (On-Hook Idle): 24 kHz
On-Hook Transmission and Talk (Off-Hook): 96 kHz
Ringing: 384 kHz

7.3.2 5 V Flyback Fixed Tracking Switching Regulator Circuit Bill of Materials

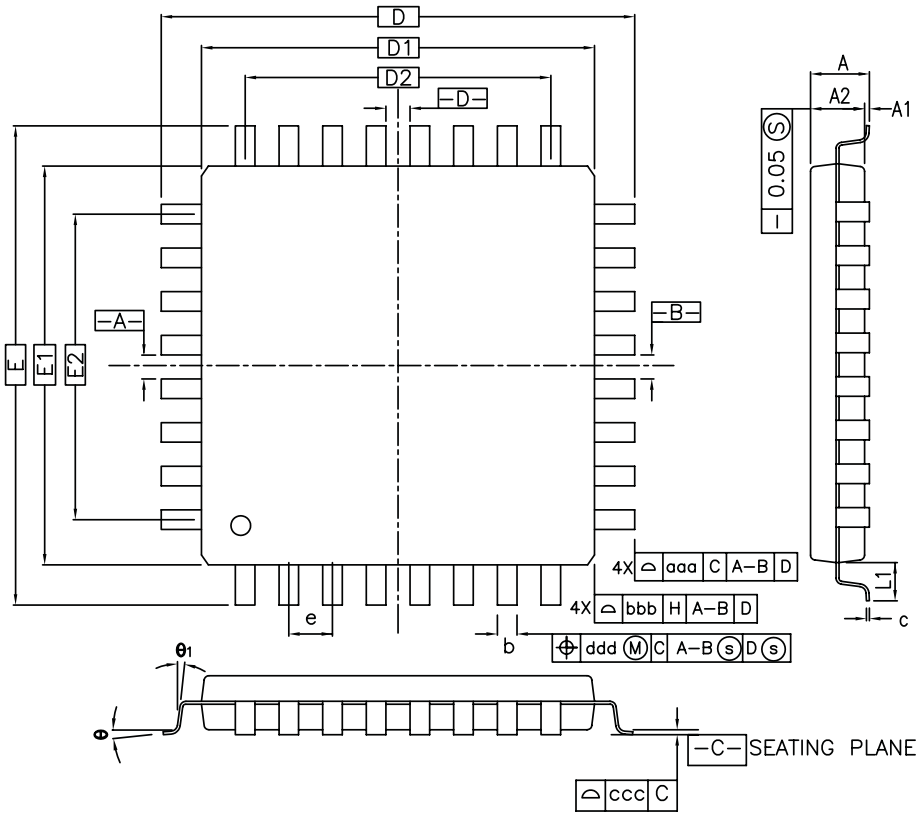
Qty	Item	Type	Value	Tol.	Rating	Size	Notes
1	CFA	Electrolytic Capacitor	100 µF, Low Impedance, 105 °C	20%	16 V	6.3x11 mm	Panasonic EEU-FC1C101, Capxon KF101M025E110, or equivalent
1	CFB	Ceramic Capacitor	0.1 µF, X7R	20%	25 V	0603	
2	CFC, CFD	Ceramic Capacitor	470 pF, C0G or X7R	20%	25 V	0402	
3	CFE	Ceramic Capacitor	220 pF, C0G or X7R	20%	25 V	0402	
1	CFF	Ceramic Capacitor	0.022 µF, X7R	20%	16 V	0402	
1	CFG	Ceramic Capacitor	47 pF, C0G	5%	100 V	0603	1.
1	CFH	Electrolytic Capacitor	22 µF, Low Impedance, 105 °C	20%	100 V	8x11.5 mm	1., 2., Panasonic EEU-FC2A220, Capxon GF220M100F115, or equivalent
1	CFJ	Ceramic Capacitor	0.1 µF, X7R	20%	100 V	0805	1., 2.
1	CFK	Electrolytic Capacitor	0.47 µF, General Purpose, 105 °C	20%	100 V	5x11 mm	1., 2.
1	CFL	Ceramic Capacitor	Do not populate			0402	
1	DF	Ultra-Fast Recovery Rectifier	ES1D or MURS120		1 A/200 V	SMA	
1	LF	Inductor	470 µH	20%	> 60 mA	1007 or 1210	3., Taiyo Yuden CBC2518T471M or equivalent
1	QFA	N-Channel MOSFET	ON Semi NTF3055L108 or Fairchild NDT3055L		3.7 A/60 V	SOT-223	
1	QFB	PNP Transistor	MMBT3906		-0.2 A/-40 V	SOT-23	
1	QFC	NPN Transistor	MMBT3904		0.2 A/40 V	SOT-23	
1	RFA	Resistor	560 Ω	5%	1/10 W	0603	
2	RFB, RFD	Resistor	10 KΩ	5%	1/10 W	0603	
1	RFC	Resistor	2.2 KΩ	5%	1/10 W	0603	
1	RFE	Resistor	1.0 KΩ	5%	1/10 W	0603	
1	RFF	Resistor	1.0 MΩ	5%	1/10 W	0603	
1	RFG	Resistor	1.0 KΩ	5%	1/8 W	0805	
1	RFH	Resistor	20 Ω	5%	1/4 W	1206	3.
1	RLMF	Current Sense Resistor	0.015 Ω	1 or 2%	1/4 W	0805 or 1206	4., Susumu RL1220T-R015-G or equivalent
1	RVS	Resistor	402 KΩ	1%	1/8 W	0805	
1	TF	Flyback Transformer	UMEC TG-UTB1473s or Sumida C8102			12x12x7 m m	4.

Notes:

1. *Capacitor ratings shown for VBAT under 75 V_{DC}. Upgrade to 160V-rated capacitors if VBAT is greater than 75 V_{DC} (i.e. ring voltage greater than 50 V_{RMS})*
2. *Components shown for the fixed tracking version of the flyback switcher circuit. For full tracking operation, CFH should be replaced with a 2.2 uF ceramic capacitor with X7R dielectric and rated for 100 V or higher, such as Kemet C1210C225K1RACTU. Also, replace CFJ and CFK with a single 0.47 uF ceramic capacitor with X7R dielectric and rated for 100 V or higher, such as Taiyo Yuden HMK316B7474KL*
3. *Populate either LF or RFH, but not both. Use LF if better EMC filtering is required.*
4. *BOM component values shown for VSW = 4.75 to 8 V_{DC}. For VSW = 8.1 to 16 V_{DC} ,change RLMF to 0.020 Ω and TF to Sumida C8100 or UMEC TG-UTB01464s if . Also, break the connections between pins 3&4 and 5&6 on the primary side of TF and connect pin 4 to the drain pins of QFA. Please refer to the transformer datasheet for more information.*

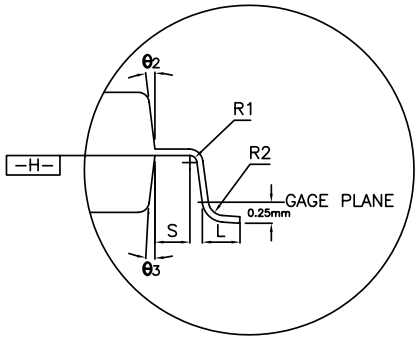
8.0 PACKAGE OUTLINE DRAWINGS

8.1 LQFP-48 Physical Dimensions



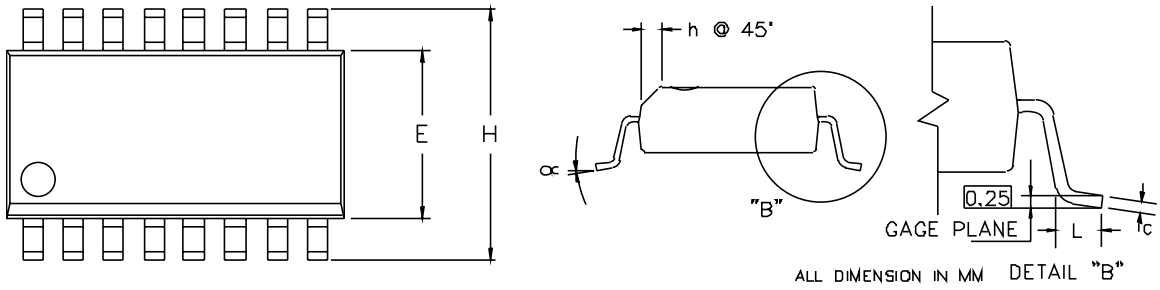
CONTROL DIMENSIONS ARE IN MILLIMETERS.

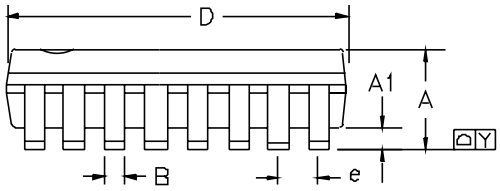
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BSC.			0.354 BSC.		
D1	7.00 BSC.			0.276 BSC.		
E	9.00 BSC.			0.354 BSC.		
E1	7.00 BSC.			0.276 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—



SYMBOL	48L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	5.50			0.217		
E2	5.50			0.217		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

8.2 SOIC-16 (Wide) Physical Dimensions





Small Outline Package (16 SOIC)						
Symbol	Millimeter			Inch		
	Min	Nom	Max	Min	Nom	Max
A	2.35	2.54	2.65	0.092	0.100	0.104
A1	0.10	0.17	0.30	0.004	0.006	0.012
B	0.33	0.42	0.51	0.013	0.016	0.020
C	0.23	0.25	0.32	0.009	0.010	0.012
E	7.40	7.50	7.60	0.291	0.295	0.299
e	1.27 BSC			0.050 BSC		
H	10.00	10.30	10.65	0.394	0.406	0.419
h	0.25	0.50	0.75	0.009	0.020	0.029
L	0.40	0.70	1.27	0.015	0.028	0.050
	0 deg	-	8 deg	0 deg	-	8 deg
Y	0.00		0.01	0.000	-	0.004
D	10.10	10.31	10.50	0.398	0.406	0.413

16-Pin SOIC

Note:

The controlling dimensions are in millimeters.

9.0 ORDERING INFORMATION

OPN	Description	Package Type[1]	Packing
Le89116QVC	SLAC (FX**S** **L**ine **A**udio **C**ontroller)	48-pin LQFP (Green)	Tray[2]
Le89810BSC	SLIC (**S**ubscriber **L**ine **I**nterface **C**ircuit)	16-pin SOIC (Green)	Tube[2]

Notes:

1. *The green packages comply with Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the Restriction of the use of certain Hazardous Substances in electrical and electronic equipment.*
2. *For delivery using a tape and reel packing system, add a "T" suffix to the OPN (Ordering Part Number) when placing an order.*

10.0 RELATED COLLATERAL

10.1 Documentation

- **VE890 Series Product Preview**
  - Document #: 081559
- **VE8901 1FXO Chipset Data Sheet**
  - Document #: 128758
- **VE8911 1FXS + 1FXO Chipset Data Sheet**
  - Document #: 081560
- **VeriVoice™ Test Suite Software Product Preview**
  - Document #: 081535
- **VoicePath™ API-II CSLAC Reference Guide**
  - Document #: 081301
- **Le71HR8921G Reference Design User's Guide**
  - Document #: 129850

10.2 Development Hardware

- **Universal VoicePath Demo Board (UVB) -** OPN: Le71HK0002
  - The Le71HK0002 UVB is a Linux-based development platform for the VE890 Series and other Zarlink voice product families.
- **2FXS + 1FXO Line Module -** OPN: Le71HR8921G
  - The Le71HR8921G Line Module consists of two FXS channels with buck-boost regulators and one DAA channel.
- **2FXS Line Module -** OPN: Le71HR8922G
  - The Le71HR8922G Line Module consists of an isolated FXS channel for dry-loop xDSL applications and a second, non-isolated FXS channel. The isolated FXS channel features a DSL voiceband filter and a flyback regulator while the non-isolated channel can be populated with either an inverting-boost or a flyback regulator. The inverting-boost regulator offers some benefits over traditional buck-boost regulators, such as the one described in this document.

10.3 Software

- **VoicePath™ API-II -** OPN: Le71SK0002
  - The VP API-II is a set of 'C' source code used by the host application to interface to the VE890 Series and other Zarlink voice product families. A signed Software License Agreement (SLA) is required.
- **VoicePath™ API-II Lite -** OPN: Le71SDKAPIL
  - The VP API-II Lite is identical to VP API-II, with reduced functionality. VP API-II Lite does not support cadencing, caller ID, or FXO signal generation (DTMF, Flash Hook, or Dial Pulse). An SLA is not required for VP API-II Lite.
- **VoicePath™ Profile Wizard -** OPN: Le71SDKPRO
  - The VP Profile Wizard is a windows based software program that aids in the organization and creation of country profiles used in the VP API-II into a single project file.
- **VeriVoice™ Auditor Test Suite -** OPN: Le890SLVV
  - The VeriVoice™ Auditor Test Suite for the VE890 Series is a subscriber line (FXS) test software package for VoIP equipment. It features all the outward tests of the Telcordia GR-909 standard and returns pass / fail results. VeriVoice™ Auditor is one of the industry's most cost effective VoIP line testing solution.

- **VeriVoice™ Professional Test Suite -** OPN: Le890SLVVP
  - — The VeriVoice™ Professional Test Suite for the VE890 Series is a super set of the VeriVoice™ Auditor software package providing measured results and greater flexibility. It also features several inward self tests to verify the operation of the FXS subsystem. VeriVoice™ Professional is one of the industry's most complete solution for VoIP line testing and helps reduce the cost of ownership for service providers.
- **UVB Images -** OPN: LE71SDKUVB
  - — The UVB is the latest in Zarlink's hardware platforms designed to provide a demonstration and development vehicle for Zarlink's devices.
- **Zarlink Toolkit -** OPN: LE71SDKTK
  - — The Zarlink Toolkit is a scripting environment that allows for the development and distribution of Tcl related collateral for Zarlink hardware and software products. The Toolkit includes several custom Tcl extension packages, i.e. VP-Script and Mini-PBX.

For more information about all Zarlink products visit our Web Site at:

www.zarlink.com