VCR2N, VCR4N, VCR7N, VCR3P



JFET Voltage Controlled Resistors

The VCR2N, VCR4N, VCR7N, and VCR3P line of JFET voltage controlled resistors utilize the JFET's linear output characteristics in the resistive region. This area of operation is around $V_{DS} = 0$ V and extends for a range up to several hundred millivolts - up to the point ID begins to saturate. Key to device performance is the predictable ros change versus V_{GS} bias where:

$$r_{DS} \text{ bias} \approx \frac{r_{DS} (@V_{GS} = 0)}{1 - \left| \frac{V_{GS}}{V_{GS}(OFF)} \right|}$$

This series features three n-channel devices with $r_{DS(ON)}$ ranging from 20 – 8000 Ω . Also featured is a p-channel device with rDS(ON) specified between 70 and 200 Ω. All packages are hermetically sealed and may be processed per MIL-S-19500. (See Section 1.)

For additional design information please consult typical performance curves (Section 7) as follows:

VCR2N	 NCB
VCR4N	 NPA
VCR7N	 NT
VCR3P	 PSCIA

	V _{GS(OFF)}	V (BR) GSS	r _{ds}	ON)	
PART NUMBER	MAX (V)	MIN (Ω)	MIN (Ω)	MAX (Ω)	
VCR2N	-3.5	-15	20	60	
VCR4N	-7	-15	200	600	
VCR7N	-5	-15	4000	8000	
VCR3P	5	15	70	200	









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2 DRAIN GATE



BOTTOM VIEW

ABSOLUTE MAXIMUM RATINGS ($T_A = 25 \degree$ C unless otherwise noted)

		LIN			
PARAMETERS/TEST CONDITIONS	SYMBOL	VCR2N-7N	VCR3P	UNITS	
Gate-Drain Voltage	V _{GD}	-15	15	v	
Gate-Source Voltage	V _{GS}	-15	-15 15		
Gate Current	۱ _G	10	-10	mA	
Power Dissipation (Case 25°C)	PD	300		mW	
Power Derating		2		mW/°C	
Operating Junction Temperature	Tj	-55 to 175			
Storage Temperature	T _{stg}	-55 to 175		°C	
Lead Temperature (1/16" from case for 10 seconds)	ΤL	300			



VCR2N, VCR4N, VCR7N, VCR3P

N-CHANNEL

ELECTRICAL CHARACTERISTICS 1		LIMITS								
				VCR2N		VCR4N		VCR7N		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP ²	MIN	ΜΑΧ	MIN	мах	MIN	мах	υνιτ
STATIC										
Gate-Source Breakdown Voltage	V _{(BR)GSS}	ا _G = –1 μA, V _{DS} = 0 V	-55	-15		-15		-15		v
Gate-Source Cutoff Voltage	V _{GS(OFF)}	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 1 \mu \text{A}$		-1	-3.5	-3.5	-7	-2.5	-5	
Gate Reverse Current	IGSS	$V_{GS} = -15 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$			-5		-0.2		-0.1	nA
Drain-Source On-Resistance	r _{DS(ON)}	V _{GS} = 0 V, I _D = 1 mA		20	60	200	600	4000	8000	Q
Gate-Source Forward Voltage	V _{GS(F)}	I _G = 1 mA, V _{DS} = 0 V	0.7							v
DYNAMIC										
Drain-Source On-Resistance	r _{ds(ON)}	$V_{GS} = 0 V, I_D = 0 A$ f = 1 kHz		20	60	200	600	4000	8000	Q
Drain-Gate Capacitance	C _{dg}	$V_{GD} = -10 \text{ V}, \text{ I}_{S} = 0 \text{ A}$ f = 1 MHz			7.5		3		1.5	рF
Source-Gate Capacitance	C _{sg}	$V_{GS} = -10 \text{ V}, \text{ I}_{D} = 0 \text{ A}$ f = 1 MHz			7.5		3		1.5	,

P-CHANNEL

ELECTRICAL CHARACT	ERISTICS ¹			LI	мітѕ	
				V	CR3P	
PARAMETER	SYMBOL	TEST CONDITIONS	TYP ²	MIN	МАХ	UNIT
STATIC						
Gate-Source Breakdown Voltage	V _{(BR)GSS}	ا _G = 1 بلA, V _{DS} = 0 V	50	15		
Gate-Source Cutoff Voltage	V _{GS(OFF)}	V _{DS} = -10 V, I _D = -1μA	2.5	1	5	- V
Gate Reverse Current	I _{GSS}	V _{GS} = 15 V, V _{DS} = 0 V	0.005		20	nA
Drain-Source On-Resistance	r _{ds(on)}	V _{GS} = 0 V, I _D = -1 mA	100	70	200	U
Gate-Source Forward Voltage	V _{GS(F)}	I _G = -1 mA, V _{DS} = 0 V	-0.7			v
DYNAMIC						
Drain-Source On-Resistance	r _{ds(ON)}	$V_{GS} = 0 V, I_D = 0 A$ f = 1 kHz	100	70	200	U
Drain-Gate Capacitance	C _{dg}	V_{GD} = 10 V, I _S = 0 A f = 1 MHz	6		25	pF
Source-Gate Capacitance	C _{sg}	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 0 \text{ A}$ f = 1 MHz	6		15	

NOTES: 1. $T_A = 25 \degree C$ unless otherwise noted.

2. For design aid only, not subject to production testing.

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