

# N-Channel 600V (D-S) Power MOSFET

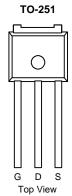
PRODUCT SUMMARY					
V <sub>DS</sub> (V)	600				
$R_{DS(on)}(\Omega)$	V <sub>GS</sub> = 10 V 2.2				
Q <sub>g</sub> (Max.) (nC)	39				
Q <sub>gs</sub> (nC)	10				
Q <sub>gd</sub> (nC)	19				
Configuration	Single				

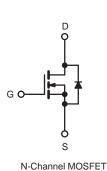
### **FEATURES**

- Ultra Low Gate Charge
- Reduced Gate Drive Requirement
- Enhanced 30 V, V<sub>GS</sub> Rating
- Reduced C<sub>iss</sub>, C<sub>oss</sub>, C<sub>rss</sub>
- Extremely High Frequency Operation
- Repetitive Avalanche Rated
- Compliant to RoHS Directive 2002/95/EC









ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub>	= 25 °C, unl	ess otherwis	se noted)			
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			V <sub>DS</sub>	600	V	
Gate-Source Voltage			$V_{GS}$	± 30	7 v	
Continuous Proin Current	V <sub>GS</sub> at 10 V	$T_{\rm C} = 25 ^{\circ}{\rm C}$ $T_{\rm C} = 100 ^{\circ}{\rm C}$		4		
Continuous Drain Current	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 100 °C	I <sub>D</sub>	2.9	Α	
Pulsed Drain Current <sup>a</sup>			I <sub>DM</sub>	25		
Linear Derating Factor				1.0	W/°C	
Single Pulse Avalanche Energy <sup>b</sup>			E <sub>AS</sub>	530	mJ	
Repetitive Avalanche Current <sup>a</sup>			I <sub>AR</sub>	6.2	Α	
Repetitive Avalanche Energy <sup>a</sup>			E <sub>AR</sub>	13	mJ	
Maximum Power Dissipation T <sub>C</sub> = 25 °C			$P_{D}$	125	W	
Peak Diode Recovery dV/dt <sup>c</sup>			dV/dt	3.0	V/ns	
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 150	°C	
Soldering Recommendations (Peak Temperature) for 10 s			300 <sup>d</sup>			
Mounting Torque	6-32 or M3 screw			10	lbf ⋅ in	
Mounting Torque				1.1	N⋅m	

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11). b.  $V_{DD} = 50$  V, starting  $T_J = 25$  °C, L = 25 mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 6.2$  A (see fig. 12). c.  $I_{SD} \le 6.2$  A, dl/dt  $\le 80$  A/µs,  $V_{DD} \le V_{DS}$ ,  $T_J \le 150$  °C.

- d. 1.6 mm from case.

<sup>\*</sup> Pb containing terminations are not RoHS compliant, exemptions may apply



THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	TYP.	MAX.	UNIT		
Maximum Junction-to-Ambient	R <sub>thJA</sub>	-	62			
Case-to-Sink, Flat, Greased Surface	R <sub>thCS</sub>	0.50	-	°C/W		
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	-	1.0			

PARAMETER	SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	
Static					•	•	
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0$	V, I <sub>D</sub> = 250 μA	600	-	-	V
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference t	o 25 °C, I <sub>D</sub> = 1 mA	-	0.70	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V$	<sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0	-	4.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V	$GS = \pm 20$	-	-	± 100	nA
Zova Cata Valtaga Dvain Cuwant		V <sub>DS</sub> = 60	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V		-	100	μΑ
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 480 V, V	V <sub>DS</sub> = 480 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	500	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 3.7 A <sup>b</sup>	-	2.2	-	Ω
Forward Transconductance	9 <sub>fs</sub>	V <sub>DS</sub> = 10	00 V, I <sub>D</sub> = 3.7 A <sup>b</sup>	3.7	-	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>	V	<sub>GS</sub> = 0 V	-	1100	-	
Output Capacitance	C <sub>oss</sub>	V <sub>I</sub>	os = 25 V	-	140	-	pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1.0 I	1.0 MHz, see fig. 5		15	-	
Total Gate Charge	Qg			-	-	39	
Gate-Source Charge	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V	$V_{GS} = 10 \text{ V}$ $I_D = 4 \text{ A}, V_{DS} = 360 \text{ V},$ see fig. 6 and 13 <sup>b</sup>		-	10	nC
Gate-Drain Charge	Q <sub>gd</sub>		See lig. 6 and 16	-	-	19	1
Turn-On Delay Time	t <sub>d(on)</sub>	$V_{DD}$ = 300 V, $I_D$ = 4 A $R_g$ = 9.1 $\Omega$ , $R_D$ = 47 $\Omega$ , see fig. 10 <sup>b</sup>		-	12	-	ns
Rise Time	t <sub>r</sub>			-	20	-	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	27	-	
Fall Time	t <sub>f</sub>			-	17	-	
Internal Drain Inductance	L <sub>D</sub>	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	
Internal Source Inductance	L <sub>S</sub>			-	7.5	-	nH
Drain-Source Body Diode Characteristic	s				•	•	
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode		-	-	4.0	
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	25	A
Body Diode Voltage	$V_{SD}$	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 4 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	1.5	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	- T <sub>J</sub> = 25 °C, I <sub>F</sub> = 4 A, dl/dt = 100 A/μs b		-	440	680	ns
					0.1	0.0	
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	2.1	3.2	μC

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- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11). b. Pulse width  $\leq$  300 µs; duty cycle  $\leq$  2 %.



### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

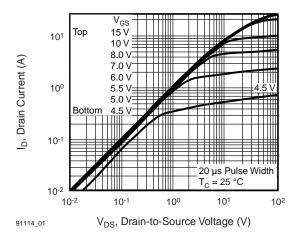


Fig. 1 - Typical Output Characteristics, T<sub>C</sub> = 25 °C

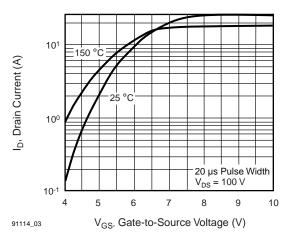


Fig. 3 - Typical Transfer Characteristics

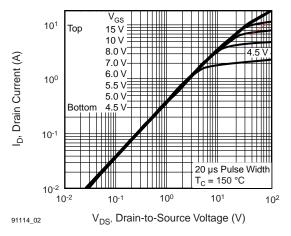


Fig. 2 - Typical Output Characteristics, T<sub>C</sub> = 150 °C

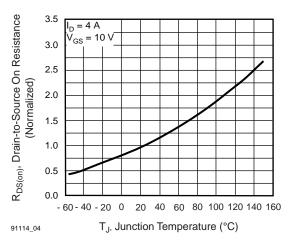


Fig. 4 - Normalized On-Resistance vs. Temperature



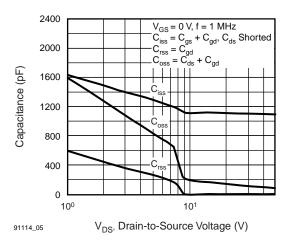


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

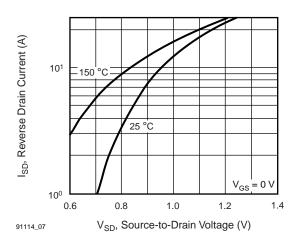


Fig. 7 - Typical Source-Drain Diode Forward Voltage

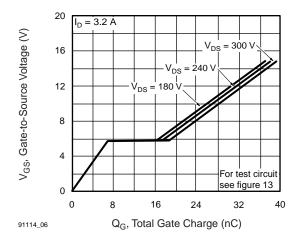


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

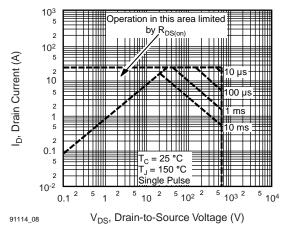


Fig. 8 - Maximum Safe Operating Area



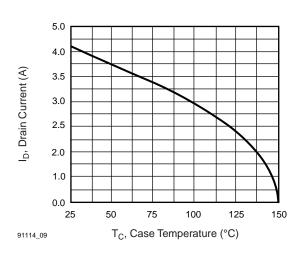


Fig. 9 - Maximum Drain Current vs. Case Temperature

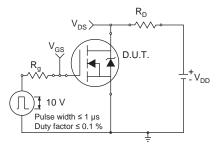


Fig. 10a - Switching Time Test Circuit

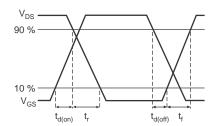


Fig. 10b - Switching Time Waveforms

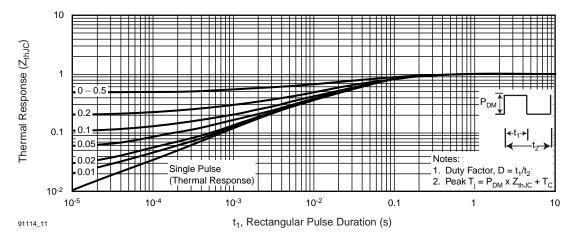
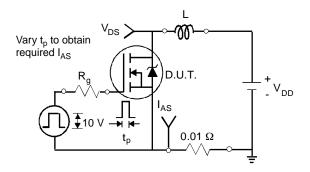
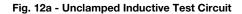


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case







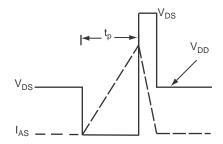


Fig. 12b - Unclamped Inductive Waveforms

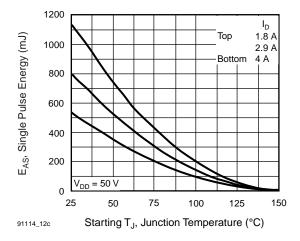


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

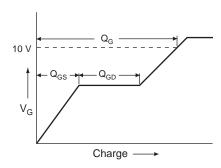


Fig. 13a - Basic Gate Charge Waveform

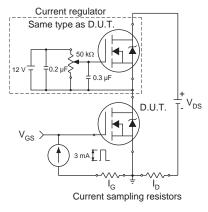
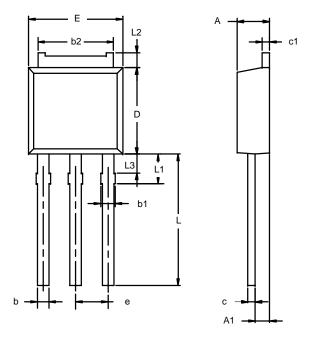


Fig. 13b - Gate Charge Test Circuit



## TO-251AA (DPAK)



Note: Dimension L3 is for reference only.

	MILLIMETERS		INC	HES	
Dim	Min	Max	Min	Max	
Α	2.21	2.38	0.087	0.094	
A1	0.89	1.14	0.035	0.045	
b	0.71	0.89	0.028	0.035	
b1	0.76	1.14	0.030	0.045	
b2	5.23	5.43	0.206	0.214	
С	0.46	0.58	0.018	0.023	
с1	0.46	0.58	0.018	0.023	
D	5.97	6.22	0.235	0.245	
E	6.48	6.73	0.255	0.265	
е	2.28 BSC		0.090 BSC		
L	8.89	9.53	0.350	0.375	
L1	1.91	2.28	0.075	0.090	
L2	0.89	1.27	0.035	0.050	
L3	1.15	1.52	0.045	0.060	
ECN: S-03946—Rev. E, 09-Jul-01 DWG: 5346					

服务热线:400-655-8788

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