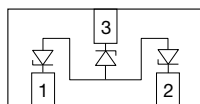
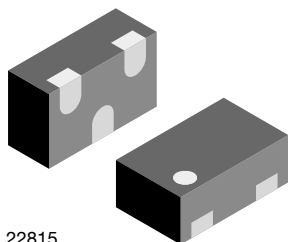


2-Line Low Capacitance, Bidirectional and Symmetrical (BiSy) ESD Protection Diode - Flow Through Design



22814



22815

MARKING (example only)



21121

Bar = cathode marking

X = date code

Y = type code (see table below)

DESIGN SUPPORT TOOLS click logo to get started



FEATURES

- Compact LLP1006-3L package
- Low package height < 0.4 mm
- 2-line ESD protection
- Low leakage current $I_R < 0.1 \mu A$
- Low capacitance: $C_D < 0.4 pF$
- Ideal for high speed data line like
 - HDMI, DisplayPort, eSATA
 - USB, 1394 / firewire
 - Thunderbolt
- ESD immunity acc. IEC 61000-4-2
 - $\pm 20 kV$ contact discharge
 - $\pm 20 kV$ air discharge
- Soldering can be checked by standard vision inspection, no X-ray necessary
- Pin plating NiPdAu (e4) no whisker growth
- e4 - precious metal (e.g. Ag, Au, NiPd, NiPdAu) (no Sn)
- PATENT(S): www.vishay.com/patents
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



ORDERING INFORMATION

DEVICE NAME	ORDERING CODE	TAPED UNITS PER REEL (8 mm TAPE ON 7" REEL)	MINIMUM ORDER QUANTITY
VBUS05M2-HT1	VBUS05M2-HT1-G4-08	8000	8000

PACKAGE DATA

DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS
VBUS05M2-HT1	LLP1006-3L	5	0.72 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	260 °C/10 s at terminals

ABSOLUTE MAXIMUM RATINGS

PARAMETER	TEST CONDITIONS	SYMBOL	VALUE	UNIT
Peak pulse current	Acc. IEC 61000-4-5; $t_P = 8/20 \mu s$; single shot	I_{PPM}	3.6	A
Peak pulse power	Acc. IEC 61000-4-5; $t_P = 8/20 \mu s$; single shot	P_{PP}	65	W
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses	V_{ESD}	± 20	kV
	Air discharge acc. IEC 61000-4-2; 10 pulses		± 20	
Operating temperature	Junction temperature	T_J	-55 to +125	°C
Storage temperature		T_{STG}	-55 to +150	°C

PATENT(S): www.vishay.com/patents

This Vishay product is protected by one or more United States and international patents.

ELECTRICAL CHARACTERISTICS (pin 1 or pin 2 to pin 3; in both directions) ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)						
PARAMETER	TEST CONDITIONS/REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Protection paths	Number of lines which can be protected	$N_{channel}$	-	-	2	lines
Reverse stand-off voltage	Max. reverse working voltage	V_{RWM}	-	-	5.5	V
Reverse voltage	At $I_R = 0.1\text{ }\mu\text{A}$	V_R	5.5	-	-	V
Reverse current	At $V_{RWM} = 5.5\text{ V}$	I_R	-	< 0.001	0.1	μA
Reverse breakdown voltage	At $I_R = 1\text{ mA}$	V_{BR}	7.5	8.5	9.5	V
Reverse clamping voltage	At $I_{PP} = 1\text{ A}$	V_C	-	11	13	V
	At $I_{PP} = I_{PPM} = 3.6\text{ A}$	V_C	-	15	18	V
Clamping voltage	Transmission line pulse (TLP), $t_p = 100\text{ ns}$ $I_{TLP} = 8\text{ A}$	V_{C-TLP}	-	19	-	V
	Transmission line pulse (TLP), $t_p = 100\text{ ns}$ $I_{TLP} = 16\text{ A}$	V_{C-TLP}	-	27	-	V
Dynamic resistance	Transmission line pulse (TLP), $t_p = 100\text{ ns}$	R_{DYN}	-	1	-	Ω
Capacitance	At $V_R = 0\text{ V}$; $f = 1\text{ MHz}$	C_D	-	0.35	0.4	pF
	At $V_R = 3.3\text{ V}$; $f = 1\text{ MHz}$		-	0.35	0.4	pF

APPLICATION NOTE

The VBUS05M2-HT1 is a two-line ESD protection device with a bidirectional and symmetrical (BiSy) breakdown and clamping performance made for application with a voltage working range up to $\pm 5.5\text{ V}$. The high ESD immunity and a very low capacitance makes it usable for high frequency applications like USB2.0, USB3.0, or HDMI.

With the VBUS05M2-HT1 two high speed data lines can be protected against transient voltage signals like ESD (electro static discharge). Connected to the data line (pin 1 and pin 2) and to ground (pin 3) negative transients will be clamped close above the 5.5 V working range.

FLOW THROUGH DESIGN

Modern digital transmission lines can be clocked up to 480 Mbit/s (USB2.0) or 1.65 Gbit/s (HDMI).

At such high data rates the transmission lines like cables or the line traces on the PCBs have to be very homogeneous regarding their surge impedance. This requires well defined trace dimensions as trace width and distance which have to be calculated depending on the requested surge impedance (e.g. $50\text{ }\Omega$) and the PCB material and layer dimensions. Any device connected to the data lines - like ESD protection devices - have to be connected with minimal changes in these trace dimensions and distances.

With the package in the so called “Flow Through Design” this is possible. The lines are running straight along the PCB while the **VBUS05M2-HT1** is placed on top without any via or loops.

SCHEMATIC DIAGRAM

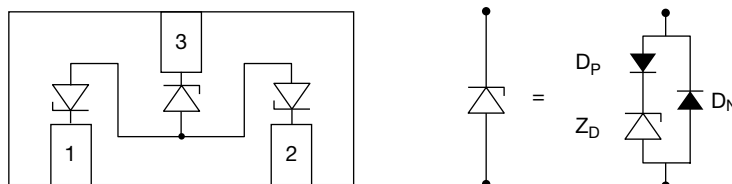


Fig. A

The simplified schematic diagram in Fig. A shows three identical Z-diodes with the cathode on pin 1, 2, or 3 and common anodes. In reality each Z-diode consist of one Z-diode for the adjustment of the breakdown voltage, and two low capacitance switching diodes which provide the low capacitance. Positive transients will be clamped through the switching diode D_P and the Z-diode Z_D while negative transients will be clamped through the switching diode D_N .

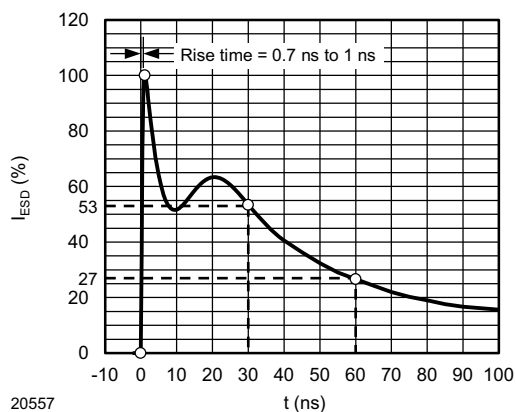
TYPICAL CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)


Fig. 1 - ESD Discharge Current Wave Form
acc. IEC 61000-4-2 (330 Ω /150 pF)

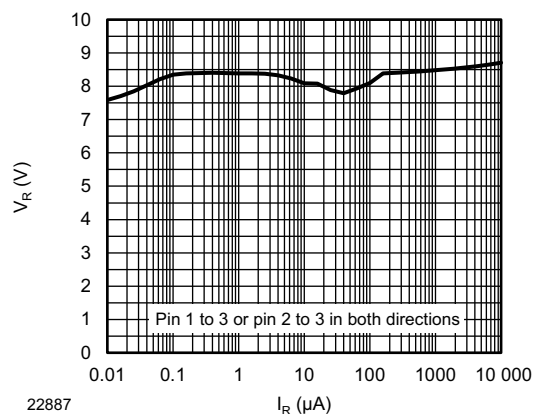


Fig. 4 - Typical Reverse Voltage vs. Reverse Current

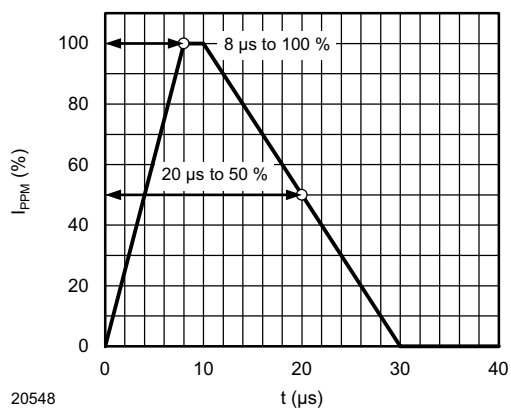


Fig. 2 - 8/20 μs Peak Pulse Current Wave Form
acc. IEC 61000-4-5

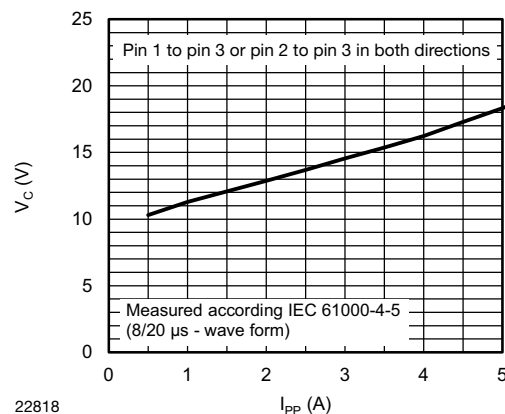


Fig. 5 - Typical Peak Clamping Voltage vs. Peak Pulse Current

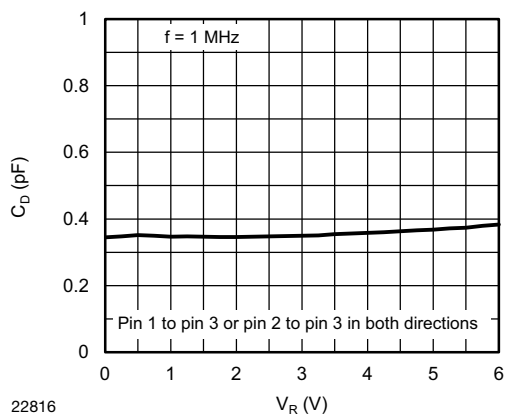


Fig. 3 - Typical Capacitance vs. Reverse Voltage

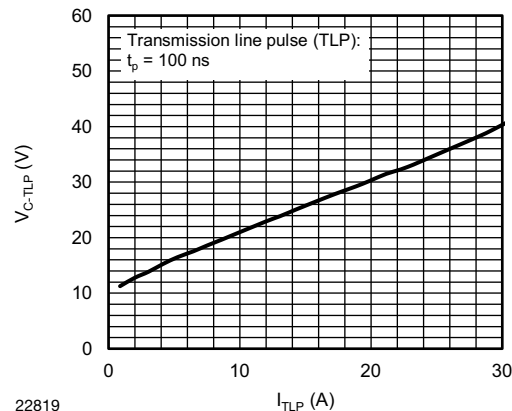
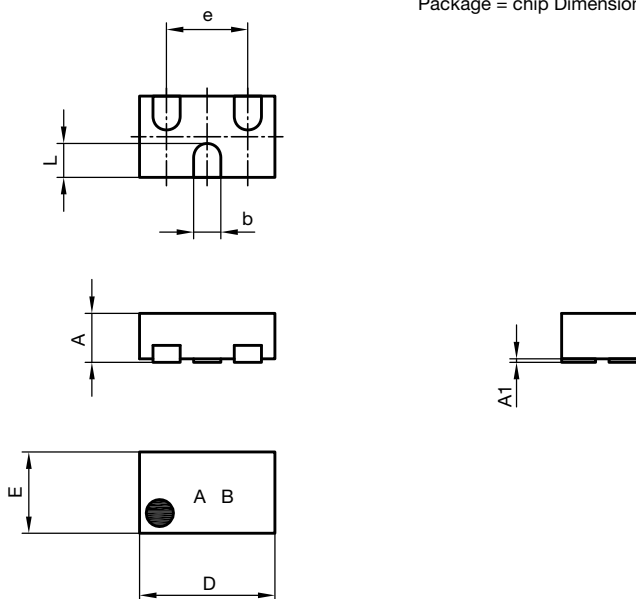


Fig. 6 - Typical Peak Forward Voltage vs. Forward Current

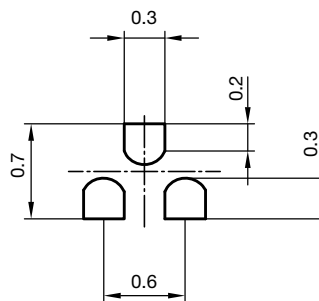
PACKAGE DIMENSIONS in millimeters: **LLP1006-3L**

Package = chip Dimensions in mm



	Millimeters	
	Min.	Max.
D	0.95	1.05
E	0.55	0.65
A	0.33	0.40
A1	0	0.05
b	0.2	
L	0.20	0.30
e	0.6	

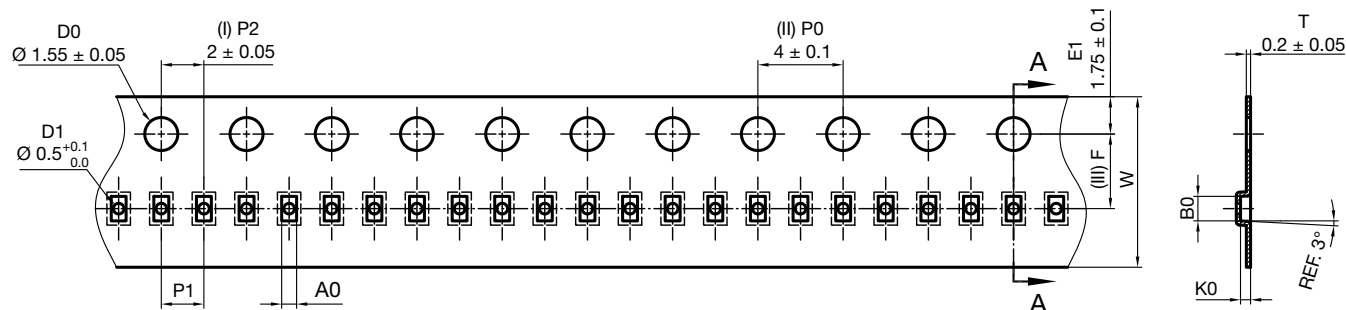
Foot print recommendation:



Document no.:S8-V-3906.04-044 (4)

Created - Date: 03. Sep. 2015

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CARRIER TAPE in millimeters: **LLP1006**

Notes

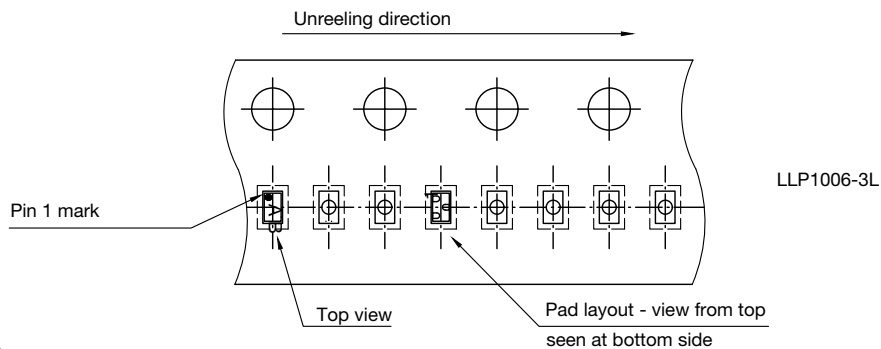
- (I) Measured from centreline of sprocket hole to centreline of pocket
- (II) Cumulative tolerance of 10 sprocket hole is ± 0.20
- (III) Measured from centreline of sprocket hole to centreline of pocket
- (IV) Other material available

	Millimeters
A0	0.70 ± 0.05
B0	1.15 ± 0.05
K0	0.47 ± 0.05
F	3.50 ± 0.05
P1	2.00 ± 0.1
W	8.00 ± 0.1

Doc. no. S8-V-3906.04-016 (3)

Created - Date: 12-Sep-2007

22823

ORIENTATION IN CARRIER TAPE: LLP1006-3L


Doc. no. S8-V-3906.04-017 (4)

Created - Date: 02-May-2017

22821



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