

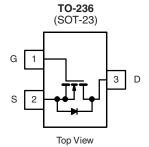
# **Power MOSFET**

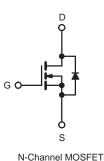
PRODUCT SUMMA	RY		
V <sub>DS</sub> (V)	650	)	
$R_{DS(on)}(\Omega)$	V <sub>GS</sub> = 10 V	8	
Q <sub>g</sub> (Max.) (nC)	18		
Q <sub>gs</sub> (nC)	3.0	)	
Q <sub>gd</sub> (nC)	8.9		
Configuration	Single		

#### **FEATURES**

- Halogen-free According to IEC 61249-2-21 Definition
- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Available in Tape and Reel
- Fast Switching
- Ease of Paralleling
- Compliant to RoHS Directive 2002/95/EC







PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V <sub>DS</sub>	650		
Gate-Source Voltage		$V_{GS}$	± 20	V	
Continuous Drain Current	V <sub>GS</sub> at 10 V	$T_{\rm C} = 25  ^{\circ}{\rm C}$ $T_{\rm C} = 100  ^{\circ}{\rm C}$	1_	1.0	
Continuous Drain Current V <sub>GS</sub> at		T <sub>C</sub> = 100 °C	I <sub>D</sub>	0.7	Α
Pulsed Drain Current <sup>a</sup>		I <sub>DM</sub>	2.0		
Linear Derating Factor			0.33	W/°C	
Linear Derating Factor (PCB Mount) <sup>e</sup>			0.020		
Single Pulse Avalanche Energy <sup>b</sup>			E <sub>AS</sub>	74	mJ
Repetitive Avalanche Currenta		I <sub>AR</sub>	2.0	Α	
Repetitive Avalanche Energy <sup>a</sup>			E <sub>AR</sub>	4.2	mJ
Maximum Power Dissipation	num Power Dissipation $T_C = 25 ^{\circ}C$		Б	42	W
Maximum Power Dissipation (PCB Mount) <sup>e</sup> T <sub>A</sub> = 25 °C		P <sub>D</sub>	2.5	l vv	
Peak Diode Recovery dV/dt <sup>c</sup>		dV/dt	3.0	V/ns	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 150	°C	
Soldering Recommendations (Peak Temperature) for 10 s		_	260 <sup>d</sup>		

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11). b.  $V_{DD} = 50 \text{ V}$ , starting  $T_J = 25 \text{ °C}$ , L = 37 mH,  $R_g = 25 \Omega$ ,  $I_{AS} = 2.0 \text{ A}$  (see fig. 12). c.  $I_{SD} \le 2.0 \text{ A}$ ,  $I_{AS} = 2.0 \text{ A}$ ,  $I_{AS} = 2.0 \text{ A}$  (see fig. 12). d. 1.6 mm from case. e. When mounted on 1" square PCB (FR-4 or G-10 material).

<sup>\*</sup> Pb containing terminations are not RoHS compliant, exemptions may apply



THERMAL RESISTANCE RAT	INGS						
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT		
Maximum Junction-to-Ambient	R <sub>thJA</sub>	-	-	110			
Maximum Junction-to-Ambient (PCB Mount) <sup>a</sup>	R <sub>thJA</sub>	-	-	50	°C/W		
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	-	-	3.0			

#### Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		650	-	-	V
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference	ce to 25 °C, I <sub>D</sub> = 1 mA	-	0.88	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu A$		2.0	-	4.0	V
Gate-Source Leakage	I <sub>GSS</sub>		V <sub>GS</sub> = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V		-	100	
		V <sub>DS</sub> = 480 V	/, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C	-	-	500	μA
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 1.0A <sup>b</sup>	-	8	-	Ω
Forward Transconductance	9 <sub>fs</sub>	V <sub>DS</sub>	= 50 V, I <sub>D</sub> = 1.0 A	1.4	-	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>	$V_{GS} = 0 \text{ V},$ $V_{DS} = -25 \text{ V},$		-	350	-	pF
Output Capacitance	C <sub>oss</sub>			-	48	-	
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1	f = 1.0 MHz, see fig. 5		8.6	-	
Total Gate Charge	Qg			-	-	18	
Gate-Source Charge	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V	$I_D = 1.0 \text{ A}, V_{DS} = 360 \text{ V},$ see fig. 6 and $13^b$	-	-	3.0	nC
Gate-Drain Charge	Q <sub>gd</sub>	1		-	-	8.9	
Turn-On Delay Time	t <sub>d(on)</sub>			-	10	-	
Rise Time	t <sub>r</sub>	$V_{DD}$ = 300 V, $I_{D}$ = 1.0 A, $R_{g}$ = 18 $\Omega$ , $R_{D}$ = 135 $\Omega$ , see fig. 10 <sup>b</sup>		-	23	-	ns
Turn-Off Delay Time	t <sub>d(off)</sub>			-	30	-	
Fall Time	t <sub>f</sub>			-	25	-	
Internal Drain Inductance	L <sub>D</sub>	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	L <sub>S</sub>			-	7.5	-	
<b>Drain-Source Body Diode Characteristic</b>	s						
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode		-	-	2.0	Α
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	8.0	
Body Diode Voltage	$V_{SD}$	$T_J = 25  ^{\circ}\text{C},  I_S = 2.0  \text{A},  V_{GS} = 0  \text{V}^{\text{b}}$		-	-	1.6	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T _ 25 °C I	- 2 0 A dl/dt - 100 A/::ah	-	290	580	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	$-$ T <sub>J</sub> = 25 °C, I <sub>F</sub> = 2.0 A, dl/dt = 100 A/ $\mu$ s <sup>b</sup>		-	0.67	1.3	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic tu	ırn-on time is negligible (turn	-on is dor	ninated b	y L <sub>S</sub> and	L <sub>D</sub> )

#### Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11). b. Pulse width  $\leq$  300 µs; duty cycle  $\leq$  2 %.



#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

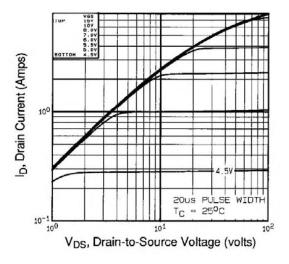


Fig. 1 - Typical Output Characteristics, T<sub>C</sub> = 25 °C

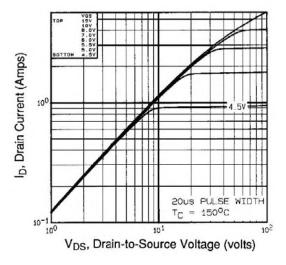


Fig. 2 - Typical Output Characteristics,  $T_C$  = 150 °C

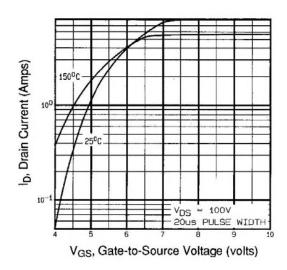


Fig. 3 - Typical Transfer Characteristics

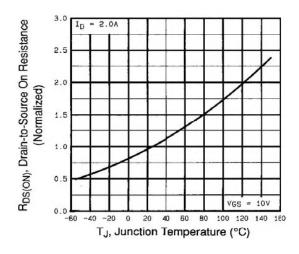


Fig. 4 - Normalized On-Resistance vs. Temperature



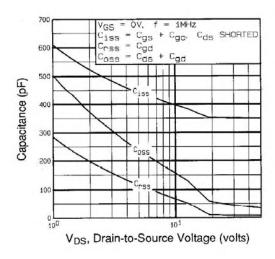


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

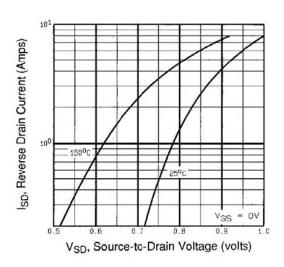


Fig. 7 - Typical Source-Drain Diode Forward Voltage

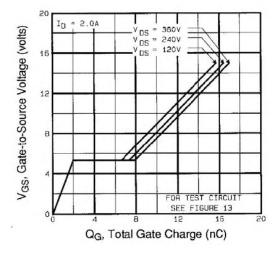


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

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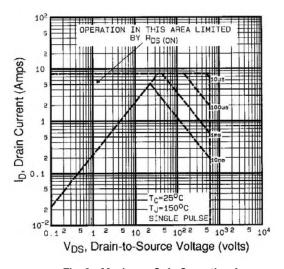


Fig. 8 - Maximum Safe Operating Area



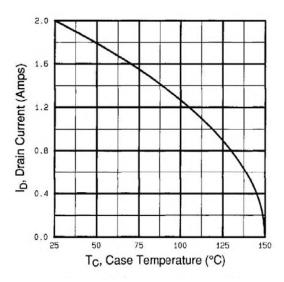


Fig. 9 - Maximum Drain Current vs. Case Temperature

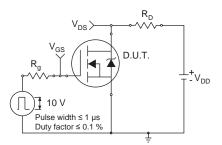


Fig. 10a - Switching Time Test Circuit

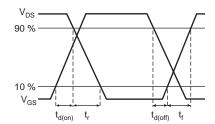


Fig. 10b - Switching Time Waveforms

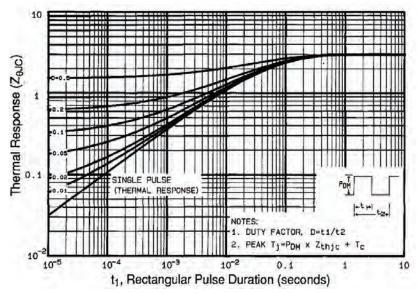


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

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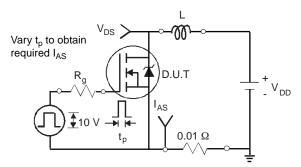


Fig. 12a - Unclamped Inductive Test Circuit

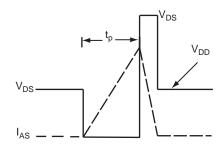


Fig. 12b - Unclamped Inductive Waveforms

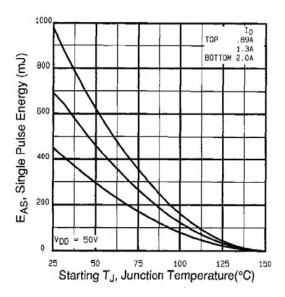


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

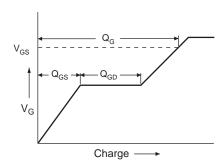


Fig. 13a - Basic Gate Charge Waveform

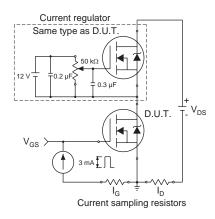
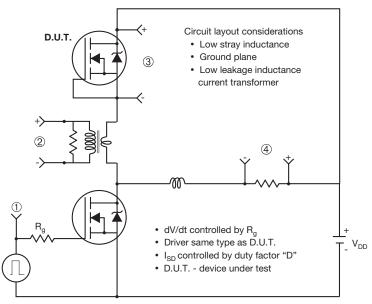


Fig. 13b - Gate Charge Test Circuit



#### Peak Diode Recovery dV/dt Test Circuit



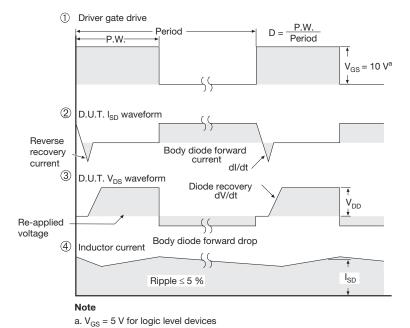
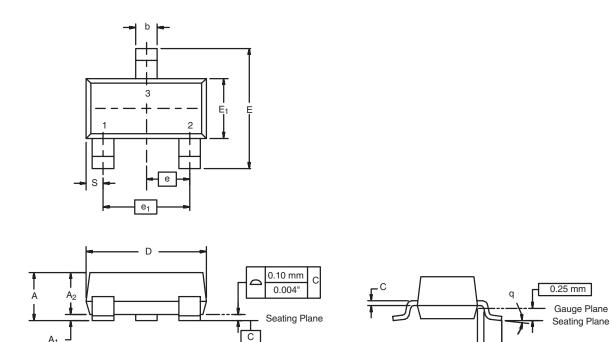


Fig. 14 - For N-Channel



## SOT-23 (TO-236): 3-LEAD



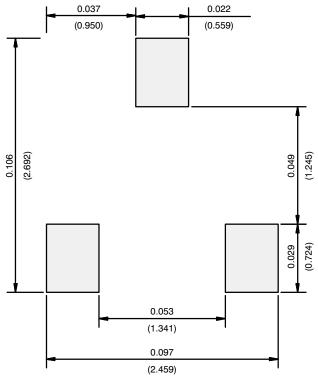
Dim	MILLIM	IETERS	INCHES		
	Min	Max	Min	Max	
Α	0.89	1.12	0.035	0.044	
A <sub>1</sub>	0.01	0.10	0.0004	0.004	
A <sub>2</sub>	0.88	1.02	0.0346	0.040	
b	0.35	0.50	0.014	0.020	
С	0.085	0.18	0.003	0.007	
D	2.80	3.04	0.110	0.120	
E	2.10	2.64	0.083	0.104	
E <sub>1</sub>	1.20	1.40	0.047	0.055	
е	0.95 BSC		0.0374	4 Ref	
e <sub>1</sub>	1.90 BSC		0.074	8 Ref	
L	0.40	0.60	0.016	0.024	
L <sub>1</sub>	0.64 Ref		0.025 Ref		
S	0.50 Ref		0.020 Ref		
q	3°	8°	3°	8°	

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DWG: 5479



### **RECOMMENDED MINIMUM PADS FOR SOT-23**



Recommended Minimum Pads Dimensions in Inches/(mm)



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