

SPECIFICATIONS

MODEL NO.	V90502-DT043WV
TYPE	LCD MODULE, 480(RGB) * 800 PIXELS

☒ Preliminary Specification

☐ Final Specification

Victronix			CUSTOMER
PREPARED	CHECKED	APPROVED	APPROVED
		2013.7.25	
2013.7.25	2013.7.25		

VICTRONIX ELECTRONICS LTD

RECORDS OF REVISION

[illegible]

CONTENT

1. GENERAL SPECIFICATION	4
2. BLOCK DIAGRAM	5
3. MECHANICAL DRAWING	6
4. INTERFACE ASSIGNMENT	7
5. ELECTRICAL SPECIFICATION	9
6. OPTICAL CHARACTERISTICS	18
7. RELIABILITY TESTS	22
8. PRECAUTIONS	23
9. LIMITED WARRANTY	23

1. GENERAL SPECIFICATION

1.1 Description

The V90502-DT043WV is a color active matrix Thin Film Transistor (TFT) Liquid Crystal Display (LCD) that uses amorphous silicon(a-Si) TFT as a switching device. This model is composed of a single 4.3 inches transmissive type main TFT-LCD panel. The resolution of the panel is 480 x 800 pixels and can display up to 16.7M color.

1.2 Feature

- TN type for main TFT-LCD panel
- Structure COG+FPC+BL
- Full, Normal (Still), Partial, Sleep, Standby mode are available

1.3 Application

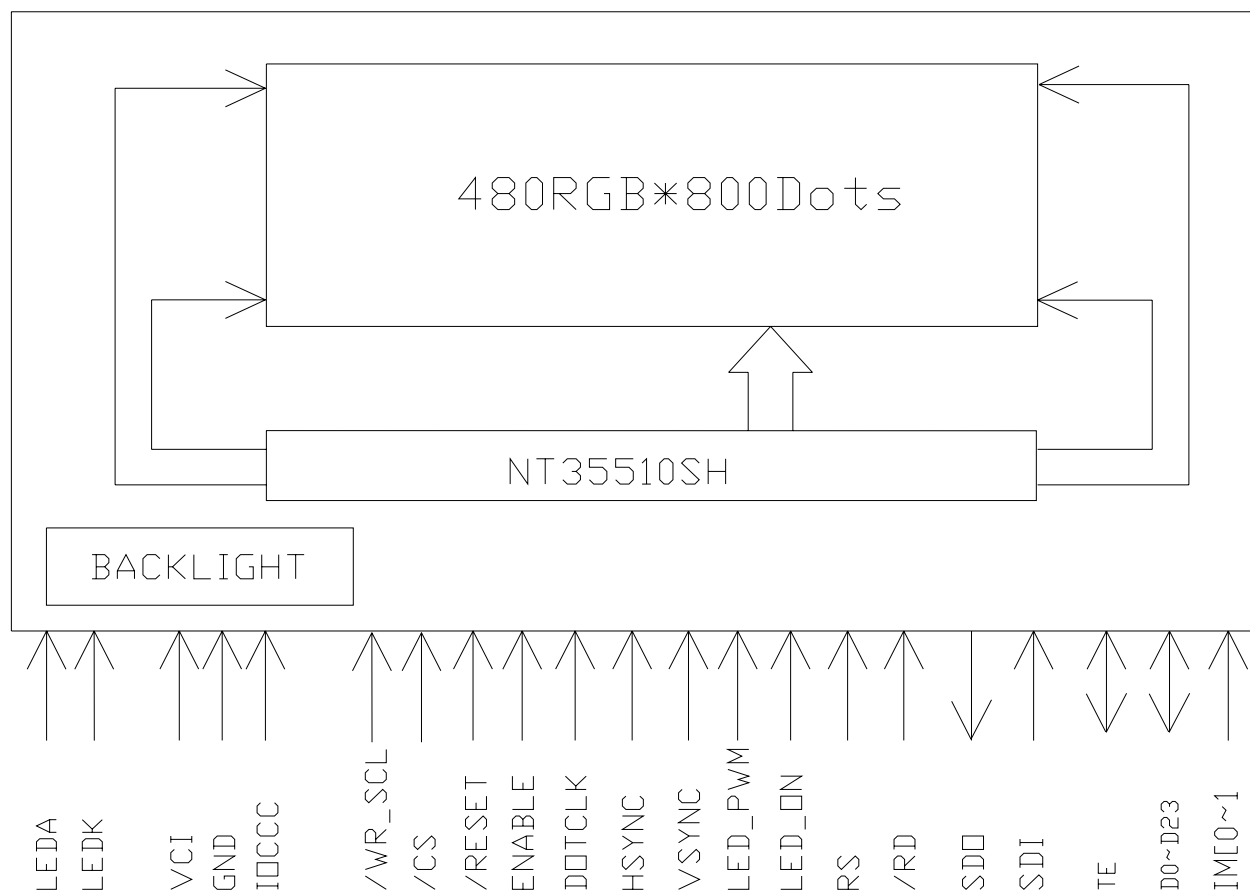
- Display terminals for cellular phone

1.4 General Specification

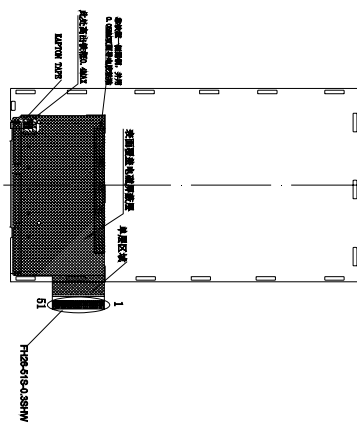
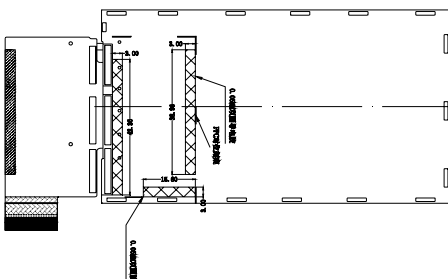
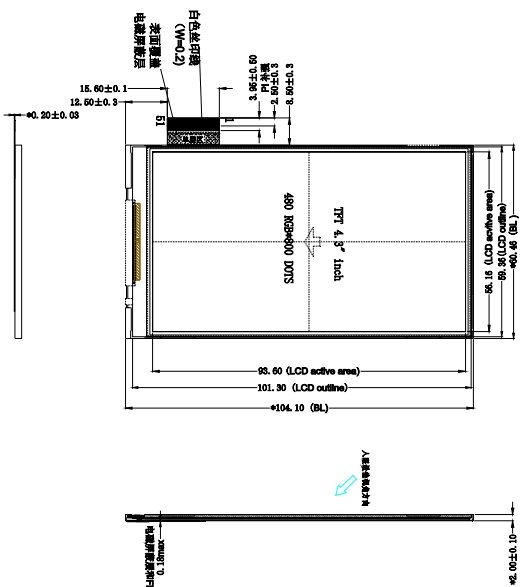
No.	Item	Specification	Unit	Remark
1	LCD Size	4.3	inch	-
2	Panel Type	a-Si TFT active matrix	-	-
3	Resolution	480 x (RGB) x 800	pixel	-
4	Display Mode	Normally white, Transmissive	-	-
5	Display Number of Colors	16.7M	-	-
6	Viewing Direction	12 o'clock(Viewing direction)	-	Note
7	Contrast Ratio	500(Typ)	-	-
8	Luminance	350(Typ)	cd/m ²	-
9	Module Size	60.64(W) x 104.1(L) x 2.0(T)	mm	Note
10	Active Area	56.16(W) x 93.6(L)	mm	Note
11	Pixel Pitch	0.108(W) x 0.108 (L)	mm	-
12	Weight	26.5	g	-
13	Driver IC	NT35510	-	-
14	Driver IC RAM Size	480x24x800	bit	-
15	Light Source	8 LEDs White	-	-
16	Interface	MPU parallel 16/18/24-bit RGB-SPI	-	Refer to IM[1:0] connection
17	Operating Temperature	-20~70	°C	-
18	Storage Temperature	-30~80	°C	-

Note: Please refer to the mechanical drawing.

2. BLOCK DIAGRAM



3. MECHANICAL DRAWING



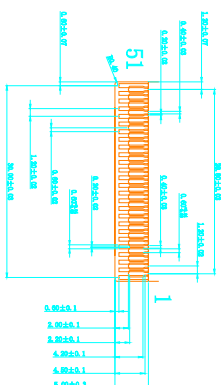
No.	PIN NAME	27	DB13
1	LEDK	28	DB12
2	LEDA	29	DB11
3	YU	30	DB10
4	XR	31	DB9
5	YD	32	DB8
6	XL	33	DB7
7	GND	34	DB6
8	VCI	35	DB5
9	NC	36	DB4
10	IOVCC	37	DB3
11	TE	38	DB2
12	SDO	39	DB1
13	SDI	40	ENB
14	/WM_SCL	41	ENABLE
15	/CS	42	D0TCLK
16	/RESET	43	HSYNC
17	DB23	44	VSNC
18	DB22	45	LED_PWM
19	DB21	46	LED_ON
20	DB20	47	RS
21	DB19	48	RD
22	DB18	49	IM0
23	DB17	50	IM1
24	DB16	51	GND
25	DB15		
26	DB14		

NOTE:

1. GENERAL TOLERANCE: ± 0.2 .
 2. (...) IS REFERENCE DIMENSION.
 3. * CRITICAL DIMENSION
 4. COMPATIBLY ROHS.
 5. VAR: $\leq 0.3\text{mm}$
 6. 表面硬度: $\geq 180\text{HV}$
 7. 是否支持倒角: 不支持
 8. 扫描方向: 左上到右下
-
- (CIRCUIT DIAGRAM)



DOTS DETAIL



DETAIL (SCALE 4:1)

"Not to use the substances and their applications or SUCCESS Management Standard for Environment-related Substances to be Controlled"

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4. INTERFACE ASSIGNMENT

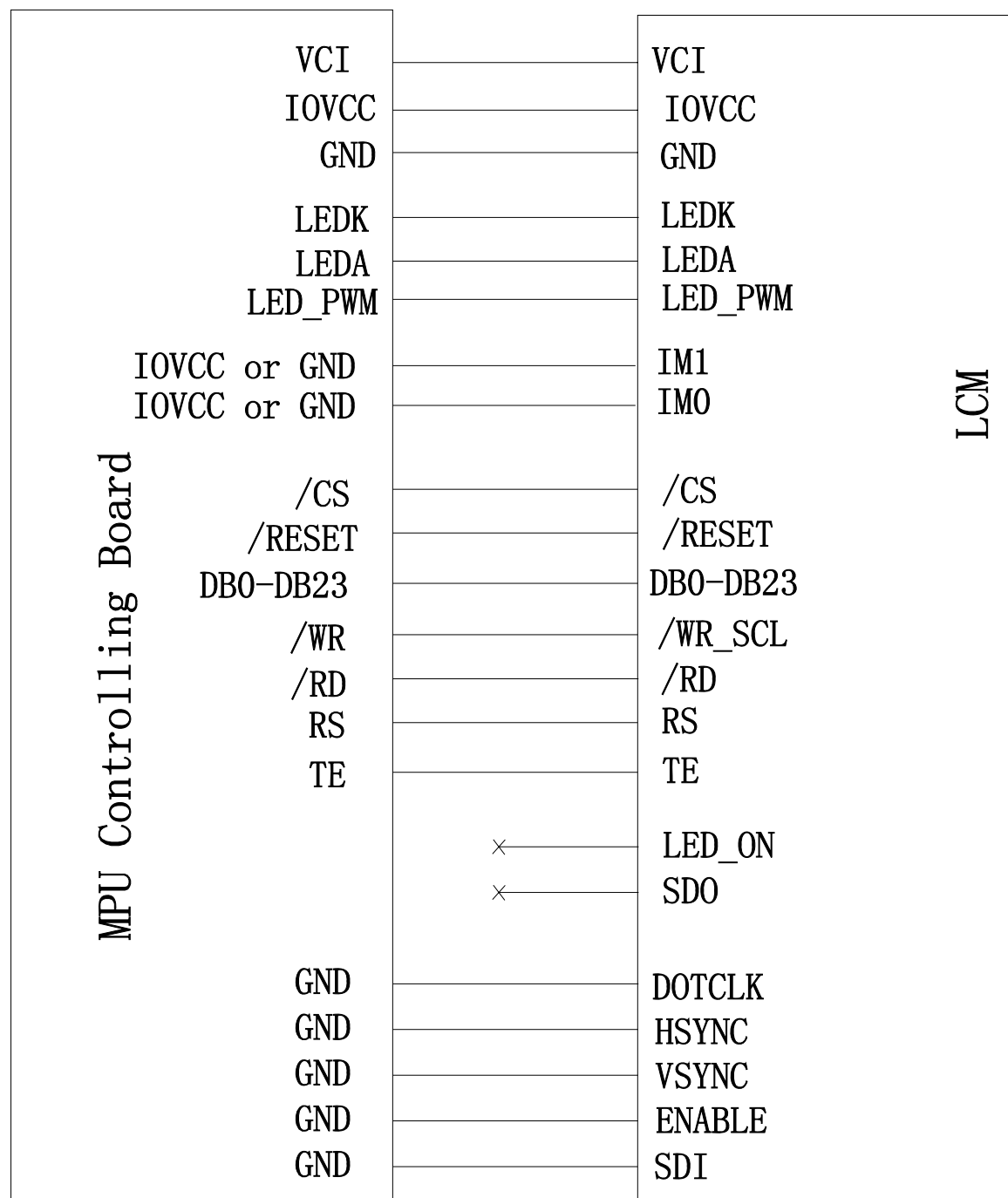
PIN NO.	SYMBOL	FUNCTION DESCRIPTIONS
1	LEDK	Power supply for backlight (anode).
2	LEDA	Power supply for backlight (cathode).
3	YU	Touch panel interface for YU,prepared for RTP.Open this pin if without RTP
4	XR	Touch panel interface for XR,prepared for RTP.Open this pin if without RTP
5	YD	Touch panel interface for YD,prepared for RTP.Open this pin if without RTP
6	XL	Touch panel interface for XL,prepared for RTP.Open this pin if without RTP
7	GND	Ground
8	VCI	Power supply 2.85V
9	NC	No connection
10	IOVCC	Power supply 1.8V
11	TE	Tearing effect output pin to synchronize MCU to frame writing, activated by S/W command. When this pin is not activated, this pin is output low. If not used, please open this pin.
12	SDO	Serial output signal in SPI I/F. The data is output on the rising/falling edge of the SCL signal. If the host places the SDI line into high-impedance state during the read interval, the SDI and SDO can be tied together. This pin is not used for 80-series MPU I/F, please open this pin.
13	SDI	Serial input signal in SPI I/F. The data is input on the rising/falling edge of the SCL signal. This pin is not used for 80-series MPU I/F, please connect to GND this pin.
14	/WR_SCL	Writes strobe signal to write data when WRX is "Low" in 80-series MPU I/F. SCL: A synchronous clock signal in SPI I/F.
15	/CS	Chip select signal
16	/RESET	Reset
17~40	DB23~DB0	24-bit bi-directional data bus for 80-series MPU I/F and 24-bit input data bus for RGB I/F.. For RGB I/F: 24-bit/pixel: D[23:16]=R[7:0], D[15:8]=G[7:0] and D[7:0]=B[7:0]
41	ENABLE	Data enable signal in RGB I/F mode 1. This pin is not used for RGB mode 2, 80-series MPU or MIPI I/F, please connect to GND this pin.
42	DOTCLK	Pixel clock signal in RGB I/F. This pin is not used for 80-series MPU or MIPI I/F, please connect to GND this pin.

43	HSYNC	Horizontal sync. Signal in RGB I/F. This pin is not used for 80-series MPU or MIPI I/F, please connect to GND this pin.		
44	VSYNC	Vertical sync. Signal in RGB I/F. This pin is not used for 80-series MPU or MIPI I/F, please connect to GND this pin.		
45	LED_PWM	This pin is connect to the external LED driver. It is a PWM type control signal for brightness of the LED backlight. The width of LEDPWM signal is set from 256 values between 0% (Low) and 100% (High) If not used, please open this pin.		
46	LED_ON	Test pin, not accessible to user. Must be left open.		
47	RS	Display data / command selection in 80-series MPU I/F. RS = "0" : Command RS = "1" : Display data or Parameter This pin is not used for 9/16-bit SPI I/F, please connect to IOVCC this pin.		
48	/RD	Reads strobe signal to write data when RDX is "Low" in 80-series MPU interface. This pin is not used for SPI or MIPI I/F, please connect to IOVCC this pin.		
49	IM0	IM[1:0]	Display Data	Command
		01	80-series 16-bit MPU I/F, DB[15:0]	80-series 16-bit MPU I/F, DB[15:0]
50	IM1	10	80-series 18-bit MPU I/F, DB[17:0]	80-series 18-bit MPU I/F, DB[17:0]
		10	80-series 24-bit MPU I/F, DB[23:0]	80-series 24-bit MPU I/F, DB[23:0]
		11	RGB I/F, D[23:0]	16-bit SPI (SCL rising edge trigger), SDI/SDO
51	GND	Ground		

5. ELECTRICAL SPECIFICATION

5.1. APPLICATION CIRCUIT

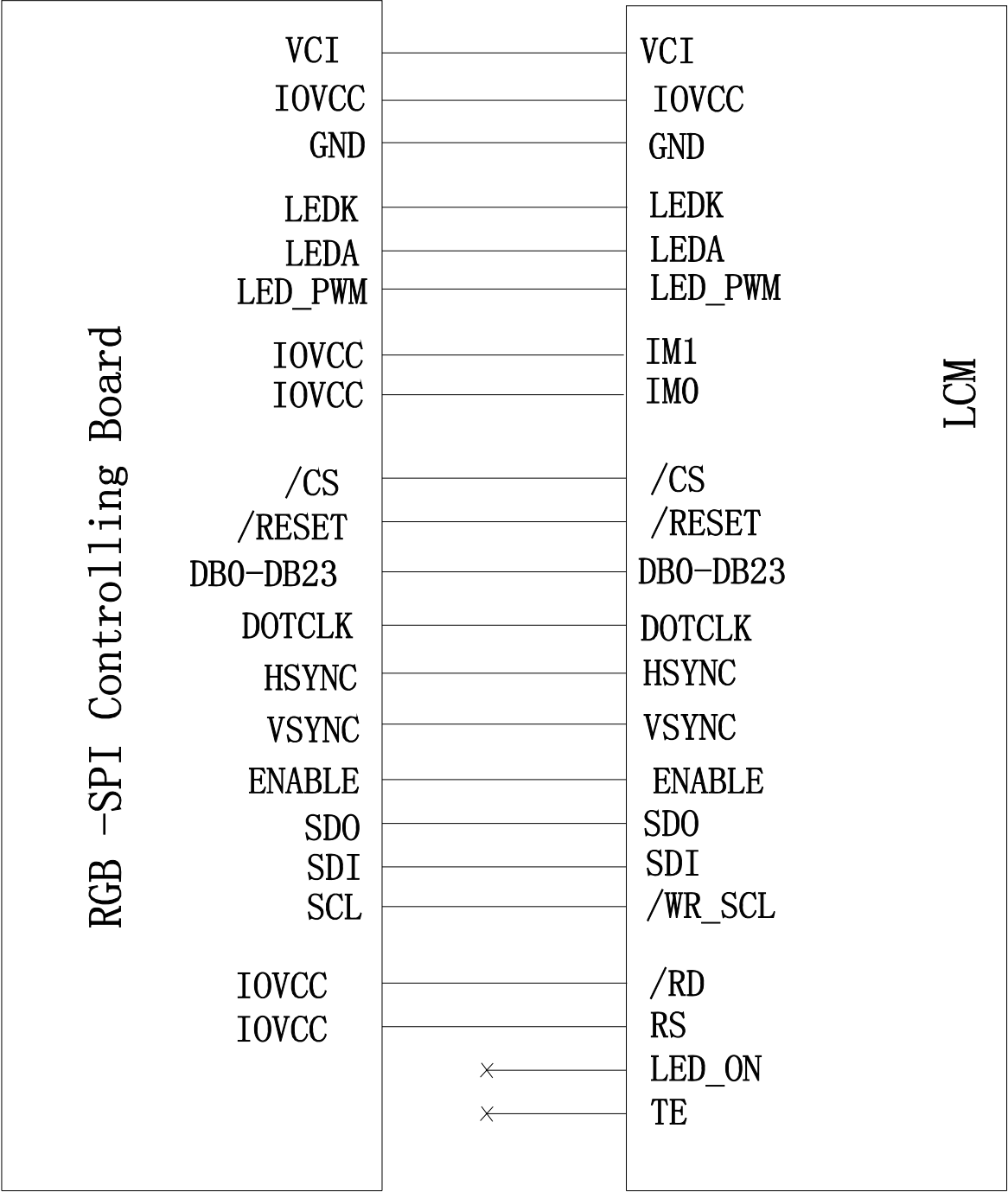
5.1.1 MPU Interface



Note:

1. For different IM[1:0] value, data bus will be different, refer to INTERFACE ASSIGNMENT;
2. MPU 18/24 bit interface is determined by IM[1:0] and initial code(3A00h)
 MPU 18-bit: (0x3A00, 0x66)
 MPU 24-bit: (0x3A00, 0x77)

5.1.2 RGB-SPI Interface



5.2. ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	CONDITION	STANDARD VALUE			UNIT
			MIN	TYP	MAX	
Power Supply for Analog	VCI	Ta=25 °C	-0.3	-	5.0	V
Power Supply for Digital IO	IOVCC	Ta=25 °C	-0.3	-	3.6	V

Note: Permanent damage to the device may occur if maximum values are exceeded or reverse voltage is applied.

5.3. TYPICAL OPERATION CONDITION**5.3.1 DC Characteristics**

ITEM	SYMBOL	CONDITION	STANDARD VALUE			UNIT
			MIN	TYP	MAX	
Power Supply for Analog	VCI	Ta=25 °C	2.5	2.85	3.6	V
Power Supply for Digital IO	IOVCC	Ta=25 °C	1.65	1.8	3.3	V
Input Signal "H" Level	V _{IH}	-	0.7IOVCC	-	IOVCC	V
Input Signal "L" Level	V _{IL}	-	0	-	0.3IOVCC	V
Output Signal "H" Level	V _{OH}	I _{OH} =-0.1mA	0.8IOVCC	-	IOVCC	V
Output Signal "L" Level	V _{OL}	I _{OL} =0.1mA	0	-	0.2IOVCC	V
Frame Frequency	f _{FRAME}	-	50	70	80	Hz

Note: To prevent IC latch up or DC operation in LCD panel, the power on/off sequence should follow the driver IC specification.

5.3.2 Current Consumption

Item	Symbol	Values		Unit	Remark
		type	Max.		
RGB-SPI 24-bit Interface					
Normal(Still) Mode	I _{CC1}	30	50	mA	Note1
Standby Mode	I _{CC1}	-	150	uA	Note2

Note1: Test Condition

Typ: IOVCC=VCI=2.85V

Display Pattern: All Pixel Black

Frame Rate=60Hz at 2-dot Inversion

Operating Temperature: 25°C

Max. current check pattern:

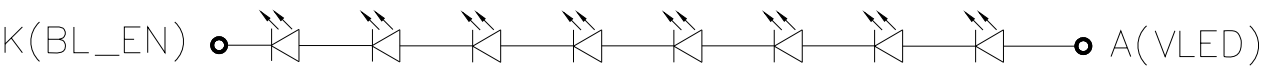


Black

Note2: In the standby mode, all the internal display operations are suspended including the internal R-C oscillator.

5.4. BACKLIGHT SPECIFICATION

5.4.1 BACKLIGHT CIRCUIT



5.4.2 ELECTRICAL CHARACTERISTICS

(T=25℃)

PARAMETER	SYMBOL	CONDITION	STANDARD VALUE			UNIT
			MIN	TYP	MAX	
FORWARD VOLTAGE (Single LED Chip)	VF	IF=20mA	2.9	3.2	3.4	v

5.5. INTERFACE TIMING CHARACTERISTICS

5.5.1 PARALLEL 80-SERIES MPU INTERFACE

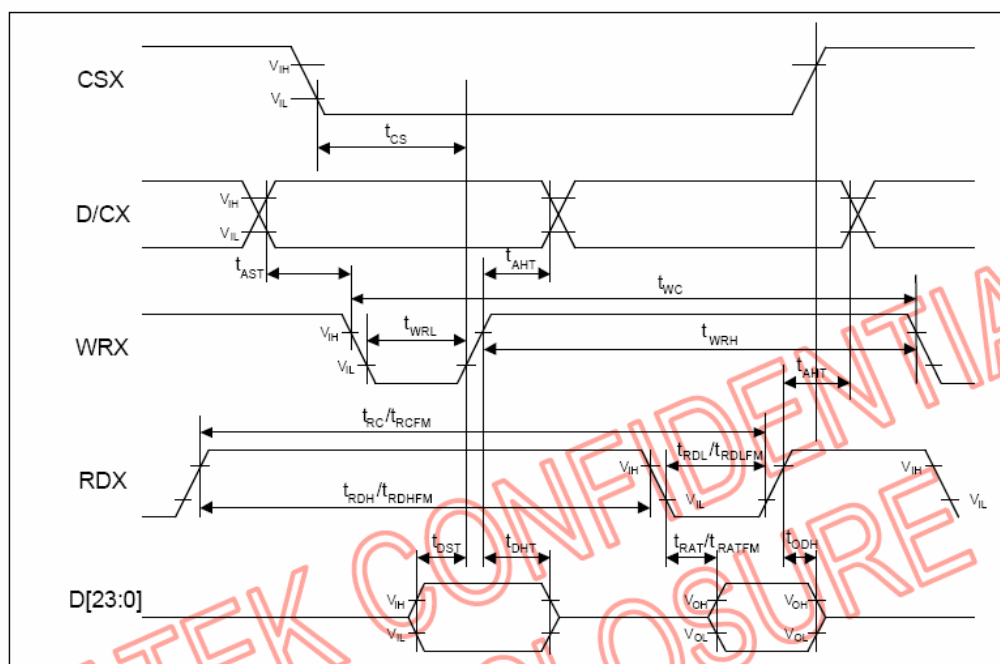


Fig. 7.3.1 Parallel interface characteristics (80-Series)

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.3V, VDD=2.5V to 3.6V, Ta = -30 to 70 °C)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
WRX	tWC	Write cycle	33	-	ns	
	tWRH	Control pulse "H" duration	15	-	ns	
	tWRL	Control pulse "L" duration	15	-	ns	
RDX(ID)	tRC	Read cycle (ID)	160	-	ns	
	tRDH	Control pulse "H" duration (ID)	90	-	ns	When read ID data
	tRDL	Control pulse "L" duration (ID)	45	-	ns	
RDX(FM)	tRCFM	Read cycle (FM)	400	-	ns	
	tRDHFM	Control pulse "H" duration (FM)	250	-	ns	When read from frame memory
	tRDLFM	Control pulse "L" duration (FM)	150	-	ns	
D/CX	tAST	Address setup time (Write)	0	-	ns	
		Address setup time (Read)	10	-	ns	
	tAHT	Address hold time	2	-	ns	
D[17:0]	tDST	Data setup time	15	-	ns	
	tDHT	Data hold time	10	-	ns	
	tRAT	Read access time (ID)	-	40	ns	
	tRATFM	Read access time (FM)	-	150	ns	
	tODH	Output disable time	5	-	ns	

Note: VSS=VSSI=DVSS=GND

VDDI=IOVCC

VDD=VCI

The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

5.5.2.SPI-3 SERIAL INTERFACE

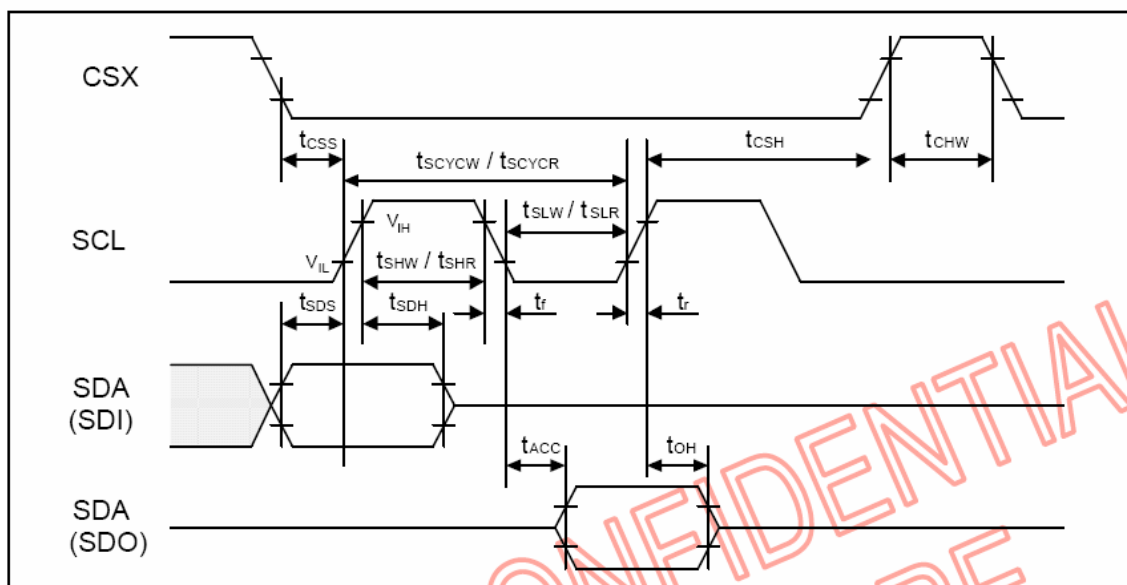


Fig. 7.3.2 3-pin serial interface characteristics

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.3V, VDD=2.5V to 3.6V, Ta = -30 to 70 °C)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
SCL	t_{SCYCW}	Serial clock cycle (Write)	100	-	ns	
	t_{SHW}	SCL "H" pulse width (Write)	40	-	ns	
	t_{SLW}	SCL "L" pulse width (Write)	40	-	ns	
	t_{SCYCR}	Serial clock cycle (Read GRAM)	300	-	ns	
	t_{SHR}	SCL "H" pulse width (Read GRAM)	140	-	ns	
	t_{SLR}	SCL "L" pulse width (Read GRAM)	140	-	ns	
	t_{SCYCR}	Serial clock cycle (Read ID)	300	-	ns	
	t_{SHR}	SCL "H" pulse width (Read ID)	140	-	ns	
	t_{SLR}	SCL "L" pulse width (Read ID)	140	-	ns	
SDI (SDO)	t_{SDS}	Data setup time	20	-	ns	
	t_{SDH}	Data hold time	20	-	ns	
	t_{ACC}	Access time	-	120	ns	
	t_{OH}	Output disable time	5	-	ns	
CSX	t_{CHW}	Chip select "H" pulse width	45	-	ns	
	t_{CSS}	Chip select setup time	20	-	ns	
	t_{CSH}	Chip select hold time	50	-	ns	

Note: VSS=VSSI=DVSS=GND

VDDI=IOVCC

VDD=VCI

The input signal rise time and fall time (t_r , t_f) is specified at 15 ns or less.

5.5.3.RGB INTERFACE

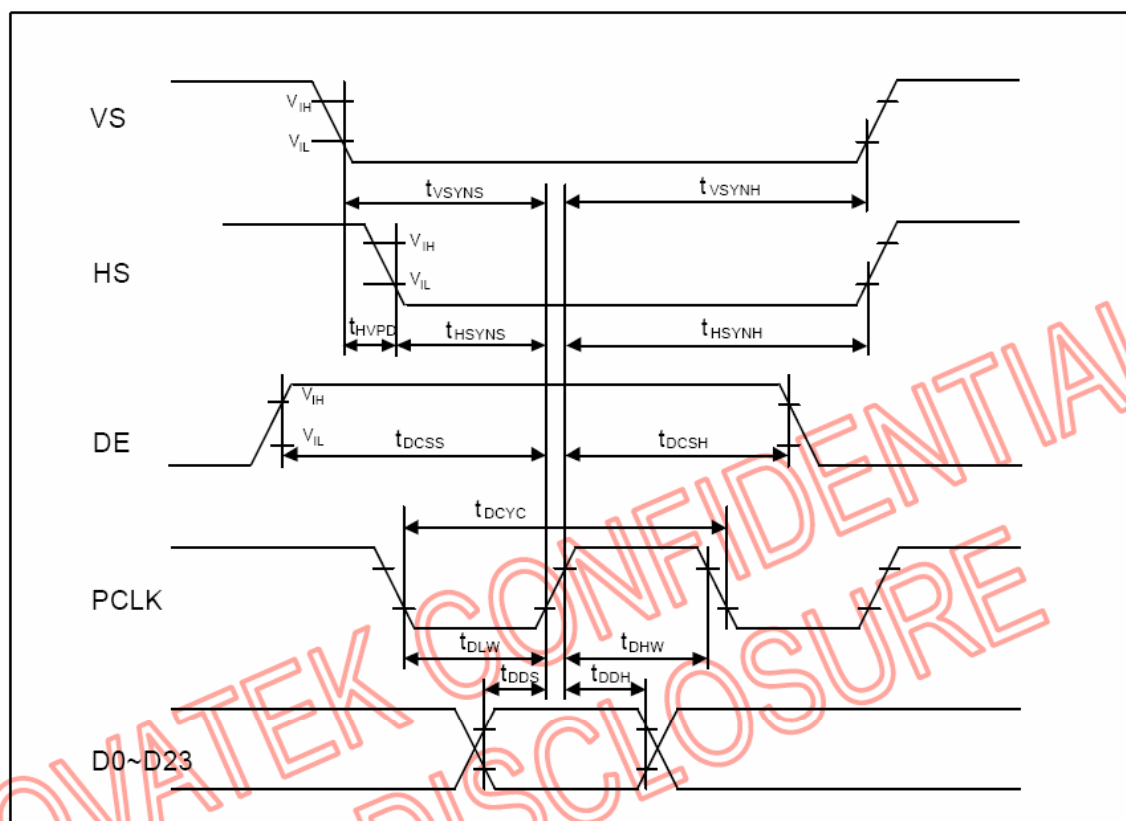


Fig. 7.3.4 RGB interface characteristics

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.3V, VDD=2.5V to 3.6V, Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
VS	t_{VSYNS}	VS setup time	10	-	-	ns	
	t_{VSYNH}	VS hold time	10	-	-	ns	
HS	t_{HSYNS}	HS setup time	10	-	-	ns	
	t_{HSYNH}	HS hold time	10	-	-	ns	
	t_{HVPD}	HSYNC to VSYNC falling edge	400	-	-	ns	
PCLK	t_{DCYC}	PCLK cycle time	33	-	125	ns	
	t_{DLW}	PCLK "L" pulse width	11	-	-	ns	
	t_{DHW}	PCLK "H" pulse width	11	-	-	ns	
	f_{DFREQ}	PCLK frequency	8	-	30	MHz	
DE	t_{DCSS}	DE setup time	10	-	-	ns	
	t_{DCSH}	DE hold Time	10	-	-	ns	
D0~D23	t_{DDS}	RGB Data setup time	10	-	-	ns	
	t_{DDH}	RGB Data hold time	10	-	-	ns	

Note: VSS=VSSI=DVSS=GND

VDDI=IOVCC

VDD=VCI

The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

5.6. RESET TIMING CHARACTERISTICS

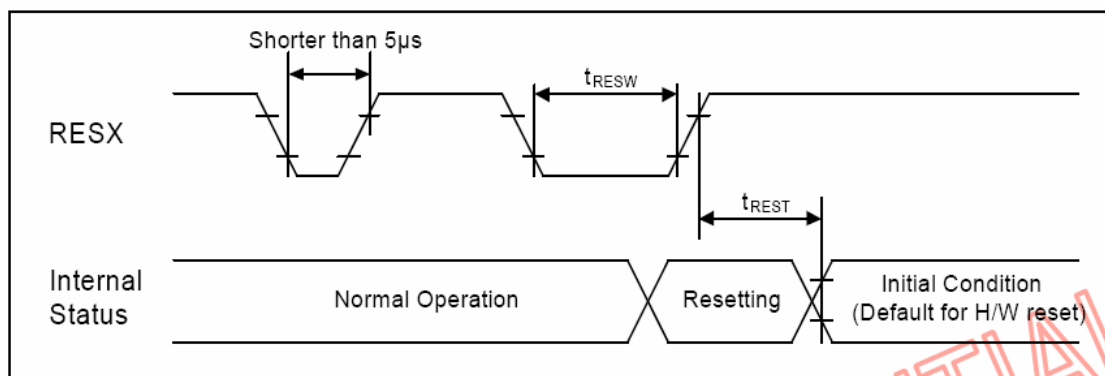


Fig. 7.3.10 Reset input timing

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.3V, VDD=2.5V to 3.6V, Ta = -30 to 70 °C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	t _{RESW}	Reset "L" pulse width (Note 1)	10	-	-	µs	
	t _{REST}	Reset complete time (Note 2)	-	-	5	ms	When reset applied during Sleep In Mode
			-	-	120	ms	When reset applied during Sleep Out Mode

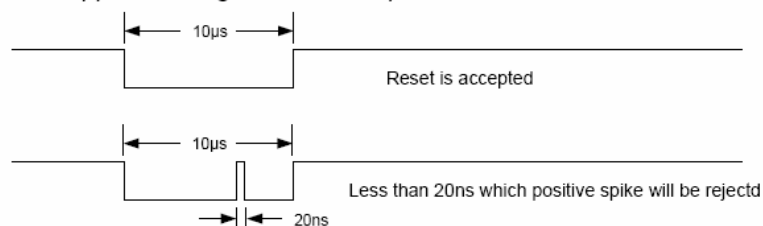
Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 10µs	Reset
Between 5µs and 10µs	Reset Start

Note 2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In–mode) and then return to Default condition for H/W reset.

Note 3) During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 5ms after a rising edge of RESX.

Note 4) Spike Rejection also applies during a valid reset pulse as shown below:



Note 5) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec

6. OPTICAL CHARACTERISTICS(T_a=+25°C, VCI=+2.85V IOVCC=+1.8V, I_B=20mA)

Item		Symbol	Condition	Values			Unit	Remark
				Min.	Typ.	Max.		
Viewing Angle Range	Left	θ_L	$CR \geq 10$	50	60	-	degree	Note 1,2
	Right	θ_R		50	60	-		
	Top	Φ_T		40	50	-		
	Bottom	Φ_B		50	60	-		
Response Time		$T_{on} + T_{off}$	Normal $\theta = \phi = 0^\circ$	-	16	32	ms	Note 2,3
Contrast Ratio		CR	Normal $\theta = \phi = 0^\circ$	-	500	-	-	Note 2,4
Luminance		L	Normal $\theta = \phi = 0^\circ$	300	350	-	cd/m ²	Note 2,5
Color Chromaticity (CIE1931)	White	Wx	Normal $\theta = \phi = 0^\circ$	-	0.30	-	-	Note 2,6
		Wy		-	0.32	-		
	Red	Rx		-	0.61	-		
		Ry		-	0.36	-		
	Green	Gx		-	0.31	-		
		Gy		-	0.59	-		
	Blue	Bx		-	0.15	-		
		By		-	0.09	-		
Color Gamut		NTSC	CIE1931	-	60	-	%	-
Luminance Uniformity		U_L	Normal $\theta = \phi = 0^\circ$	75	80		%	Note 2,7

Note 1: Definition of viewing angle range

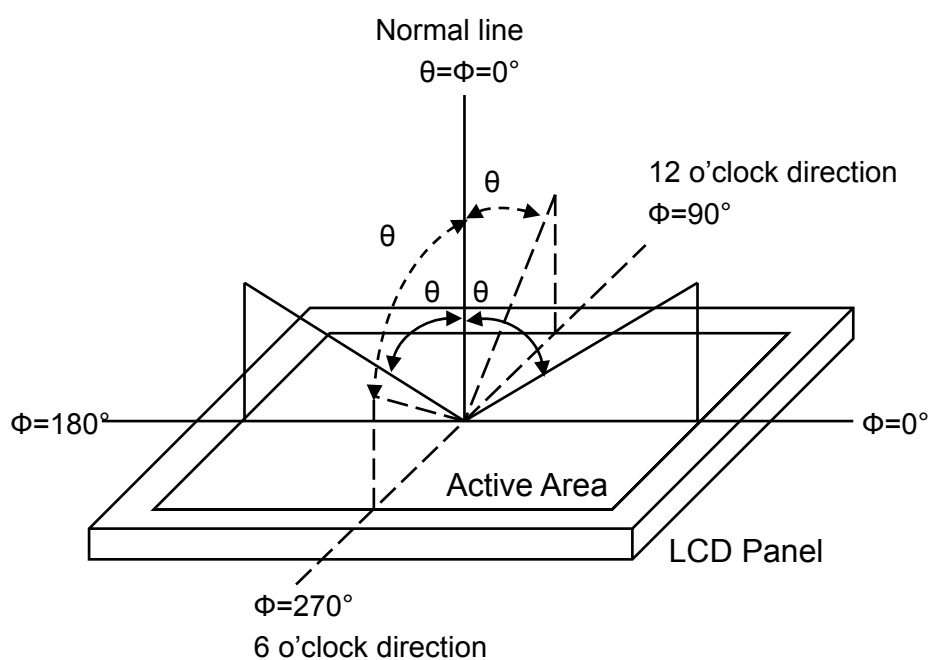


Fig. 1 Definition of viewing angle

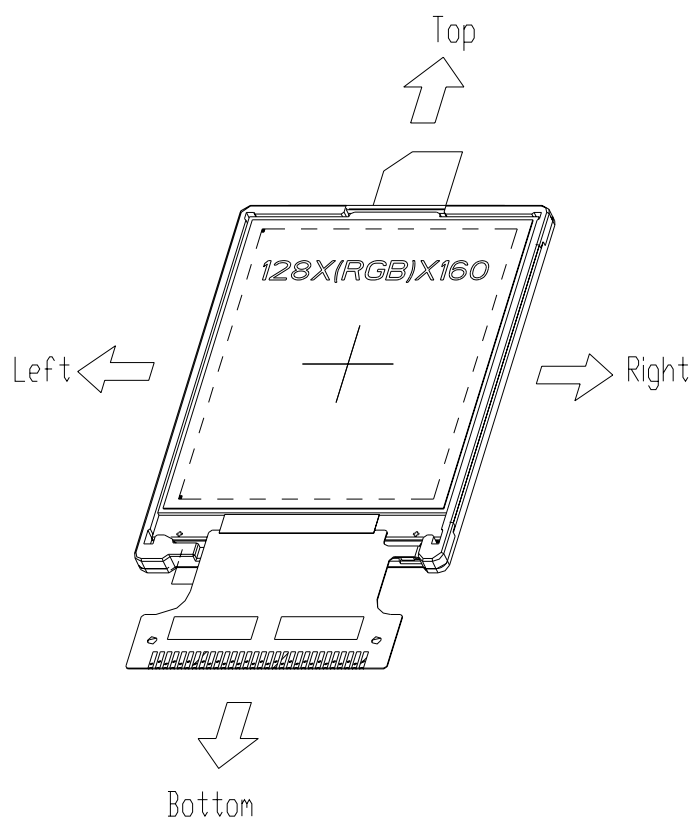


Fig. 2 Definition of viewing angle for display

Note 2: Definition of optical measurement system

The optical characteristics should be measured in a dark room with ambient temperature $T_a=+25^{\circ}\text{C}$. The optical properties are measured at the center point of the LCD screen after 5 minutes operation. (Equipment: Photo detector TOPCON BM-5AS Field of view: 1° /Height: 500mm.)

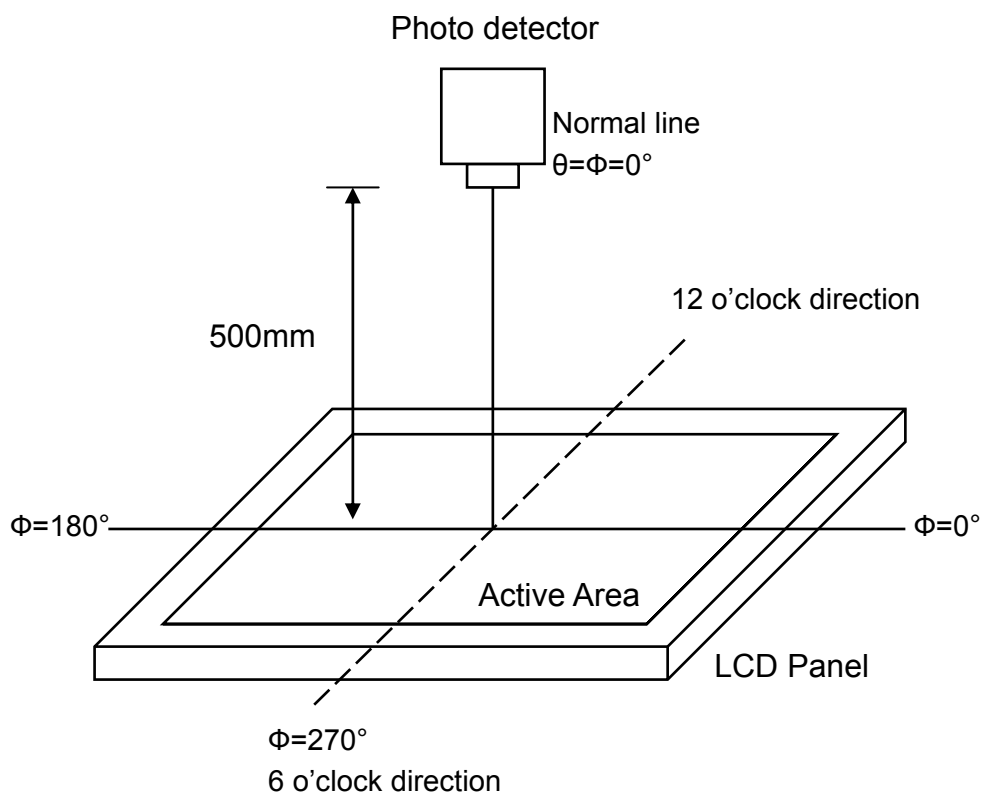


Fig. 3 Optical measurement system setup

Note 3: Definition of response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (T_{on}) is the time between photo detector output intensity changed from 90% to 10%, and fall time (T_{off}) is the time between photo detector output intensity changed from 10% to 90%.

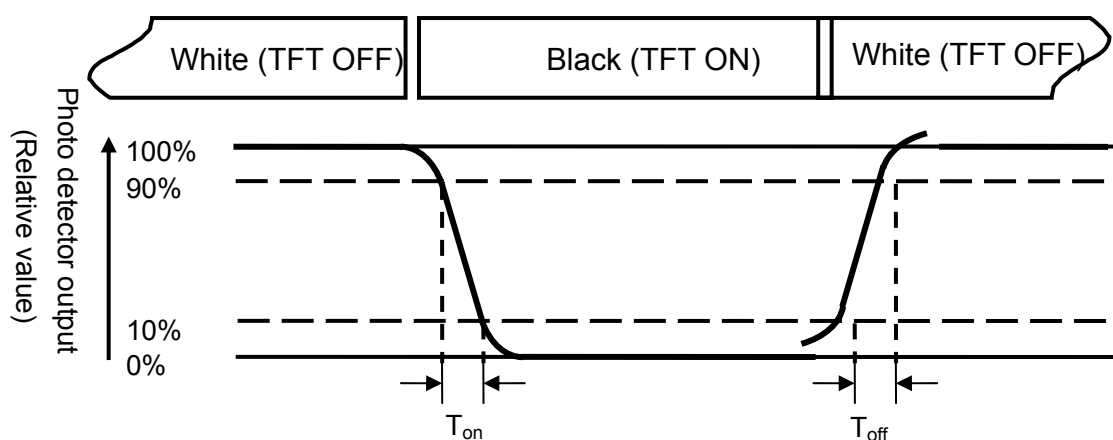


Fig. 4 Definition of response time

Note 4: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: Definition of luminance

Measured at the center area of the panel when LCD panel is driven at "white" state.

Note 6: Definition of color chromaticity (CIE1931)

Color coordinates measured at the center point of LCD when panel is driven at "White", "Red", "Green" and "Blue" state respectively.

Note 7: Definition of luminance uniformity

To test for uniformity, the tested area is divided into 3 rows and 3 columns. The measurement spot is placed at the center of each circle as below.

$$\text{Luminance Uniformity (U}_L\text{)} = \frac{L_{\min}}{L_{\max}}$$

L-----Active area length

W----- Active area width

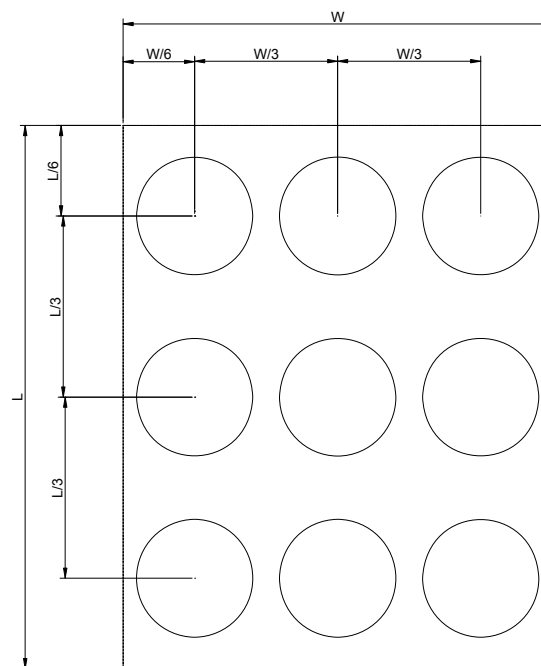


Fig. 5 Definition of luminance uniformity

$L_{\min}$: The measured minimum luminance of all measurement position.

$L_{\max}$: The measured maximum luminance of all measurement position.

7. RELIABILITY TESTS

ITEM	CONDITION	CRITERION
Operating Temperature Test	High Temperature: +70 °C $\pm$ 3°C, 72 hrs	No defects in display and operational functions
	Low Temperature: -20 °C $\pm$ 3°C, 72 hrs	
Storage Temperature Test	High Temperature: +80 °C $\pm$ 3°C, 120 hrs	No defects in display and operational functions
	Low Temperature: -30 °C $\pm$ 3°C, 120 hrs	
Humidity Endurance Test	60 °C $\pm$ 3°C, 90% $\pm$ 3%RH, 72 hrs	No defects in display and operational functions
Thermal Shock Test	-30 °C (30mins)~ +80 °C (30mins) 10 cycles	No defects in display and operational functions
Vibration Resistance Test	Operating Time: thirty minutes exposure for each direction (X,Y,Z) Sweep Frequency:10~55Hz (1 min) Amplitude: 1.5mm	No defects in display and operational functions
Mechanical Shock	100G 6ms, $\pm$ X, $\pm$ Y, $\pm$ Z 3 times for each direction	No defects in display and operational functions
Electro Static Discharge	$\pm$ 2KV, Human Body Mode, 100pF/1500 Ω	No defects in display and operational functions

NOTE:

- 1) The samples must be free from defect before test, must be restored at room condition at least for 2 hours after reliability test before any inspection.
- 2) Before test the function of TP, the sample must be placed in room temperature for 24hrs after RA test.