V6355D

(LCDC)

■ OUTLINE

V6355D (LCDC) is a silicon gate CMOS device. This controller can be connected to both LCD and CRT displays. It is software compatible with IBM-PC and has a function to expand it.

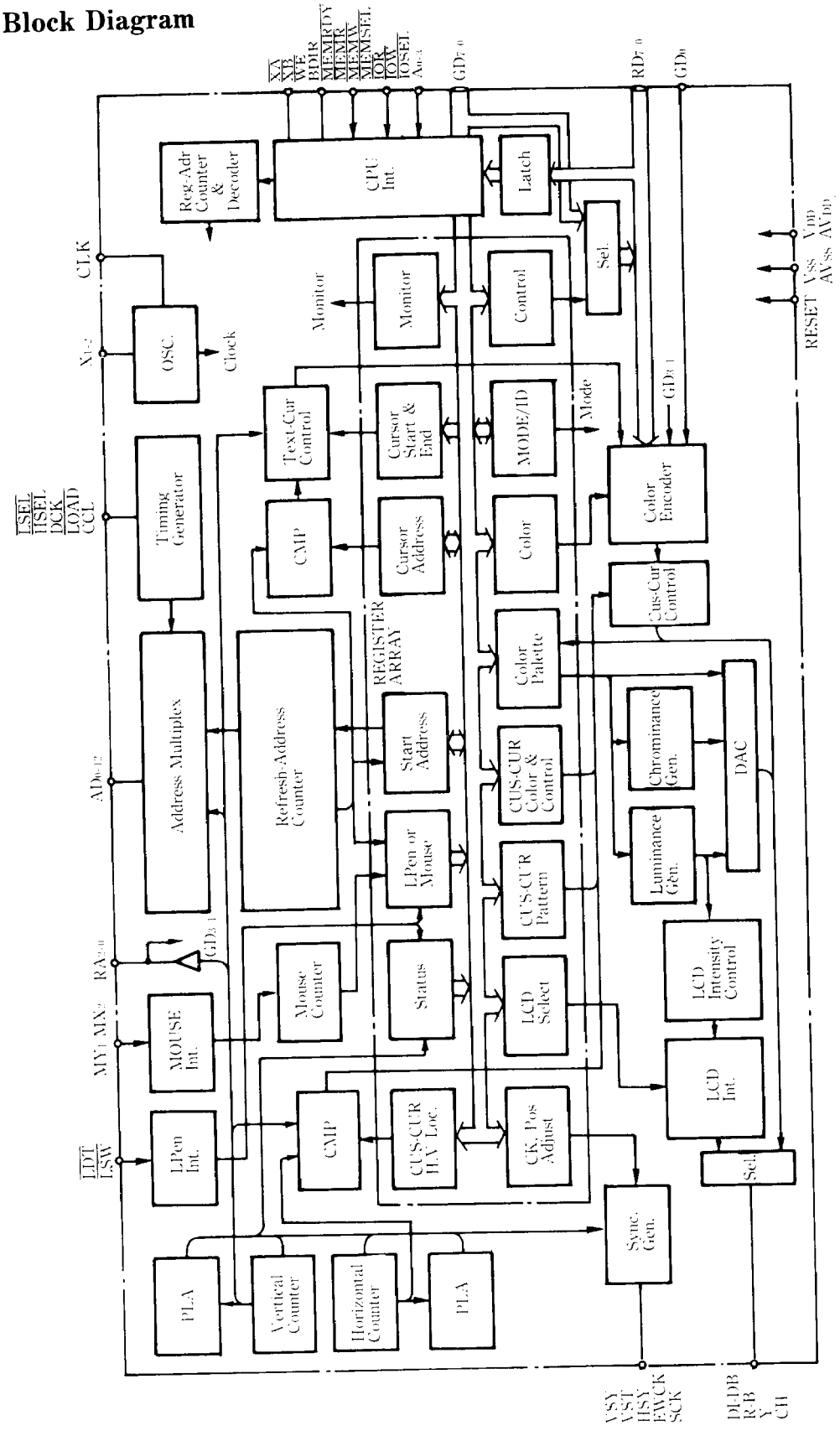
V6355-DF is a 100 pin plastic flat package (QFP) type and V6355-DJ is a 84 pin plastic chip carrier type.

■ FEATURES

- Capable of controlling both LCD and CRT displays.
- Includes 6845 restricted mode and CRT peripheral circuits for IMB-PC.
- Both SRAM and DRAM are usable as VRAM.
- Includes MOUSE and LIGHT PEN interface.
- Cursor position can be specified by any 16 × 16 dot patterns in the bit unit (AND and EXOR screens).
- Includes color palette (16/512 colors).
- LCD intensity controllable (16 or 8 gradation steps)
- Screen modes are available in combinations of the following.

  Horizontal dot number: 640, 320, 512, 256
  Vertical dot number: 192, 200, 204, 64 (64 only with LCD)
  Raster adjustment: 0, 2, 4 or 6 specifiable
- Capable of displaying 16 colors in 640 × 204 by using external circuits.
- CRT monitor selectable from among IBM Color, Monochrome, NTSC system and PAL system.
- Can be interfaced with 3 types of LCD driver.
- Usable with 16 bit bus CPU.

■ LCDC Block Diagram



■ Pin Functions

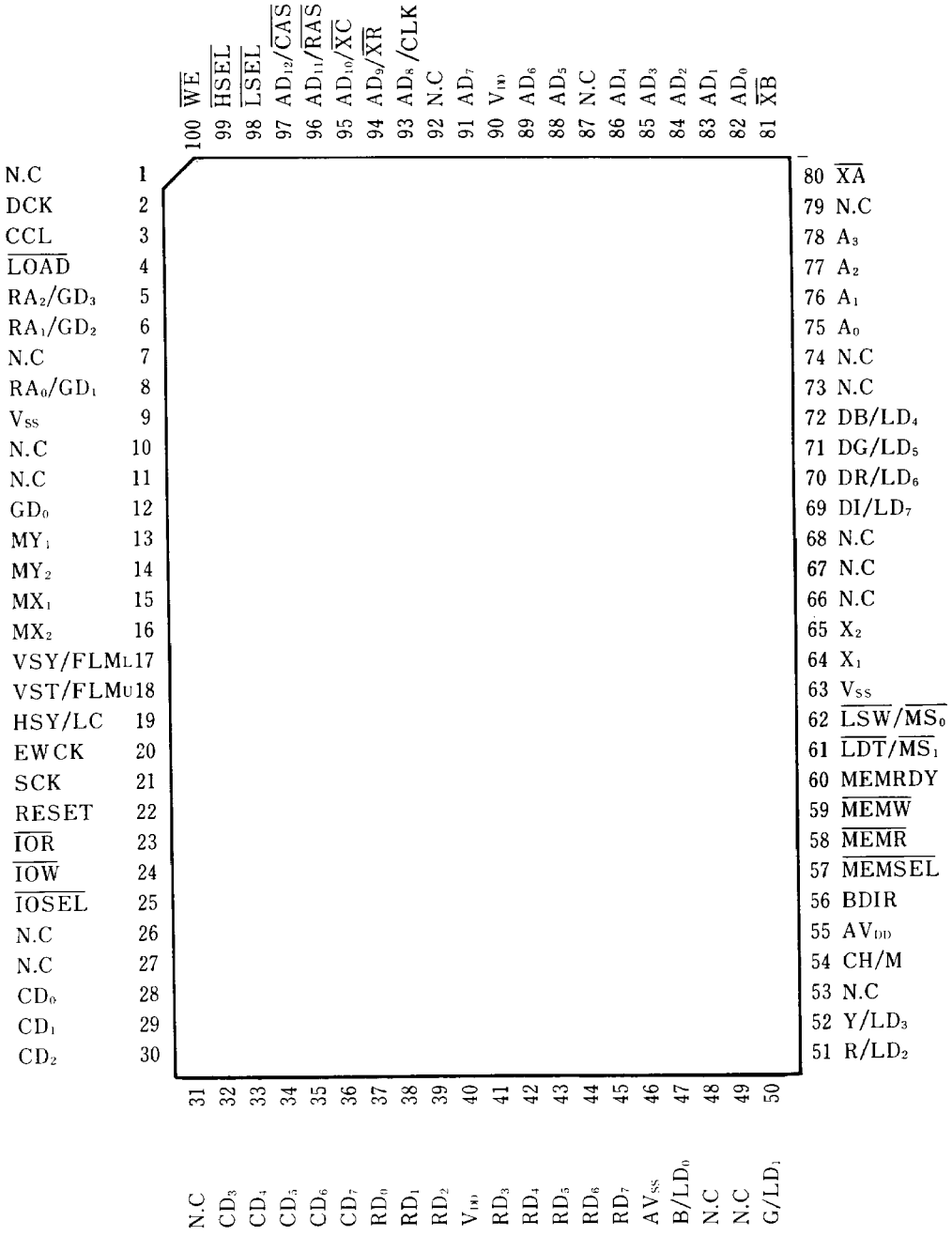
Signature	I/O	Description
$\overline{IOR}$	I	Read enable for I/O register, Active at low level
$\overline{IOW}$	I	Write enable for I/O register, Active at low level
$\overline{IOSEL}$	I	High-order bit decode signal of I/O register address signal, selected at low level
A_0	I	I/O register address signal
A_1	I	
A_2	I	
A_3	I	
$\overline{MEMSEL}$	I	High-order bit decode signal of memory address signal, selected at low level
$\overline{MEMR}$	I	Read enable for memory, Active at low level
$\overline{MEMW}$	I	Write enable for memory, Active at low level
MEMRDY	O	Memory (VRAM) access ready signal, Busy (wait) at low level (High impedance state when memory non-selected ($\overline{MEMSEL}$ = high level))
$\overline{WE}$	O	Write enable for memory
BDIR	O	Direction control of bi-directional buffer (for CPU data bus)
RESET	I	Reset signal
CD_0	I/O	Data bus with CPU
~	I/O	
CD_7	I/O	
RD_0	I/O	Data bus with VRAM
	I/O	
RD_7	I/O	
AD_0	O	VRAM address
~	O	
AD_7	O	

		At SRAM	At DRAM
$AD_8/\overline{CLK}$	O	VRAM address	Outputs external clock dividing signal of 14.31818MHz. Usable for CPU clock by dividing.
$AD_9/\overline{XR}$	O	do.	CPU row Address enable
$AD_{10}/\overline{XC}$	O	do.	CPU column Address enable
$AD_{11}/\overline{RAS}$	O	do.	$\overline{RAS}$
$AD_{12}/\overline{CAS}$	O	do.	$\overline{CAS}$
$\overline{XB}$	O	Data enable when memory read/write	——
$\overline{XA}$	O	Memory read/write timing (CPU address enable at SRAM)	

		At SRAM (8bit CPU)	16bit CPU
$\overline{LSEL}$	O	1st 8K byte selected	Low byte selected
$\overline{HSEL}$	O	2nd 8K byte selected	High byte selected

Signature	I/O	Description	
		A/N Mode	640 × 200 Color mode
RA_2/GD_3	I/O	Raster address (Output)	Graphic data (Input)
RA_1/GD_2	I/O		
RA_0/GD_1	I/O		
GD_0	I	Dot data for character display	
		CRT	LCD
VSY/FLM_L	O	Vertical synchronizing signal	Lower block FLM
VST/FLM_U	O	Vertical retrace line period	Upper block FLM
HSY/LC	O	Horizontal synchronizing signal	Latch clock
EWCK	O	Display valid period	Driver enable signal or tone gradation intensifying signal
SCK	O	——	Shift clock
CH/M	O	Chrominance signal	Signal to change into AC
Y/LD_3	O	Brightness (black/white composite) signal	Data output for upper block
R/LD_2	O	Output for linear RGB	
G/LD_1	O		
B/LD_0	O		
DI/LD_7	O	Output for IBM monitor	Data output for lower block
DR/LD_6	O		
DG/LD_5	O		
DB/LD_4	O		
DCK	O	Dot shift clock (for P/S)	
CCL	O	VRAM data latch clock	
$\overline{LOAD}$	O	Load signal for P/S	
MY_1	I	Counter pulse for MOUSE Y direction	
MY_2	I		
MX_1	I	Counter pulse for MOUSE X direction	
MX_2	I		
$\overline{LDT/MS_1}$	I	Light pen detect signal or mouse switch signal	
$\overline{LSW/MS_0}$	I	Switch signal of light pen or mouse	
X_1	I	For X'tal oscillation, Input to X_1 when inputting external clock	
X_2	O		
AV_{SS}	I	0V — Analog (for DAC) power supply	
AV_{DD}	I	+5V	
V_{SS}	I	0V — Digital power supply	
V_{SS}	I	0V	
V_{DD}	I	+5V	
V_{DD}	I	+5V	

■ Pin Assignment



■ Electrical Characteristics

① Absolute maximum ratings

Parameter	Signature	Min.	Max.	Unit
Supply voltage	V_{DD}	−0.5	+7.0	V
Input voltage	V_I	−0.5	V_{DD}+0.5	V
Output voltage	V_O	−0.5	V_{DD}+0.5	V
Operating temperature	T_{OP}	0	+70	°C
Storage temperature	T_{STG}	−50	+125	°C

(V_{SS}, AV_{SS}=0.0V as standard)

② Recommended conditions for use

Parameter	Signature	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	4.75	5.0	5.25	V
Operating temperature	T_{OP}	0	25	70	°C

Used with V_{DD} and AV_{DD} at the same voltage and V_{SS}, AV_{SS}=0.0V.

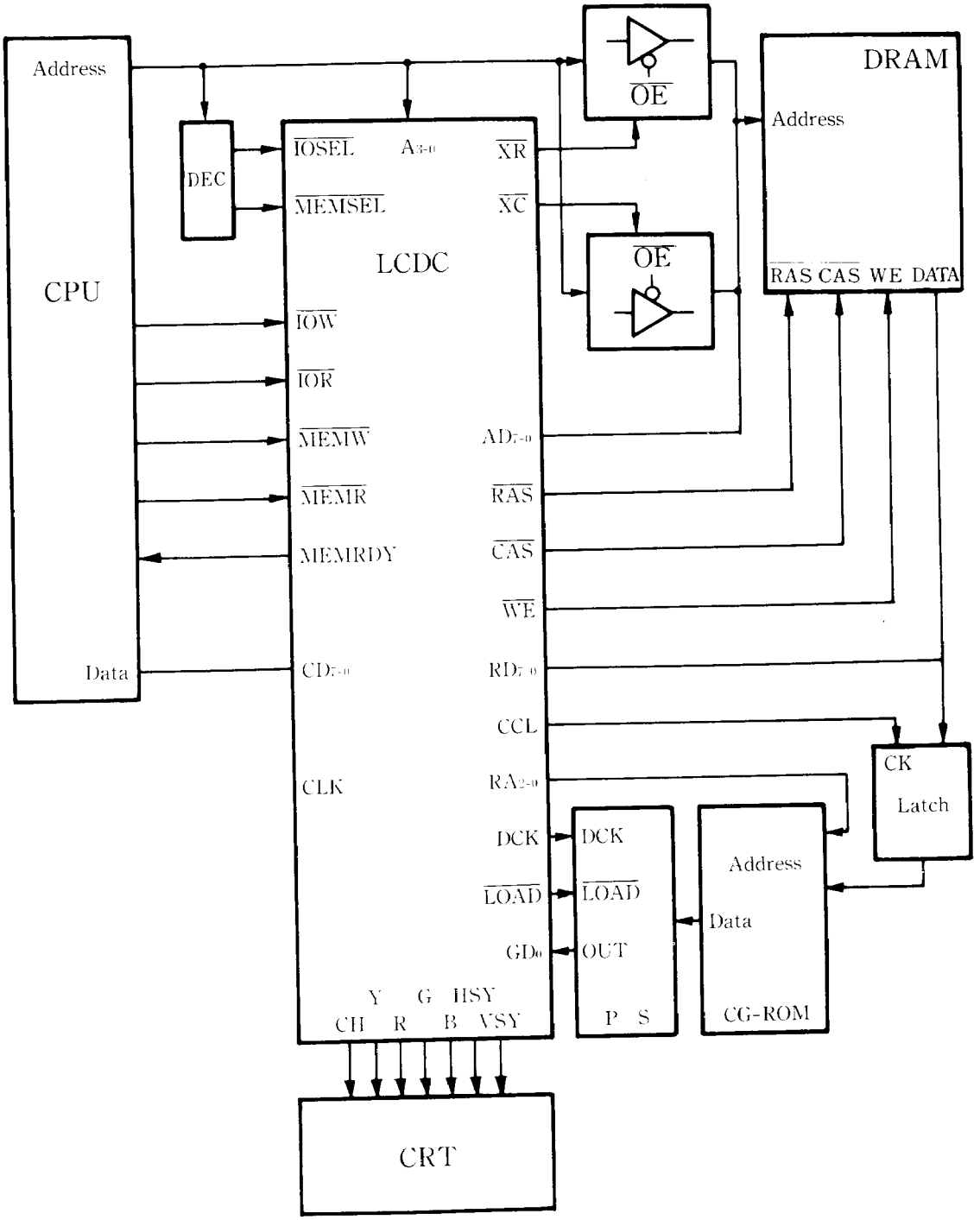
③ DC characteristics

Parameter	Signature	Conditions	Min.	Max.	Unit
High-level output voltage (TTL)	V_{OH}	I_{OH}= −0.4mA	2.7		V
Low-level output voltage (TTL)	V_{OL}	I_{OL}=0.8mA		0.4	V
High-level output voltage (CMOS)	V_{OH}	I_{OH} < 1μA	V_{DD} − 0.4		V
Low-level output voltage (CMOS)	V_{OL}	I_{OL} < 1μA		0.4	V
High-level input voltage	V_{IH}		2.2		V
Low-level input voltage	V_{IL}			0.8	V
High-level output current	I_{OH}	V_{OH}=2.7V	−0.4		mA
Low-level output current	I_{OL}	V_{OL}=0.4V	0.8		mA
Input leak current	I_L		−10	10	μA
Output leak current (tri-state)	I_{LZ}		−10	10	μA
Supply current (at normal operation)	I_{DD}	R_L=5.6KΩ		70	mA
Supply current (at standby)	I_{DD}	R_L=5.6KΩ		50	mA
High-level clock input voltage	V_{CH}		3.6		V
Low-level clock input voltage	V_{CL}			0.6	V

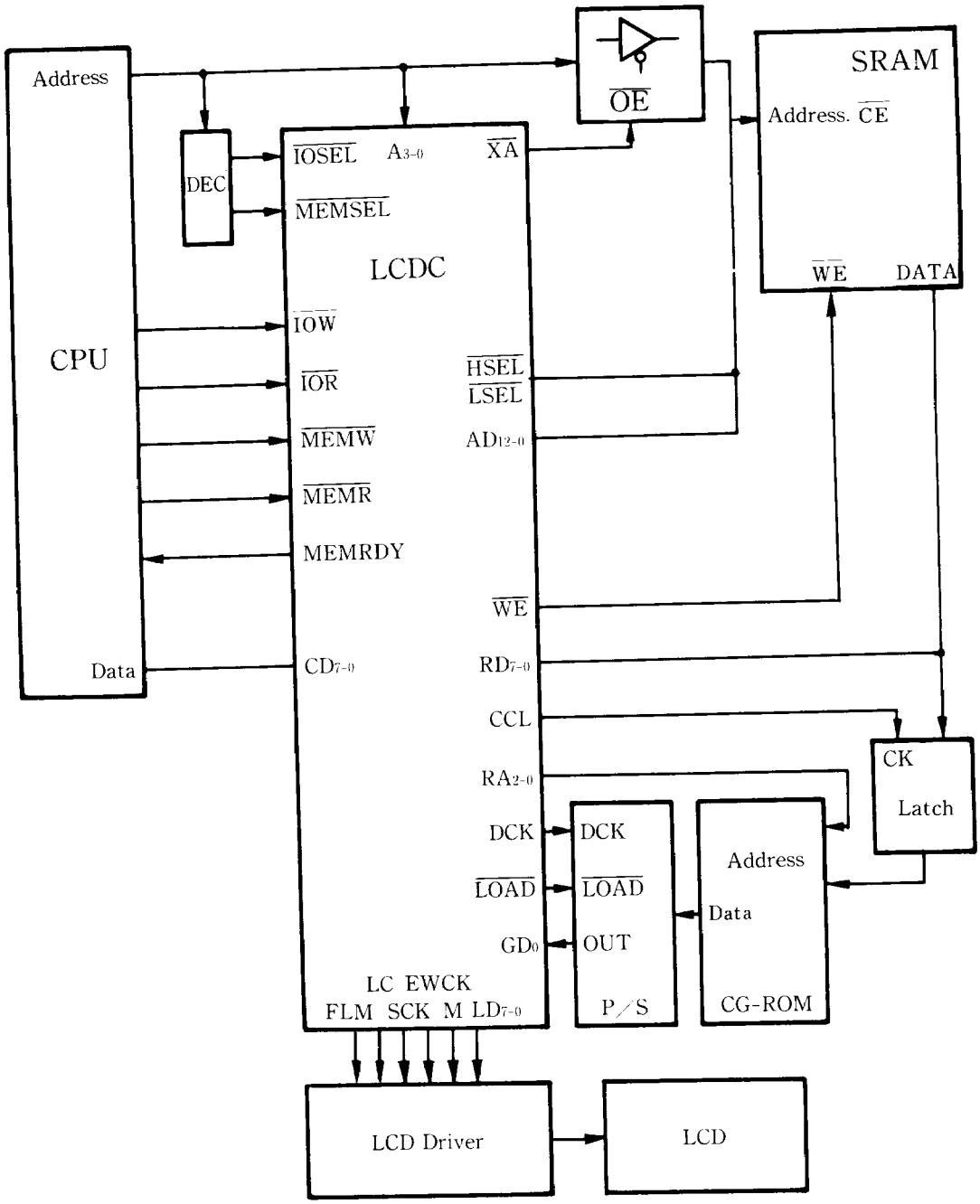
- V_{DD}, AV_{DD}=5.0V ± 5%, T_{OP}=0 ~ 70°C
  Supply voltage is obtained by adding mean current at V_{DD} and AV_{DD} terminals.
- R_L: Terminal resistance between Y, R, G, B, CH terminals and GND.
- Output leak current (tri-state) is for when $CD_{0\sim7}$, $RD_{0\sim7}$ and $RA_2/GD_3 \sim RA_0/D_1$ are in the input mode and when $AD_0 \sim AD_{12}$ $\overline{CAS}$, $\overline{LSEL}$, $\overline{HSEL}$ and MEMRDY are in the high impedance mode.

■ System Configuration (Examples)

① When using CRT display (DRAM used)

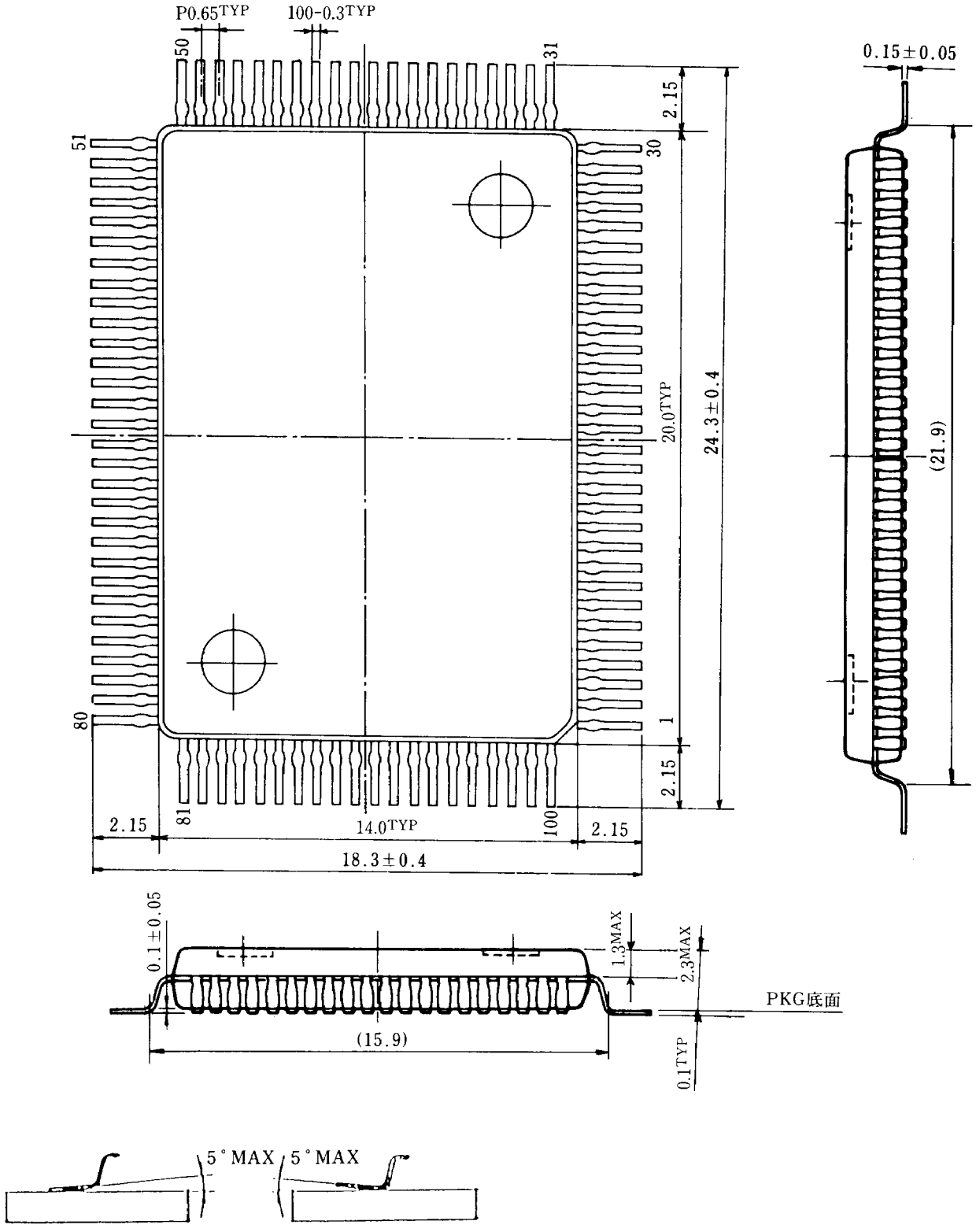


② When using LCD display (SRAM used)

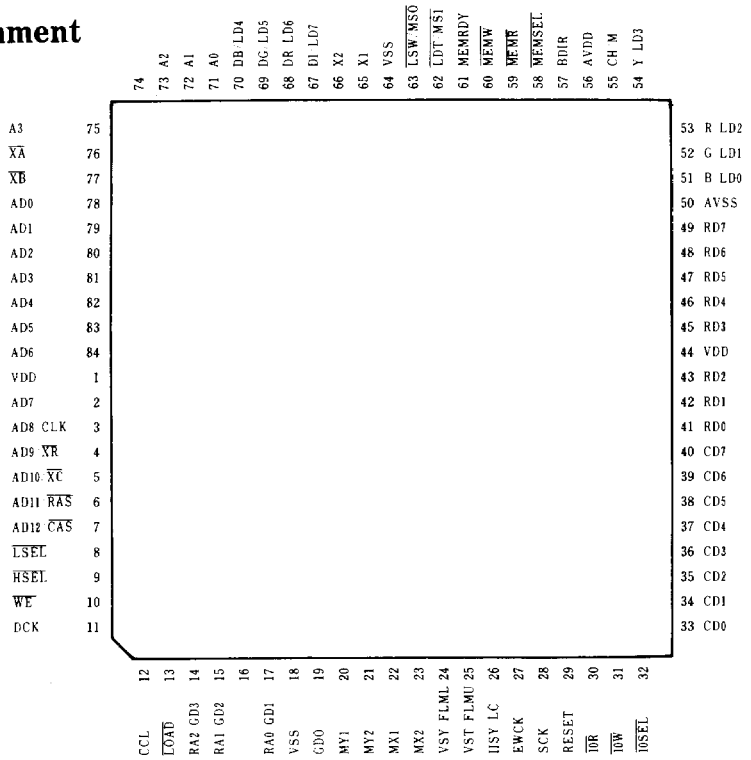


■ V6355D-F Package Dimensions

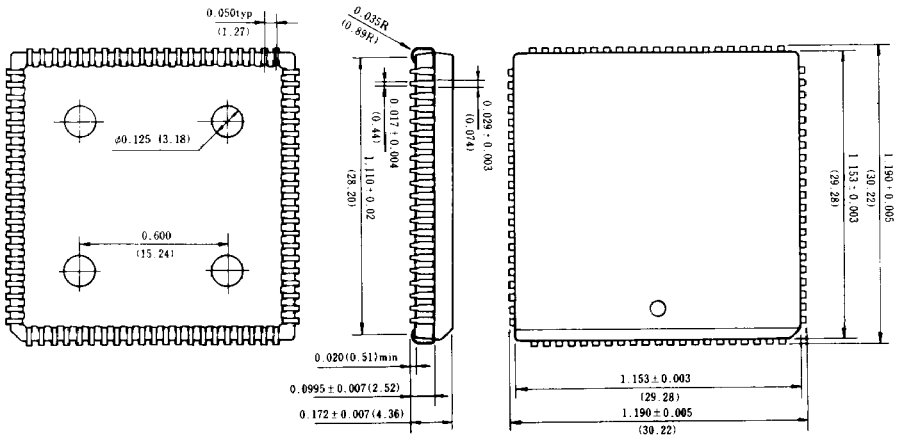
Base of package



■ V6355D-J Pin Assignment



■ V6355D-J Package Dimensions



The specifications of this product are subject to improvement changes without prior notice.

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