V62C1161024L(L)

Ultra Low Power
64K x 16 CMOS SRAM

Features

- **Ultra Low-power consumption**
  - **Active: 30mA I_{CC} at 70ns**
  - **Stand-by: 5 µA (CMOS input/output)**
    1 µA (CMOS input/output, L version)
- **70/85/100/120 ns access time**
- **Equal access and cycle time**
- **Single +1.8V to 2.2V Power Supply**
- **Tri-state output**
- **Automatic power-down when deselected**
- **Multiple center power and ground pins for improved noise immunity**
- **Individual byte controls for both Read and Write cycles**
- **Available in 44 pin TSOP (II) Package**

Functional Description

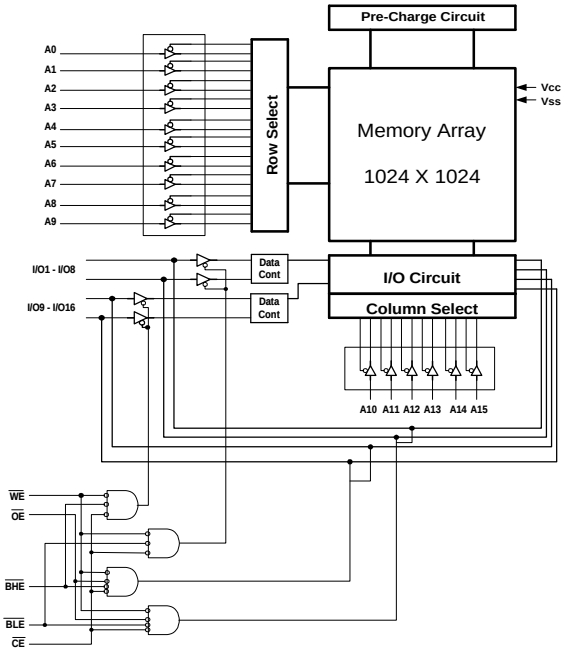
The V62C1161024L is a Low Power CMOS Static RAM organized as 65,536 words by 16 bits. Easy memory expansion is provided by an active LOW ($\overline{CE}$) and ($\overline{OE}$) pin.

This device has an automatic power-down mode feature when deselected. Separate Byte Enable controls ($\overline{BLE}$ and $\overline{BHE}$) allow individual bytes to be accessed. $\overline{BLE}$ controls the lower bits I/O1 - I/O8. $\overline{BHE}$ controls the upper bits I/O9 - I/O16.

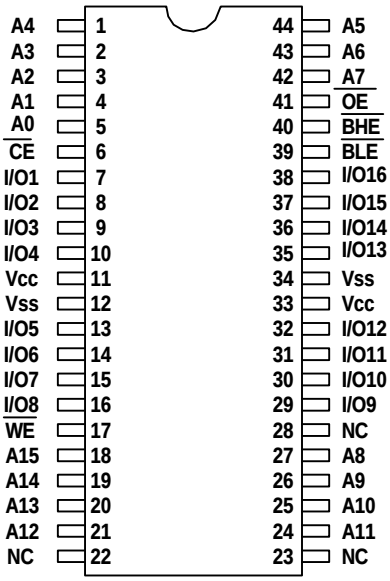
Writing to these devices is performed by taking Chip Enable ($\overline{CE}$) with Write Enable ($\overline{WE}$) and Byte Enable ($\overline{BLE}$/$\overline{BHE}$) LOW.

Reading from the device is performed by taking Chip Enable ($\overline{CE}$) with Output Enable ($\overline{OE}$) and Byte Enable ($\overline{BLE}$/$\overline{BHE}$) LOW while Write Enable ($\overline{WE}$) is held HIGH.

Logic Block Diagram



TSOP(II)



Absolute Maximum Ratings *

Parameter	Symbol	Minimum	Maximum	Unit
Voltage on Any Pin Relative to Gnd	Vt	-0.5	+4.0	V
Power Dissipation	PT	–	1.0	W
Storage Temperature (Plastic)	Tstg	-55	+150	^{0}C
Temperature Under Bias	Tbias	-40	+85	^{0}C

*** Note:** Stresses greater than those listed above Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and function operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect reliability.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O1-I/O8	I/O9-I/O16	Power	Mode
H	X	X	X	X	High-Z	High-Z	Standby	Standby
L	L	H	L	H	Data Out	High-Z	Active	Low Byte Read
L	L	H	H	L	High-Z	Data Out	Active	High Byte Read
L	L	H	L	L	Data Out	Data Out	Active	Word Read
L	X	L	L	L	Data In	Data In	Active	Word Write
L	X	L	L	H	Data In	High-Z	Active	Low Byte Write
L	X	L	H	L	High-Z	Data In	Active	High Byte Write
L	H	H	X	X	High-Z	High-Z	Active	Output Disable
L	X	X	H	H	High-Z	High-Z	Active	Output Disable

*** Key:** X = Don't Care, L = Low, H = High

Recommended Operating Conditions (T_A = 0^{o}C to +70^{o}C / -40^{o}C to 85^{o}C**)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	1.8	2.0	2.2	V
	Gnd	0.0	0.0	0.0	V
Input Voltage	V_{IH}	1.6	-	V_{CC} + 0.2	V
	V_{IL}	-0.5*	-	0.4	V

***** V_{IL} min = -2.0V for pulse width less than t_{RC}/2.

****** For Industrial Temperature

DC Operating Characteristics (V_{CC} = 2V±10%, Gnd = 0V, T_A = 0^0C to +70^0C / -40^0C to 85^0C)

Parameter	Sym	Test Conditions		-70		-85		-100		-120		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = Max, V_{in} = Gnd to V_{CC}		-	1	-	1	-	1	-	1	µA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CE}$ = V_{IH} or V_{CC}= Max, V_{OUT} = Gnd to V_{CC}		-	1	-	1	-	1	-	1	µA
Operating Power Supply Current	I_{CC}	$\overline{CE}$ = V_{IL} , V_{IN} = V_{IH} or V_{IL} , I_{OUT} = 0		-	3	-	3	-	3	-	3	mA
Average Operating Current	I_{CC1}	I_{OUT} = 0mA, Min Cycle, 100% Duty		-	30	-	25	-	20	-	20	mA
	I_{CC2}	$\overline{CE}$ ≤ 0.2V I_{OUT} = 0mA, Cycle Time=1µs, Duty=100%		-	3	-	3	-	3	-	3	mA
Standby Power Supply Current (TTL Level)	I_{SB}	$\overline{CE}$ = V_{IH}		-	0.5	-	0.5	-	0.5	-	0.5	mA
Standby Power Supply Current (CMOS Level)	I_{SB1}	$\overline{CE}$ ≥ V_{CC} - 0.2V V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC}- 0.2V	L	-	5	-	5	-	5	-	5	µA
			LL	-	*1*	-	*1*	-	*1*	-	*1*	µA
Output Low Voltage	V_{OL}	I_{OL} = 2 mA		-	0.4	-	0.4	-	0.4	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1 mA		1.6	-	1.6	-	1.6	-	1.6	-	V

Capacitance (f = 1MHz, T_A = 25^0C)

Parameter*	Symbol	Test Condition	Max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	7	pF
I/O Capacitance	$C_{I/O}$	V_{in} = V_{out} = 0V	8	pF

* This parameter is guaranteed by device characterization and is not production tested.

AC Test Conditions

Input Pulse Level	0.4V to 1.6V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	1.0V
Output Load Condition	
70ns/85ns	C_L = 30pf + 1TTL Load
Load for 100ns/120ns	C_L = 100pf + 1TTL Load

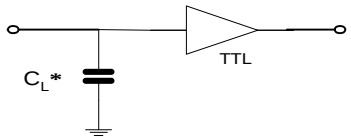


Figure A. * Including Scope and Jig Capacitance

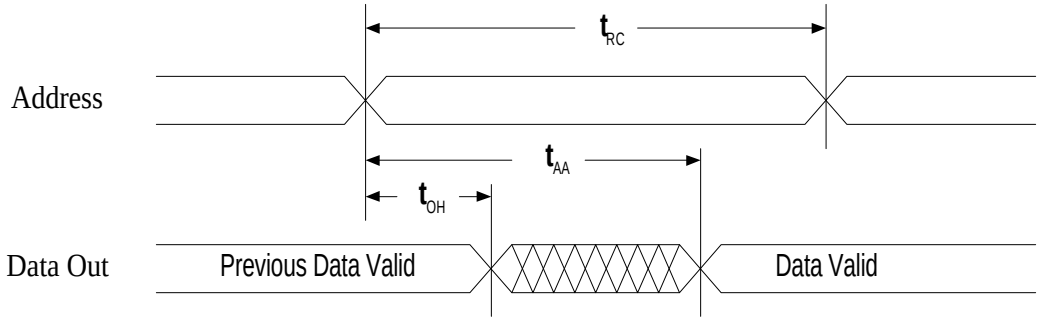
Read Cycle [9] (V_{cc} = 2V±0.2V, Gnd = 0V, T_A = 0^0C to +70^0C / -40^0C to +85^0C)

Parameter	Sym	-70		-85		-100		-120		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{RC}	70	-	85	-	100	-	120	-	ns	
Address Access Time	t_{AA}	-	70	-	85	-	100	-	120	ns	
Chip Enable Access Time	t_{ACE}	-	70	-	85	-	100	-	120	ns	
Output Enable Access Time	t_{OE}	-	40	-	40	-	50	-	60	ns	
Output Hold from Address Change	t_{OH}	10	-	10	-	10	-	10	-	ns	
Chip Enable to Output in Low-Z	t_{LZ}	10	-	10	-	10	-	10	-	ns	4,5
Chip Disable to Output in High-Z	t_{HZ}	-	30	-	35	-	40	-	40	ns	3,4,5
Output Enable to Output in Low-Z	t_{OLZ}	5	-	5	-	5	-	5	-	ns	
Output Disable to Output in High-Z	t_{OHZ}	-	25	-	30	-	35	-	40	ns	
$\overline{BLE}$, $\overline{BHE}$ Enable to Output in Low-Z	t_{BLZ}	5	-	5	-	5	-	5	-	ns	4,5
$\overline{BLE}$, $\overline{BHE}$ Disable to Output in High-Z	t_{BHZ}	-	25	-	30	-	35	-	40	ns	3,4,5
$\overline{BLE}$, $\overline{BHE}$ Access Time	t_{BA}	-	40	-	40	-	50	-	60	ns	

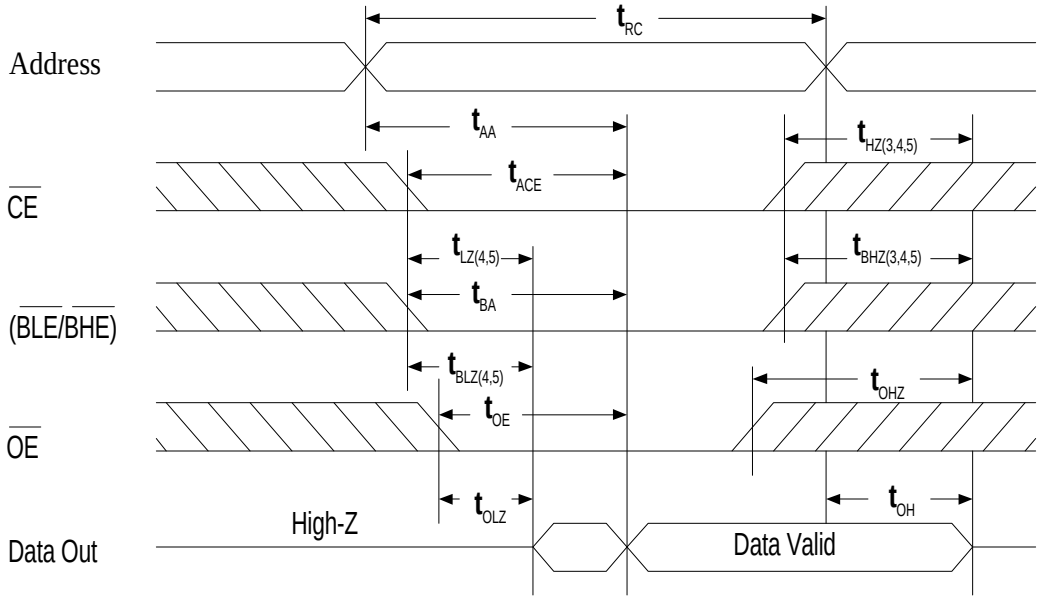
Write Cycle [11] (V_{cc} =2V±0.2V, Gnd = 0V, T_A = 0^0C to +70^0C / -40^0C to +85^0C)

Parameter	Symbol	-70		-85		-100		-120		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{WC}	70	-	85	-	100	-	120	-	ns	
Chip Enable to Write End	t_{CW}	60	-	70	-	80	-	90	-	ns	
Address Setup to Write End	t_{AW}	60	-	70	-	80	-	40	-	ns	
Address Setup Time	t_{AS}	0	-	0	-	0	-	0	-	ns	
Write Pulse Width	t_{WP}	50	-	60	-	70	-	80	-	ns	
Write Recovery Time	t_{WR}	0	-	0	-	0	-	0	-	ns	
Data Valid to Write End	t_{DW}	30	-	35	-	40	-	45	-	ns	
Data Hold Time	t_{DH}	0	-	0	-	0	-	0	-	ns	
Write Enable to Output in High-Z	t_{WHZ}	-	30	-	35	-	40	-	40	ns	
Output Active from Write End	t_{OW}	5	-	5	-	5	-	5	-	ns	
$\overline{BLE}$, $\overline{BHE}$ Setup to Write End	t_{BW}	60	-	70	-	80	-	90	-	ns	

Timing Waveform of Read Cycle 1 (Address Controlled)



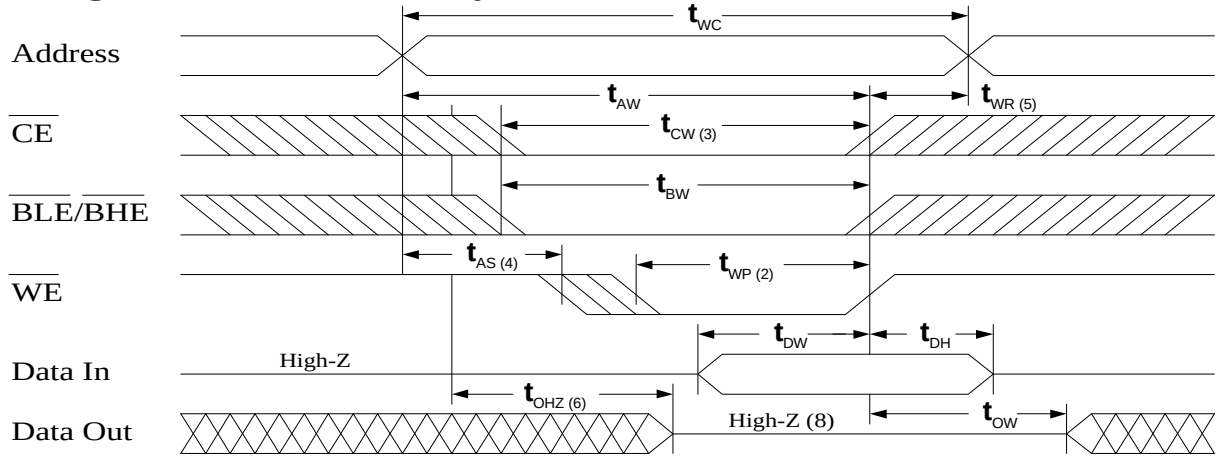
Timing Waveform of Read Cycle 2



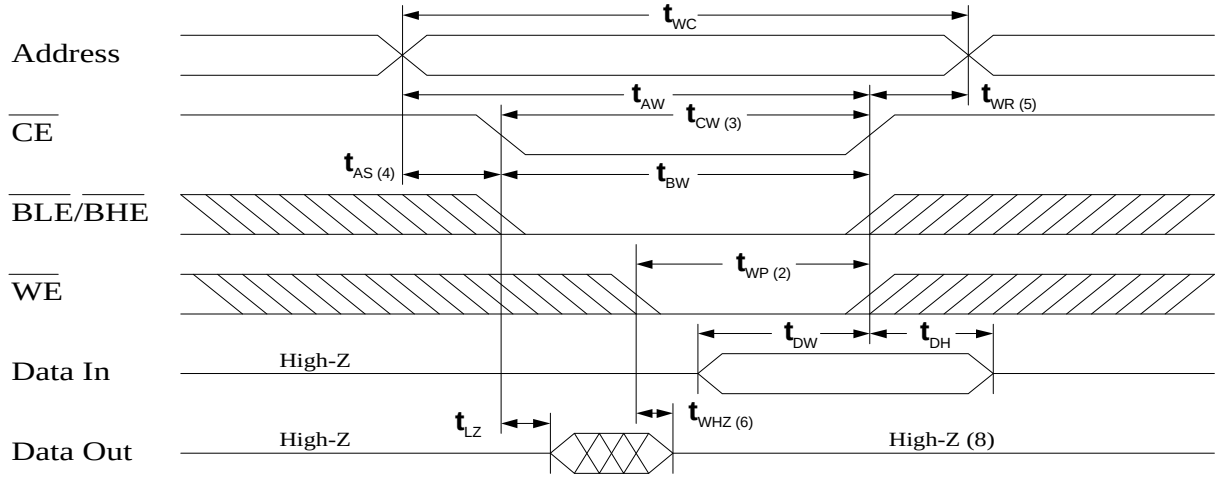
Notes (Read Cycle)

1. WE are high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.
5. Transition is measured ± 200mV from steady state voltage with load. This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CE}$ = V_{IL}.
7. Address valid prior to coincident with $\overline{CE}$ transition Low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
9. For test conditions, see *AC Test Condition*, Figure A.

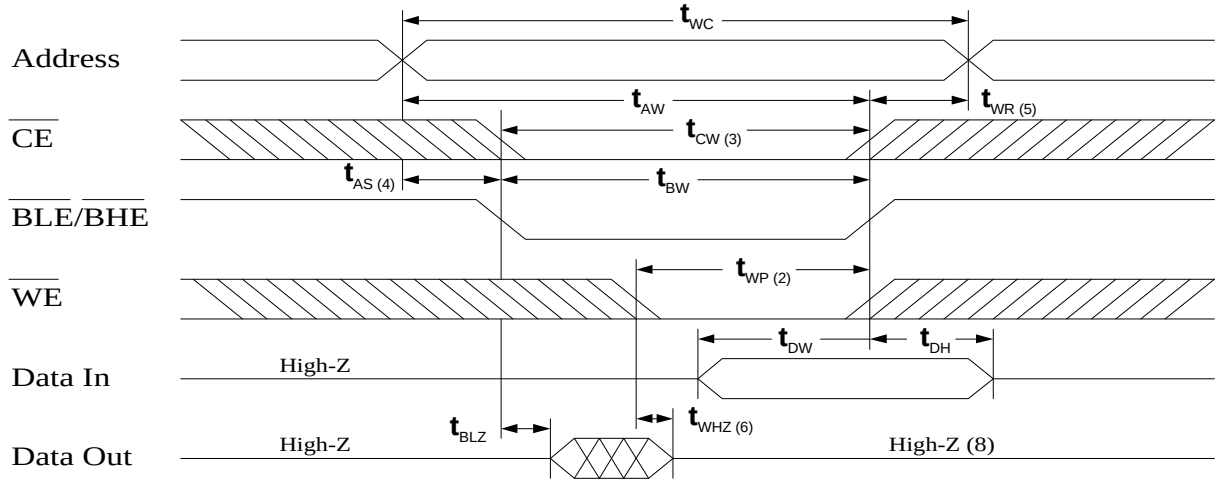
Timing Waveform of Write Cycle 1 (Address Controlled)



Timing Waveform of Write Cycle 2 ($\overline{CE}$ Controlled)



Timing Waveform of Write Cycle 3 ($\overline{BLE}$/$\overline{BHE}$ Controlled)



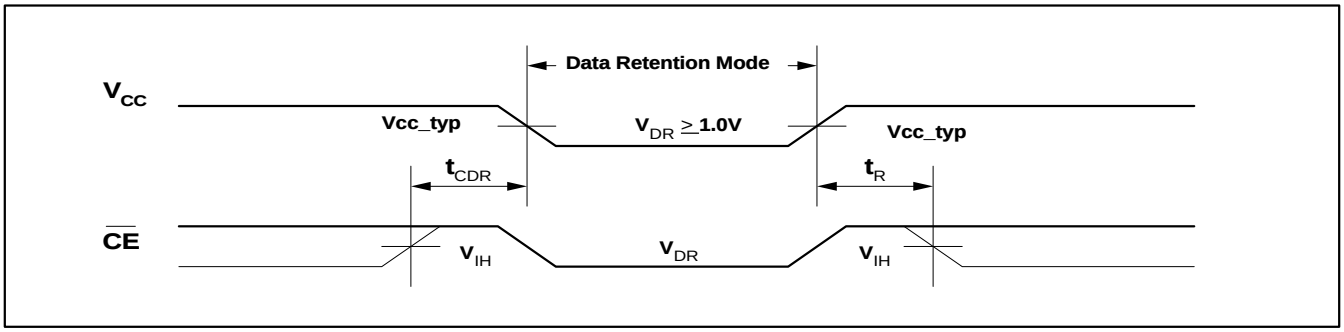
Notes (Write Cycle)

1. All write timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CE}$ and $\overline{WE}$. A write begins at the latest transition among $\overline{CE}$ and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CE}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CE}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change.
6. If $\overline{OE}$, $\overline{CE}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output Low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. D_{OUT} is the read data of the new address.
10. When $\overline{CE}$ is low: I/O pins are in the outputs state. The input signals in the opposite phase leading to the output should not be applied.
11. For test conditions, see *AC Test Condition*, Figure A & B.

Data Retention Characteristics (L Version Only)[1]

Parameter	Symbol	Test Condition	Min	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CE} \geq V_{CC}$ - 0.2V	1.0	-	V
Data Retention Current	I_{CCDR}	L	-	5 1	µA
Chip Deselect to Data Retention Time	t_{CDR}	$V_{IN} \geq V_{CC}$ - 0.2V or	0	-	ns
Operation Recovery Time[2]	t_R	$V_{IN} \leq$ 0.2V	t_{RC}	-	ns

Data Retention Waveform (L Version Only) (T_A = 0^0C to +70^0C / -40^0C to +85^0C)



Notes

1. L-version includes this feature.
2. This Parameter is sampled and not 100% tested.
3. For test conditions, see *AC Test Condition*, Figure A.
4. This parameter is tested with CL = 5pF as shown in Figure B. Transition is measured ± 500mV from steady-state voltage.
5. This parameter is guaranteed, but is not tested.
6. $\overline{WE}$ is High for read cycle.
7. $\overline{CE}$ and $\overline{OE}$ are LOW for read cycle.
8. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
9. All read cycle timings are referenced from the last valid address to the first transtion address.
10. $\overline{CE}$ or $\overline{WE}$ must be HIGH during address transition.
11. All write cycle timings are referenced from the last valid address to the first transition address.

Ordering Information

Device Type*	Speed	Package
V62C1161024L-70T	70 ns	44-pin TSOP Type 2
V62C1161024L-85T	85 ns	
V62C1161024L-100T	100 ns	
V62C1161024L-120T	120 ns	
V62C1161024LL-70T	70 ns	
V62C1161024LL-85T	85 ns	
V62C1161024LL-100T	100 ns	
V62C1161024LL-120T	120 ns	

*** For Industrial temperature tested devices, an "I" designator will be added to the end of the device number.**

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