40 Segment Static LCD Driver

Features

- Serial data input / output
- Low dynamic current, 5 µA max.
- Low standby current, 1 µA max.
- Separate input and display voltages
- Wide power supply range:
  V_{DD} (logic) 2 to 8 V, V_{LCD} (display) V_{DD} to 12 V
- On-chip latches separate control and display sections
- Drives up to 40 LCD segments in direct drive
- Crossfree cascadable
- Schmitt Trigger on the inputs
- 30 ns (typ.) glitch filter on every input
- High noise immunity
- Segment outputs short circuit protected
- LCD blanking function
- - 40 to +85 °C temperature range
- On request extended temperature range,
  - 40 to +125 °C
- QFP52 and TAB packages

Description

The V6108 is a CMOS integrated circuit that drives LCD. The circuit drives up to 40 LCD segments from a serial clocked input. It has a serial output for cascading to further drives. The serially clocked data is parallel loaded into 40 latches under control of the strobe pin. The latched data determines which segments are ON or OFF. Any segment output can be used to drive a backplane. A blank function is provided to clear the display.

Applications

- Balances and scales
- Automotive displays
- Utility meters
- Large displays
- Pagers
- Portable, battery operated products
- Telephones

Typical Operating Configuration

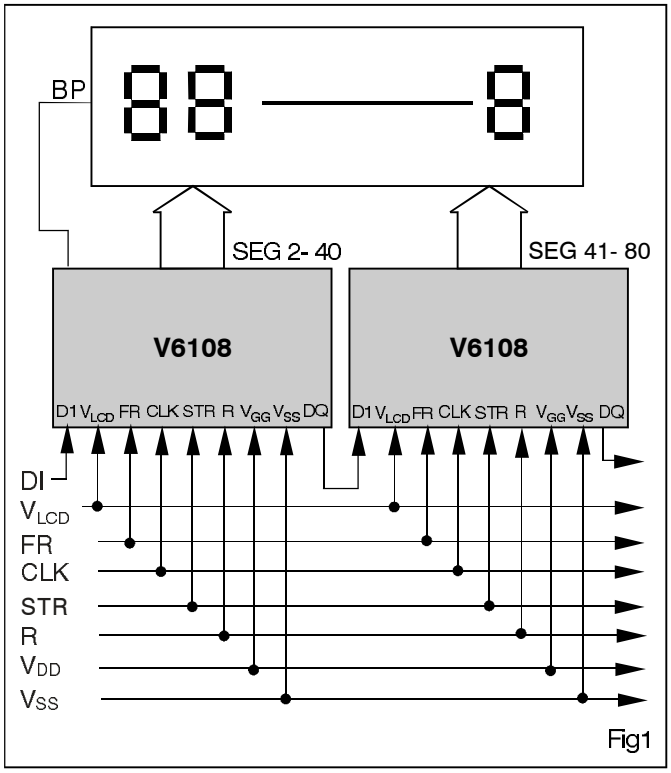


Fig1

Pin Assignment

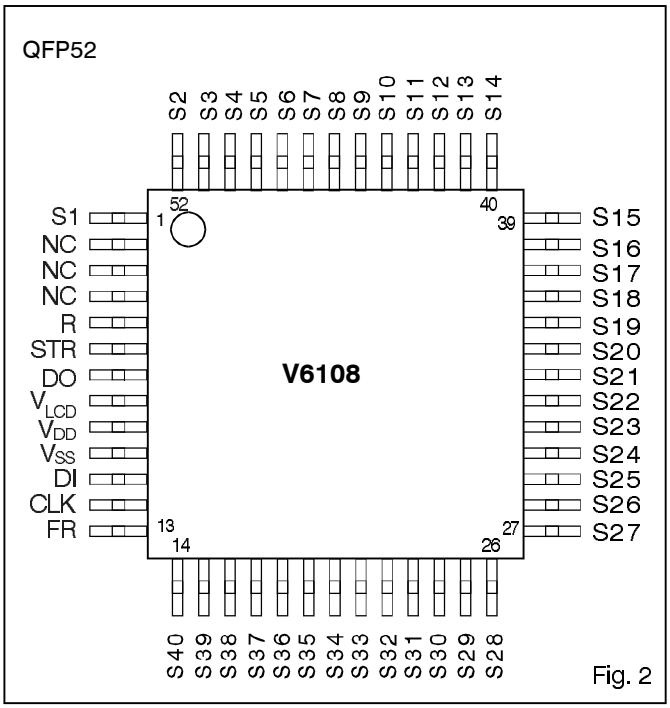


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Logic supply voltage	V_{DD}	-0.3V to +10V
LCD supply voltage [1]	V_{LCD}	-0.3V to +14V
Voltage at DI, CLK,STR, FR, R, DO	V_{LOGIC}	-0.3V to V_{DD}+0.3V
Voltage at S1 to S40	V_{DISP}	V_{DD} to V_{LCD} + 0.3V
Storage temperature range	T_{STO}	- 65 to +150 °C
Power dissipation	P_{MAX}	100 mW
Electrostatic discharge max. to MIL-STD-883 C method 3015	V_{Smax}	1000V
Max. soldering conditions	T_S	250 °C x 10 s

[1] V_{LCD} has to be higher or equal to V_{DD} Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature [1]	T_A	-40		+125	°C
Logic supply voltage	V_{DD}	2.0		8	V
LCD supply voltage	V_{LCD}	V_{DD}		12	V

[1] The maximum operating temperature is confirmed by sampling at initial device qualification. In production, all devices are tested at +85 °C. On request devices tested at +125°C can be supplied. Table 2

Electrical Characteristics

V_{DD} = 5V ± 10%, V_{LCD} = 12 V and T_A = -40 to 85 °C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Static supply current	I_{DD}	See note [1]		0.1	1	µA
Static supply current	I_{LCD}	See note [1]		0.1	1	µA
Dynamic supply current	I_{DD}	See note [1][2]		55	75	µA
Dynamic supply current	I_{LCD}	See note [1][3]		0.6	5	µA
All Input Signals						
Low level input voltage	V_{IL}				0.8	V
High level input voltage	V_{IH}		3.8	3.5		V
Leakage Input current	I_{IL}	V_{IN} = V_{SS} or V_{IN} = V_{DD}			1	µA
Data Output DO						
High level output voltage	V_{OH}	I_H = 100 µA V_{DD} = V_{LCD} = 4.5 V	V_{DD} - 100			mV
Low level output voltage	V_{OL}	I_L = 100 µA V_{DD} = V_{LCD} = 4.5 V			V_{SS} + 100	mV
Driver Outputs S1...S40						
High level output voltage	V_{SH}	I_H = 20 µA, V_{DD} = V_{LCD} = 4.5 V	V_{LCD}- 100			mV
Low level output voltage	V_{SL}	I_L = 20 µA, V_{DD} = V_{LCD} = 4.5 V			V_{SS} + 100	mV
Short Circuit Current	I_{SC}	only one output		0.9	2	mA

[1] Tested with V_{IL} = V_{SS}, V_{IH} = V_{DD} Table 3

[2] Tested with f_{CL} = 100 kHz, F_{DI} = 50 kHz, 50 pF on each segment

[3] Tested with f_{FL} = 64 Hz, f_{CL} = 0 Hz, 50 pF on each segment

Timing Characteristics

V_{DD} = 5V ± 10%, V_{LCD} = 12 V and T_A = -40 to +85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Clock high pulse width	t_{CH}		500			ns
Clock low pulse width	t_{CL}		500			ns
Clock and FR rise time	t_{CR}				500	ns
Clock and FR fall time	t_{CF}				500	ns
Data input setup time	t_{DS}		250			ns
Data input hold time	t_{DH}		0			ns
Data output propagation	t_{PD}	C_{LOAD} = 50 pF		600	800	ns
CLK falling to STR rising	t_P		50			ns
STR falling to CLK falling	t_D		250			ns
STR pulse width	t_{STR}		200			ns
FR frequency	f_{FR}			64 Hz[1]	1[2]	MHz
Delay S1 - S40 fall time	t_{SF}			0.5	1	µs
Delay S1 - S40 rise time	t_{SR}			2.9	5	µs

[1] Recommended frame frequency. [2] Maximum test frequency. Table 4

Timing Waveforms

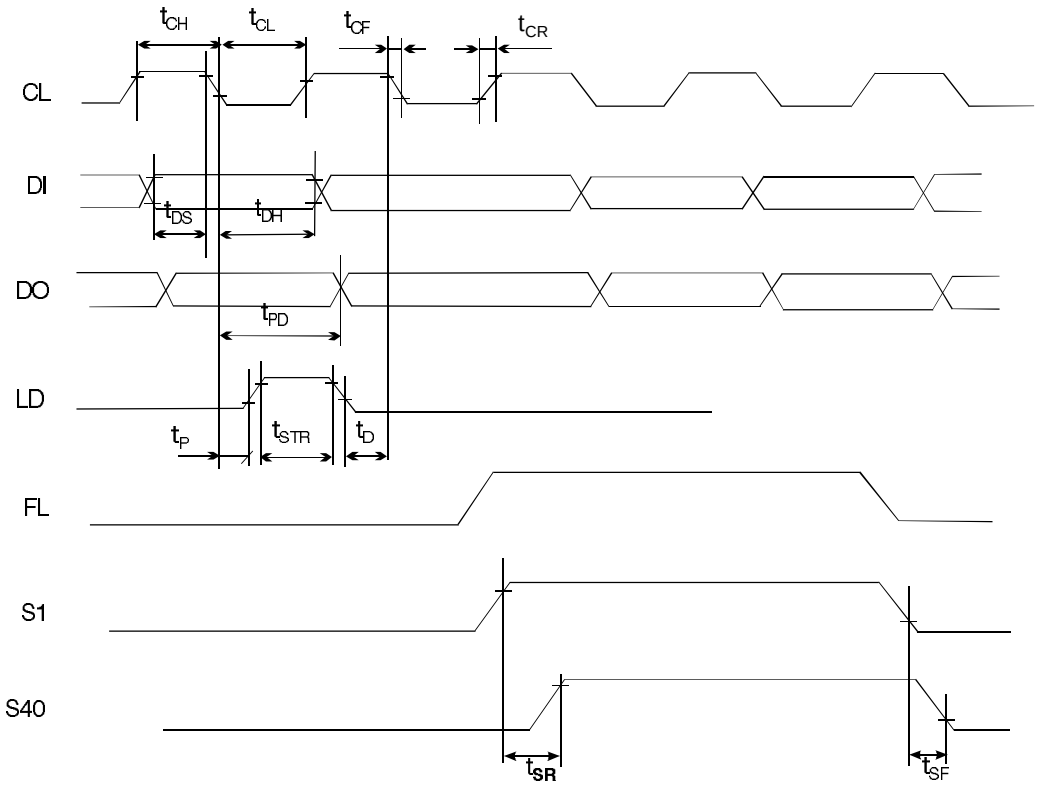


Fig. 3

V_{OL} S1 ... S40 versus V_{LCD} at -40 °C, +25 °C and +85 °C

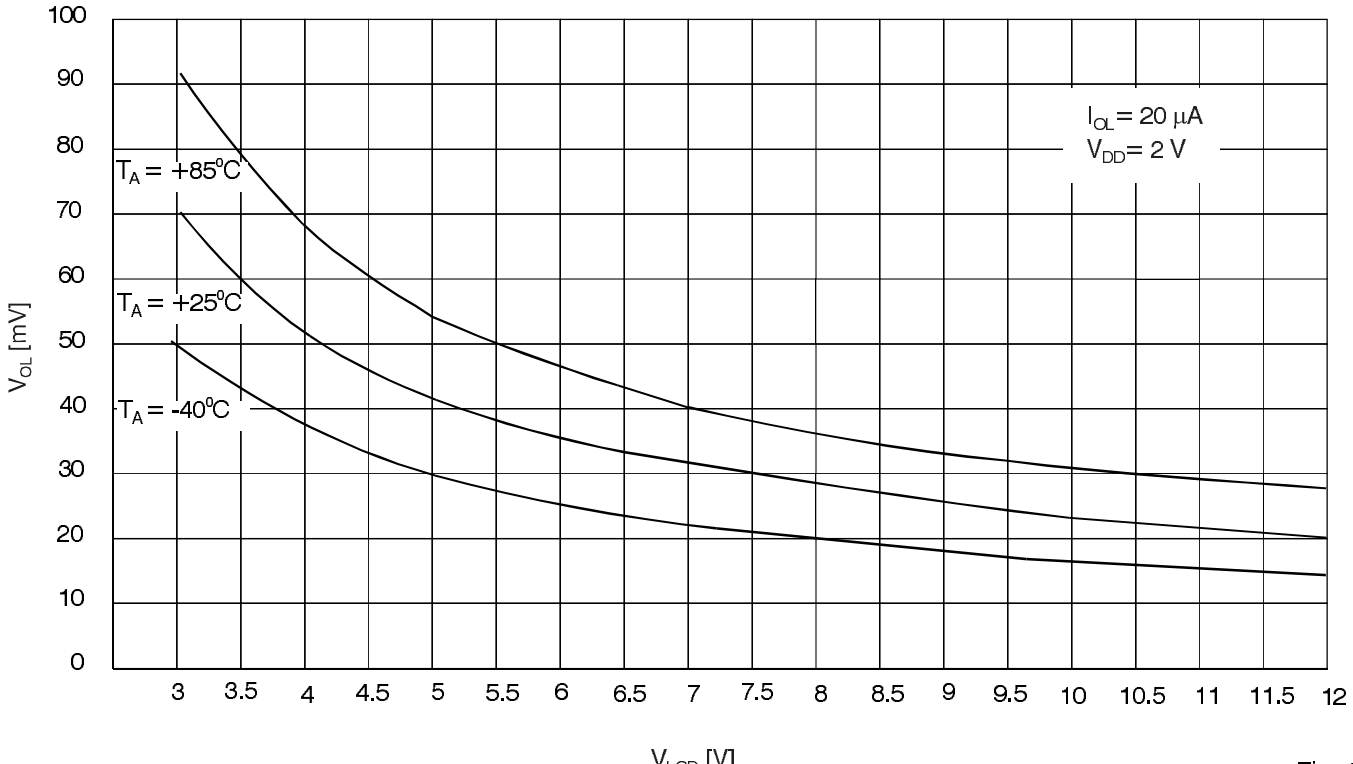


Fig. 4

V_{OH} S1 ... S40 versus V_{LCD} at – 40 °C, +25 °C and+85 °C

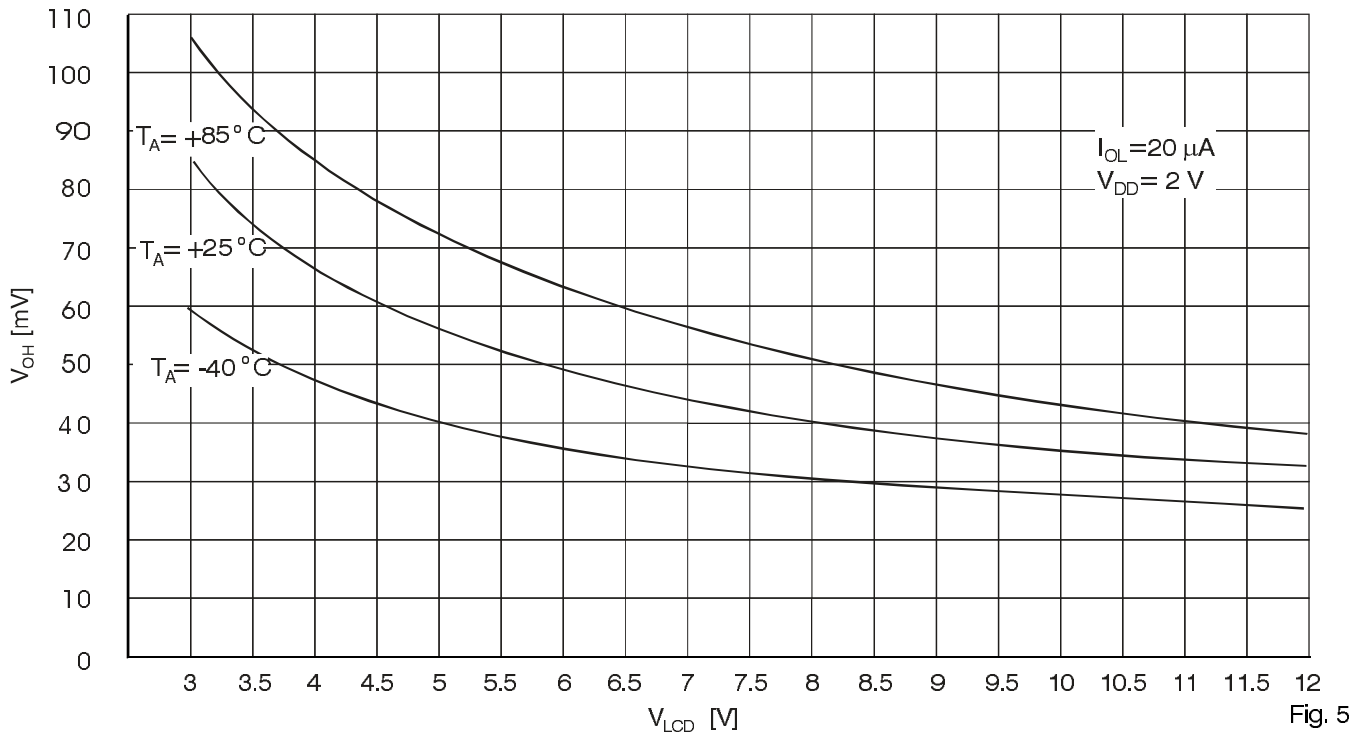


Fig. 5

V_{OL} DO versus V_{DD} at – 40°C, +25°C and +85°C

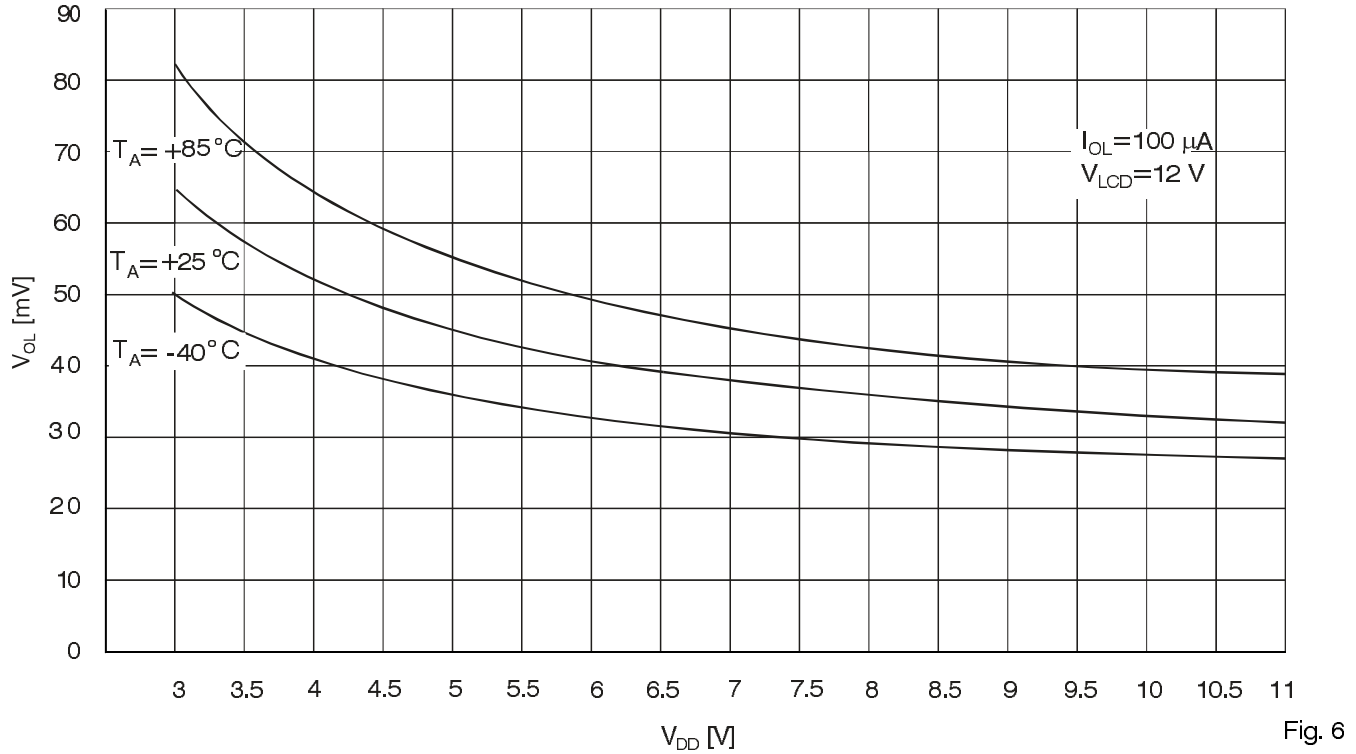


Fig. 6

V_{OH} DO versus V_{DD} at -40°C, + 25°C and +85°C

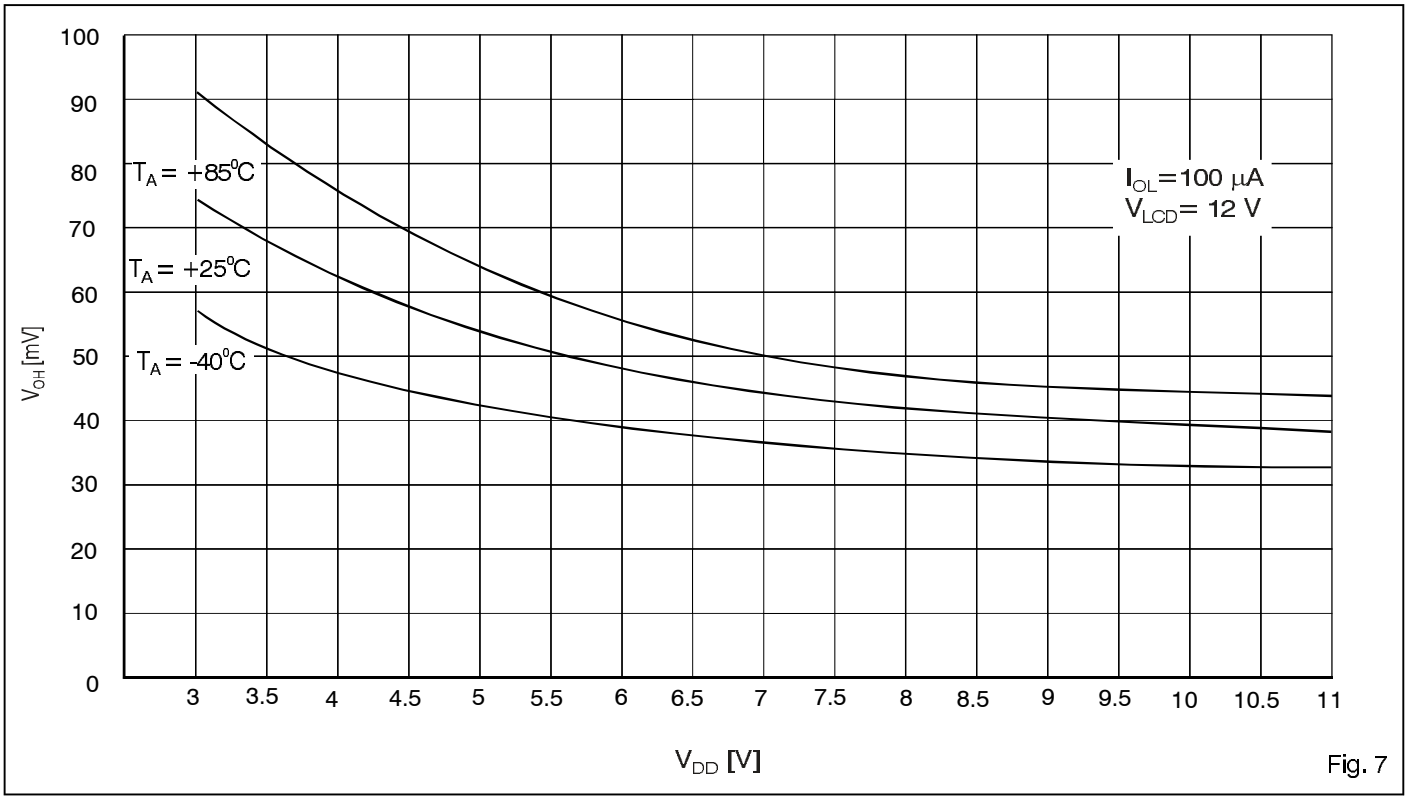
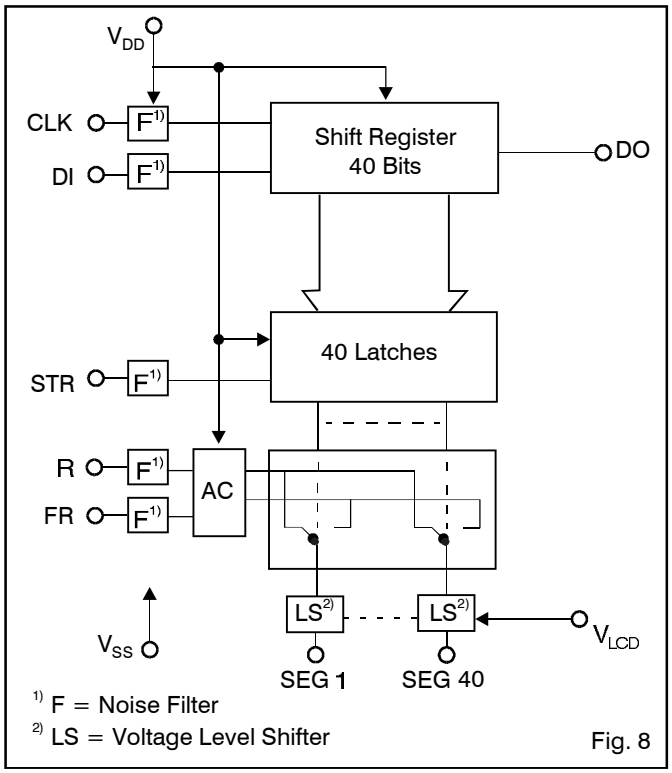


Fig. 7

Block Diagram



1) F = Noise Filter
2) LS = Voltage Level Shifter

Fig. 8

Pin Assignments

Name	Function
S1...S40	Segment drive outputs
V_{LCD}	Power supply for the LCD
V_{DD}	Power supply for logic
FR	Input for segment frequency control
DI	Serial data input
DO	Serial data output
CLK	Clock input
STR	Strobes the input data into the output latches
R	Display blank control input
V_{SS}	Supply ground

Table 5

Functional Description

Supply Voltages V_{LCD}, V_{DD}, V_{SS}

V_{DD} is the positive supply line for the logic and V_{LCD} for the display signals. V_{LCD} has to be equal or higher than V_{DD}. All voltages are specified relative to V_{SS}.

Data Input / Output (DI / DO)

The data input pin (DI) accepts serial data from the data source. The data is clocked in a rate determined by the clock input frequency (CLK). A logic "1" on DI corresponds to a visible segment when the backplane is driven by a signal corresponding to logic "0". The data at DO is equal to the data at DI delayed by 40 clock periods. In

order to cascade devices the DO of one chip must be connected to DI of the following chip (see Fig. 1).

CLK Input
The clock input pin (CLK) is used to clock the DI serial data into the 40-bit shift register. Loading, shifting and outputting of the data occurs at the falling edge of this clock (see Fig. 3). When cascading devices, all CLK lines should be tied together.

STR Input
The strobe input pin (STR) is used to latch the input data shifted into the 40-bit shift register. The latched data is held for display. A logic "1" on the STR input transfers the data contained in the shift register cells to the corresponding latches. The latches remain open during the whole time STR remains at logic "1". When cascading devices the STR lines should all be connected.

R Input
When R is active (high), the display is blanked: all segment outputs are tied to V_{SS}. R does not clear the information in the latches.

Segment Driver
The number of segment drivers available on the chip is 40. Each segment driver can be used as backplane-driver. If two or more drivers are connected together, care must be taken to ensure the drivers do not cause circuit malfunction by driving one against the other.

FR Input
This input controls the segment output switching frequency according to Table 6. It must be connected to an external clock signal. When cascading devices, their FR inputs may all be connected to a common signal.

Segment Switching Table

Latched Signal (DI) $0 = V_{IL}$ $1 = V_{IH}$	Signal FR	Segment Voltage $0 = V_{SS}$ $1 = V_{LCD}$
0	0	0
0	1	1
1	0	1
1	1	0

Table 6

Typical Applications
Type V 6108 Circuits Driving an 79 Segment Display

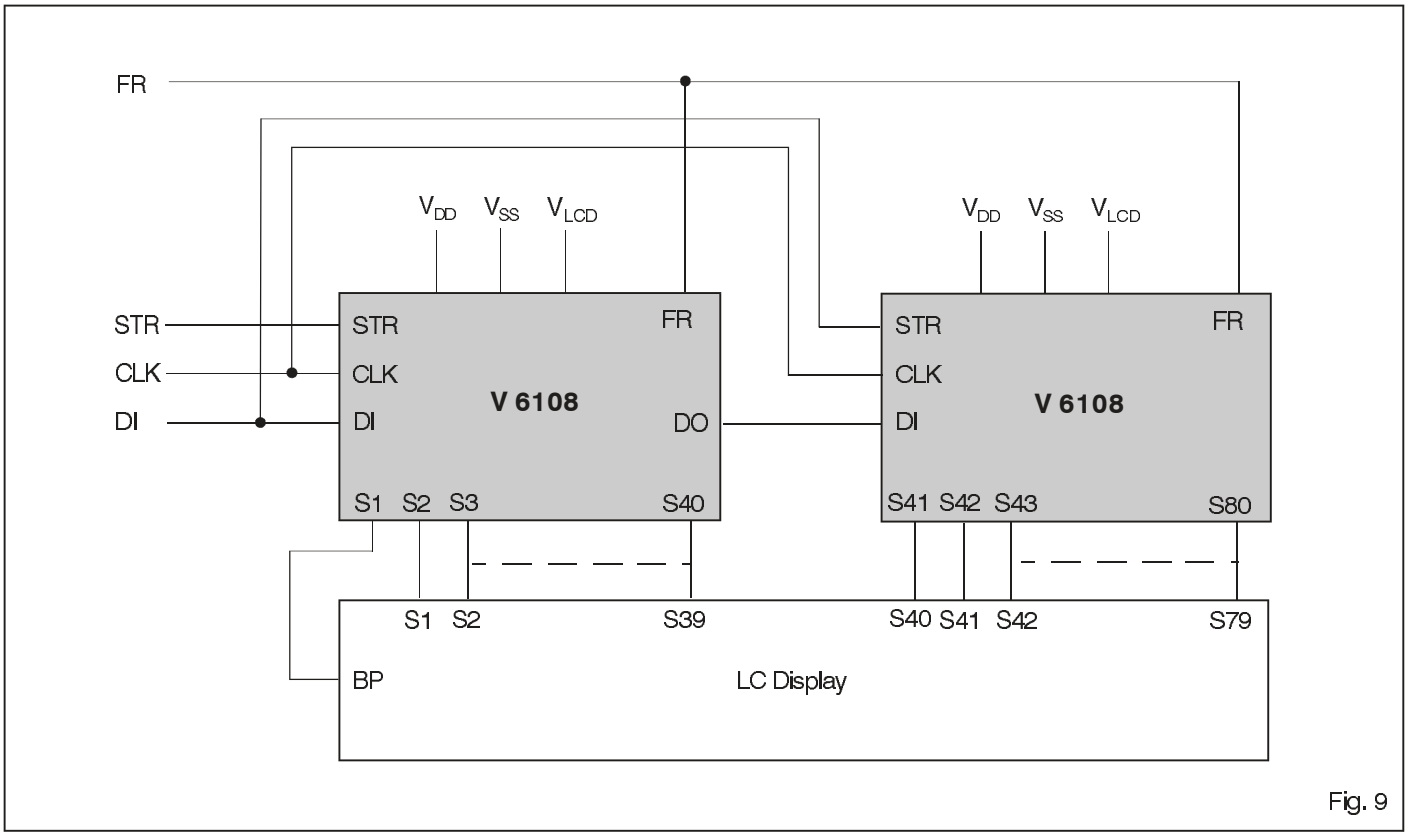


Fig. 9

Cascaded V6108 TAB for Direct Drive Application

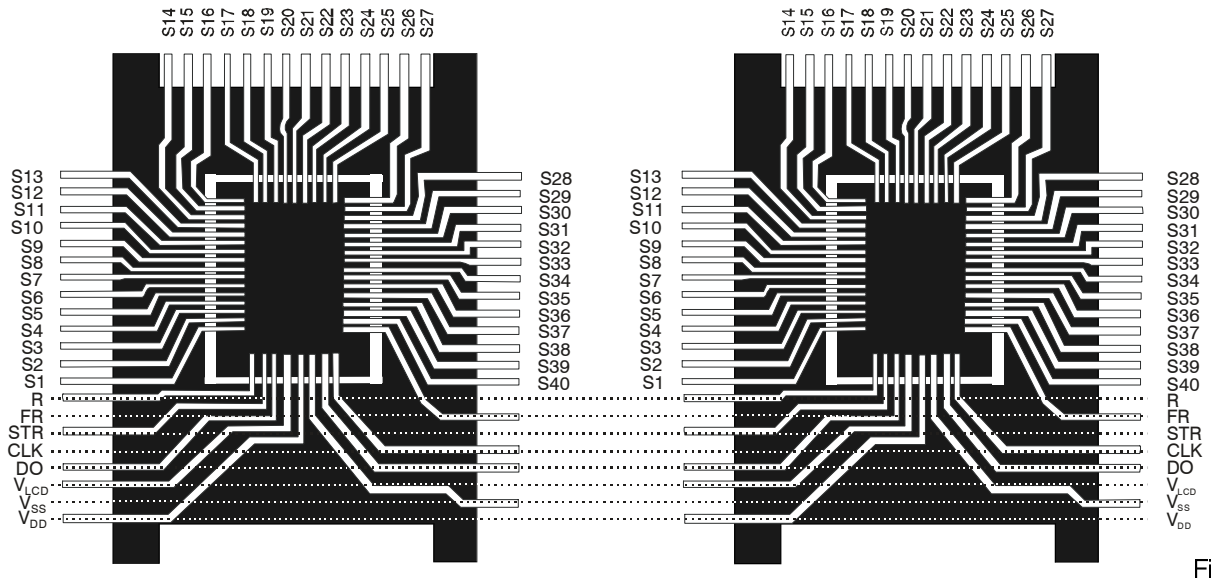
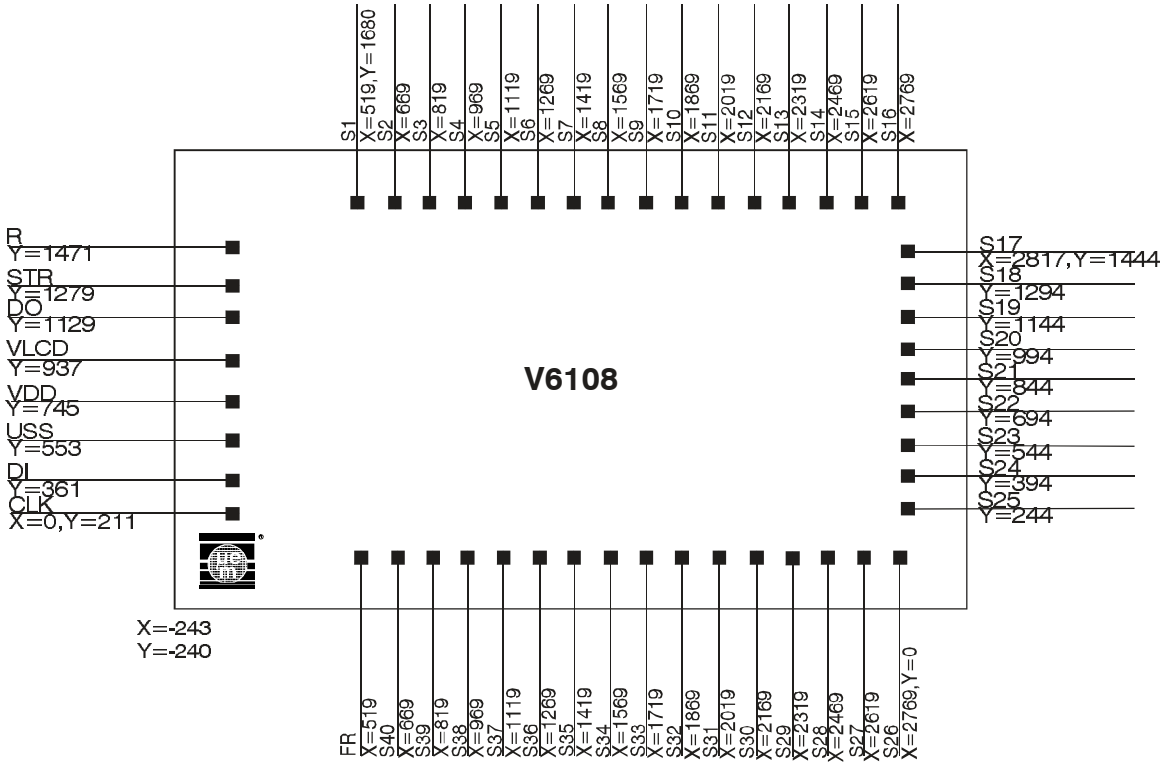


Fig. 10

Package and Ordering Information

Dimensions of Chip Form



Chip size is X= 3302 by Y= 2159 microns or X= 130 by Y= 85 mils

Note: The origin(0,0) is the lower left coordinate of center pads.
The lower left corner of the chip shows distances to origin.

Dimensions in microns

Fig. 11

Side View and Recommended Solder Area

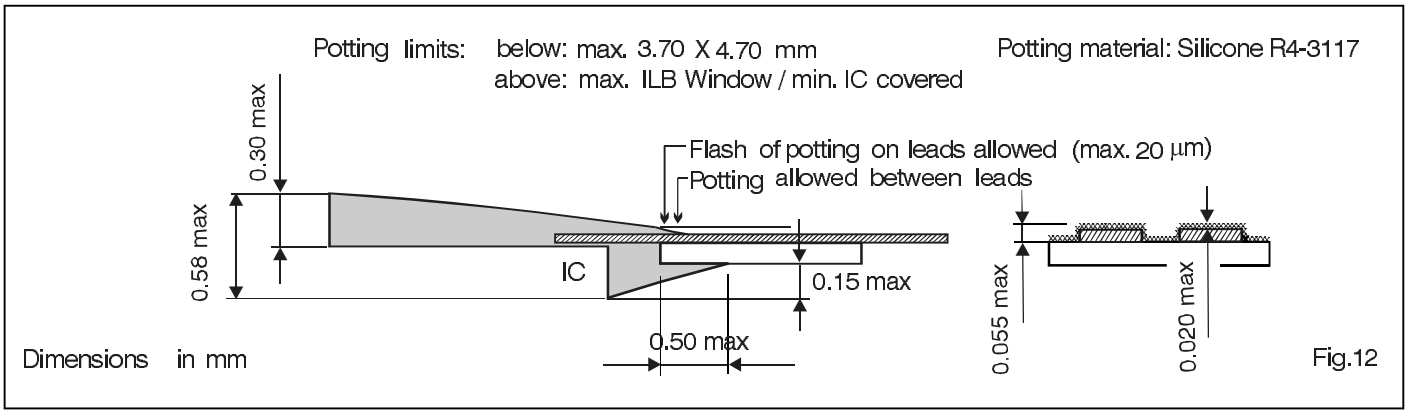


Fig.12

Package and Ordering Information

The V 6108 is available in the following packages:

QFP52, pin plastic package	V6108 52F
TAB, tape automated bonding	V6108 TAB
Chip form	V6108 Chip *

When ordering, please specify the complete part number and package.

* on request