



- ☐ Tentative Specification
- ☐ Preliminary Specification
- ☒ Approval Specification

**MODEL NO.: V400H1**  
**SUFFIX: LH9**

**Customer: SEC**

**APPROVED BY**

**SIGNATURE**

Name / Title

**Note**

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
Chao-Chun Chung	Josh Chi	Joanne Chung

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**REVISION HISTORY**

Version	Date	Page (New)	Section	Description
Ver 2.0	Nov. 19,'09	All	All	Approval Specification was first issued.
Ver 2.1	Jan. 19,'11	31	9.2	Modify Figure.9-1 packing method.(add 2pcs drier)
www.panelook.com				



## 1. GENERAL DESCRIPTION

### 1.1 OVERVIEW

V400H1- LH9 is a 40" TFT Liquid Crystal Display module with 12-CCFL Backlight unit and 4ch-LVDS interface. This module supports 1920 x 1080 FHD format and can display true 1.07G (8-bit+Hi-FRC) colors. The Balance Board module for backlight is built-in.

### 1.2 FEATURES

- High brightness (500 nits)
- Ultra-high contrast ratio (6500:1)
- Faster response time (Gray to gray average 4.5ms)
- High color saturation NTSC 72%
- Ultra wide viewing angle: 176(H)/176(V) (CR>20) with Super MVA technology
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Color reproduction (nature color)
- Optimized response time for 100/120 Hz frame rate
- Low color shift function
- RoHS compliance

### 1.3 APPLICATION

- TFT LCD TVs
- Multi-Media Display

### 1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	885.6(H) x 498.15 (V) (40" diagonal)	mm	(1)
Bezel Opening Area	891.7 (H) x 504.8 (V)	mm	
Driver Element	a-si TFT active matrix	-	
Pixel Number	1920 x R.G.B. x 1080	pixel	
Pixel Pitch (Sub Pixel)	0.15375 (H) x 0.46125 (V)	mm	
Pixel Arrangement	RGB vertical stripe	-	
Display Colors	1.07G	color	
Display Operation Mode	Transmissive mode / Normally black	-	
Surface Treatment	Glare coating (Super Clear), Hard coating (3H)	-	

### 1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	951	952	953	mm	(1)
	Vertical(V)	550	551	552	mm	(1)
	Depth(D)	34	35	36	mm	To Rear
	Depth(D)	52.8	53.8	54.8	mm	To Inv Cover
Weight		-	9360	-	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

## 2. ABSOLUTE MAXIMUM RATINGS

### 2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T <sub>ST</sub>	-20	+60	°C	(1)
Operating Ambient Temperature	T <sub>OP</sub>	0	+50	°C	(1), (2)
Shock (Non-Operating)	S <sub>NOP</sub>	-	50	G	(3), (5)
Vibration (Non-Operating)	V <sub>NOP</sub>	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. ( $T_a \leq 40\text{ }^{\circ}\text{C}$ ).

(b) Wet-bulb temperature should be 39 °C Max. ( $T_a > 40\text{ }^{\circ}\text{C}$ ).

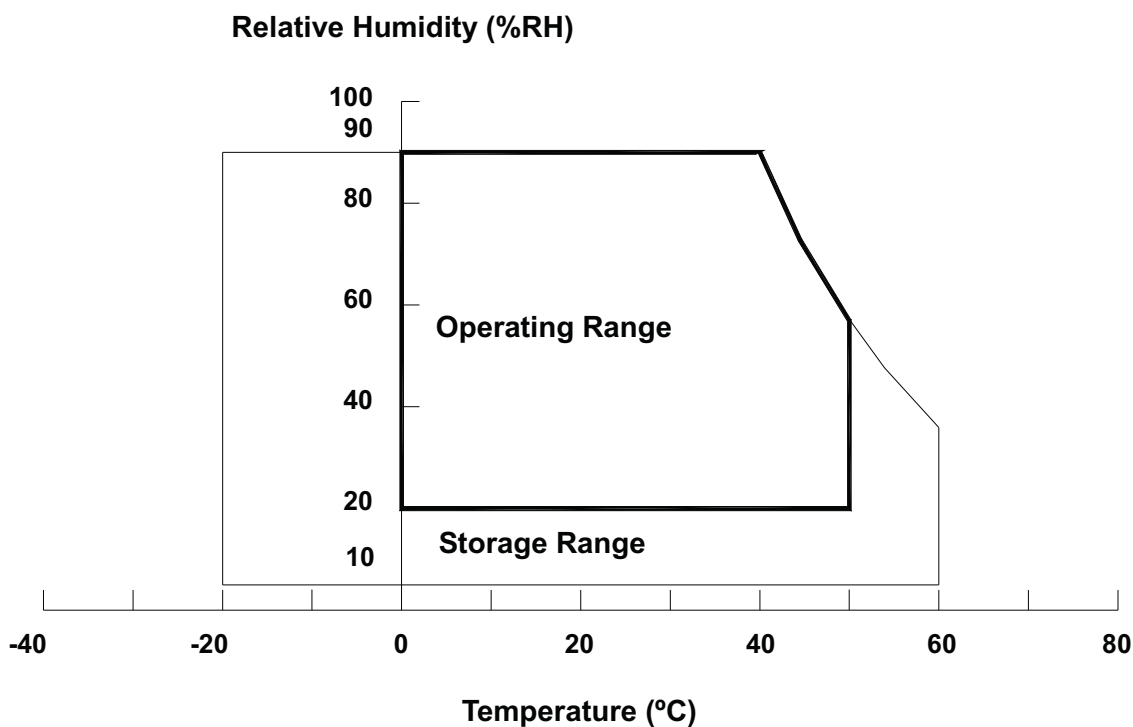
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for  $\pm X$ ,  $\pm Y$ ,  $\pm Z$ .

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.





## 2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

- (a) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 °C at normal humidity without condensation.
- (b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

## 2.3 ELECTRICAL ABSOLUTE RATINGS

### 2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	Vcc	-0.3	13.5	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

### 2.3.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V <sub>W</sub>	—	3000	V <sub>RMS</sub>	

Note (1) No moisture condensation or freezing.

### 3. ELECTRICAL CHARACTERISTICS

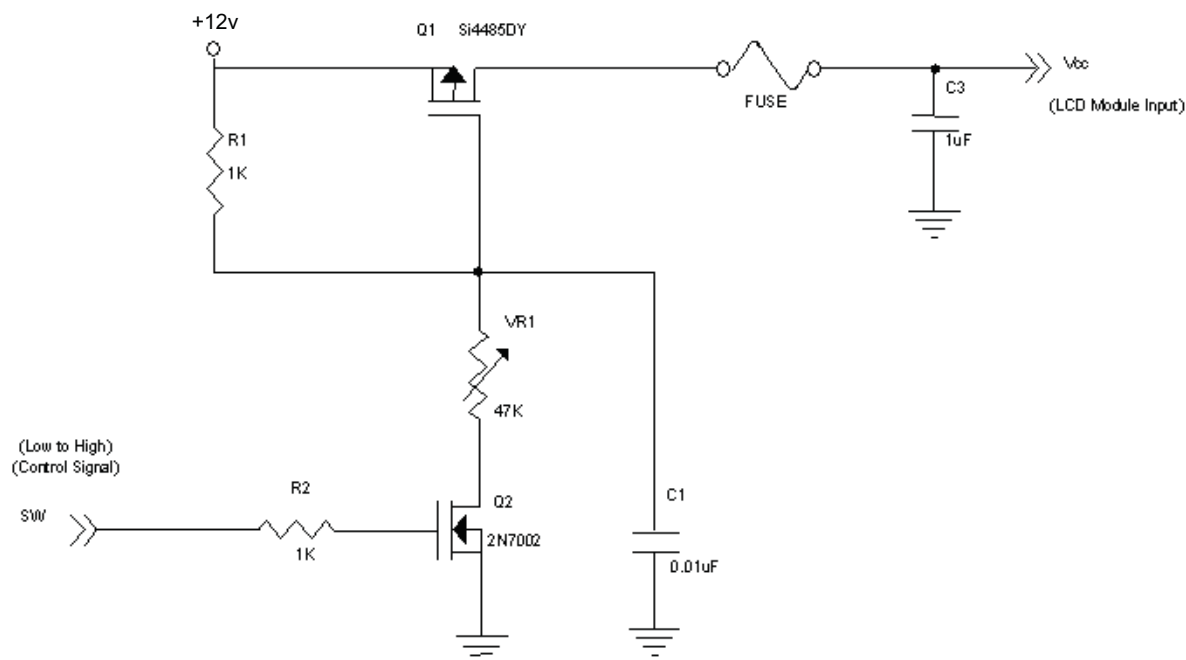
#### 3.1 TFT LCD MODULE

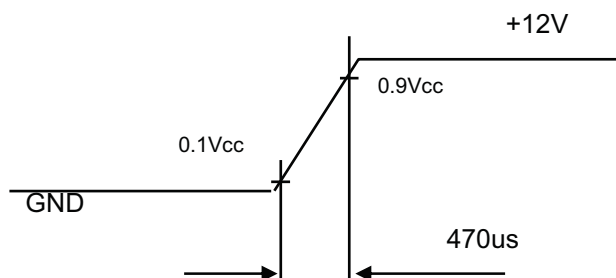
Ta = 25 ± 2 °C

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V <sub>CC</sub>	10.8	12	13.2	Vrms	(1)
Rush Current		I <sub>RUSH</sub>	-	-	4.48	A	(2)
Power Supply Current	White Pattern	I <sub>CC</sub>	-	0.97	-	A	(3)
	Black Pattern		-	0.44	-	A	
	Horizontal Stripe		-	1.11	-	A	
LVDS Interface	Differential Input High Threshold Voltage	V <sub>LVTH</sub>	+100	-	-	mV	(4)
	Differential Input Low Threshold Voltage	V <sub>LVTL</sub>	-	-	-100	mV	
	Common Input Voltage	V <sub>CM</sub>	1.0	1.2	1.4	V	
	Differential input voltage	V <sub>ID</sub>	200	—	600	ohm	
	Terminating Resistor	R <sub>T</sub>	-	100	-		
CMOS interface	Input High Threshold Voltage	V <sub>IH</sub>	2.7	-	3.3	V	
	Input Low Threshold Voltage	V <sub>IL</sub>	0	-	0.7	V	

Note (1) The module should be always operated within above ranges.

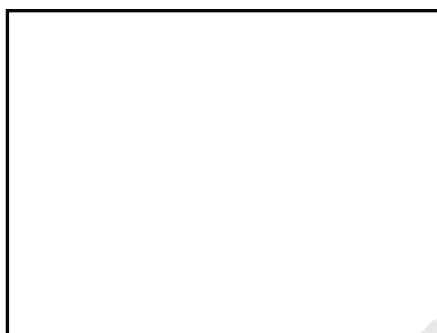
Note (2) Measurement Conditions:



**Vcc rising time is 470us**

Note (3) The specified power supply current is under the conditions at  $V_{cc} = 12\text{ V}$ ,  $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$ ,  $f_v = 120\text{ Hz}$ , whereas a power dissipation check pattern below is displayed.

a. White Pattern



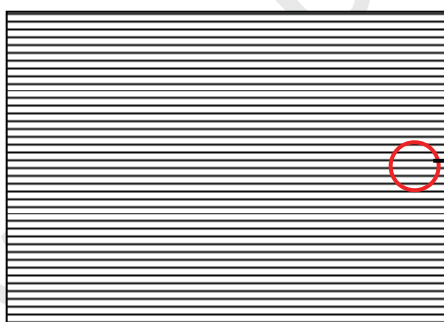
Active Area

b. Black Pattern

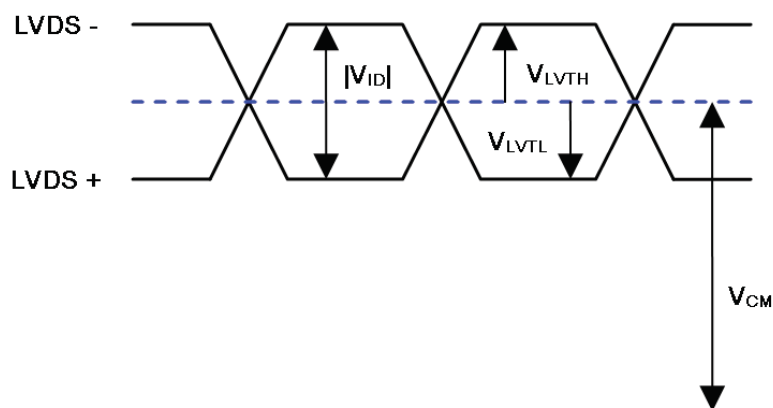


Active Area

c. Horizontal Pattern



Note (4) The LVDS input characteristics are as follows:



### 3.2 BACKLIGHT UNIT

#### 3.2.1 CCFL (Cold Cathode Fluorescent Lamp) CHARACTERISTICS ( $T_a = 25 \pm 2^\circ\text{C}$ )

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Voltage	$V_W$	-	910	-	$V_{RMS}$	$I_h = 14.5\text{mA}$
Lamp Current	$I_L$	14.0	14.5	15.0	$\text{mA}_{RMS}$	(1)
Lamp Starting Voltage	$V_S$	-	-	1500	$V_{RMS}$	(2), $T_a = 0^\circ\text{C}$
		-	-	1300	$V_{RMS}$	(2), $T_a = 25^\circ\text{C}$
Operating Frequency	$F_O$	30	-	80	KHz	(3)
Lamp Life Time	$L_{BL}$	50,000	-	-	Hrs	(4), at 14.5mA

Note (1) Lamp current is measured by utilizing AC current probe and its value is average by measuring master and slave board.:

Note (2) The lamp starting voltage  $V_S$  should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency of the display input signals, and it may result in line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) The life time of a lamp is defined as when the brightness is larger than 50% of its original value and the effective discharge length is longer than 80% of its original length (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at the center point of lamp.) as the time in which it continues to operate under the condition at  $T_a = 25 \pm 2^\circ\text{C}$  and  $I_L = 14.0 \sim 15.0 \text{ mA}_{RMS}$ .

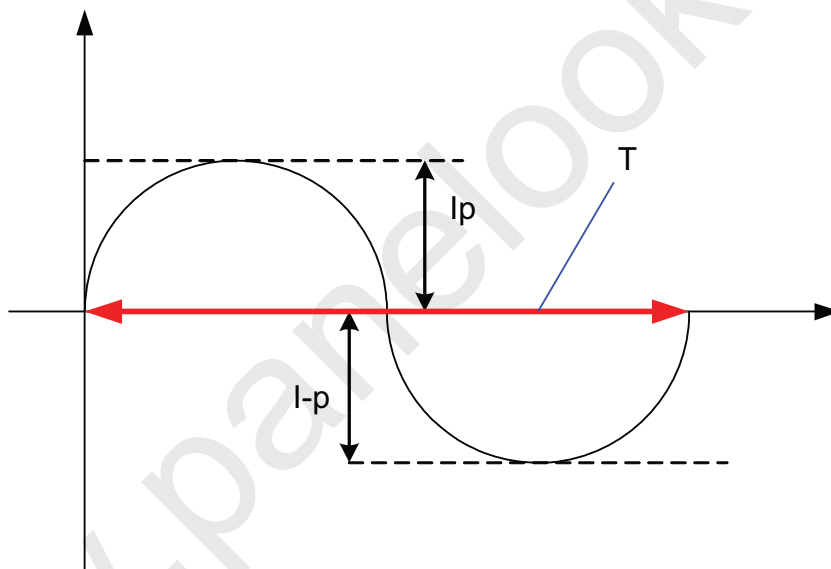
**3.2.2 BALANCE BOARD CHARACTERISTICS** ( $T_a = 25 \pm 2 \text{ }^{\circ}\text{C}$ )

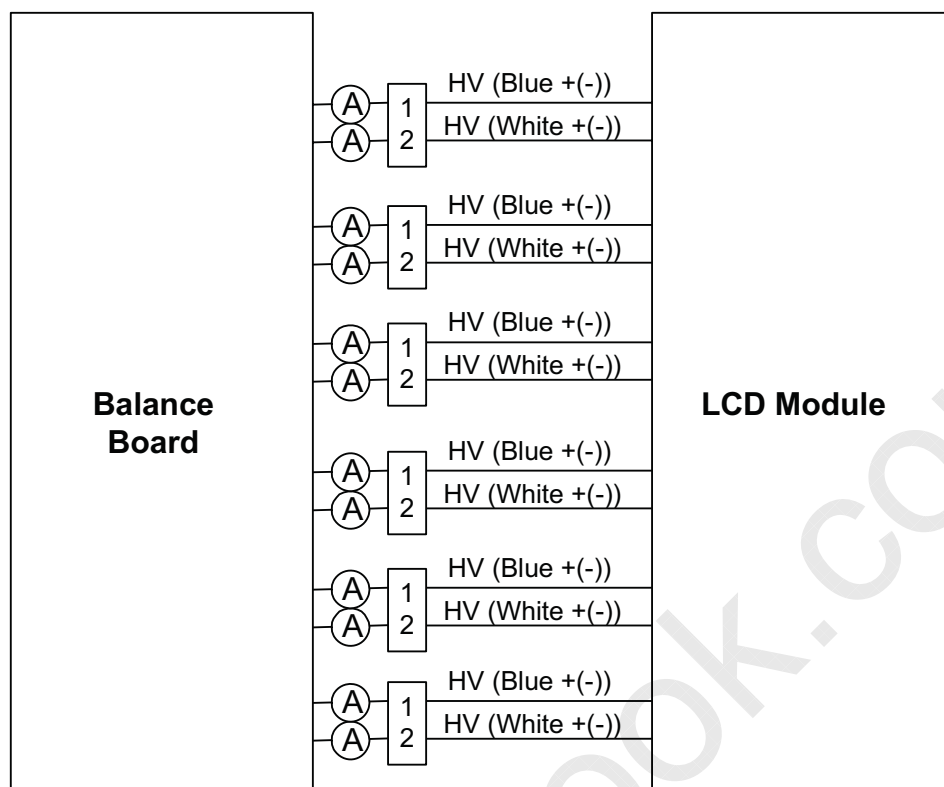
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Input High Voltage		$V_{(HV1/HV)}$	-	910	-	Vrms	(2)
Input Current		$I_{BL(HV)}$		174		mA <sub>rms</sub>	No Dimming
Oscillating Frequency		$F_W$	45	47	49	kHz	
Individual Lamp Current		$I_L$	14.0	14.5	15.0	mA	H.V
Lamp Detection	High (LD)	LD	5			V	Normal Operation
	Low (LD)	LD			1.5	V	Lamp Connector Open
Dimming frequency		$F_B$	135	150	165	Hz	
Minimum Duty Ratio		$D_{MIN}$	-	15	-	%	

Note (1) Lamp current is measured by utilizing high frequency current meters as shown below:

Note (2) Input High Voltage Hv based on spec. +-7% tolerance.

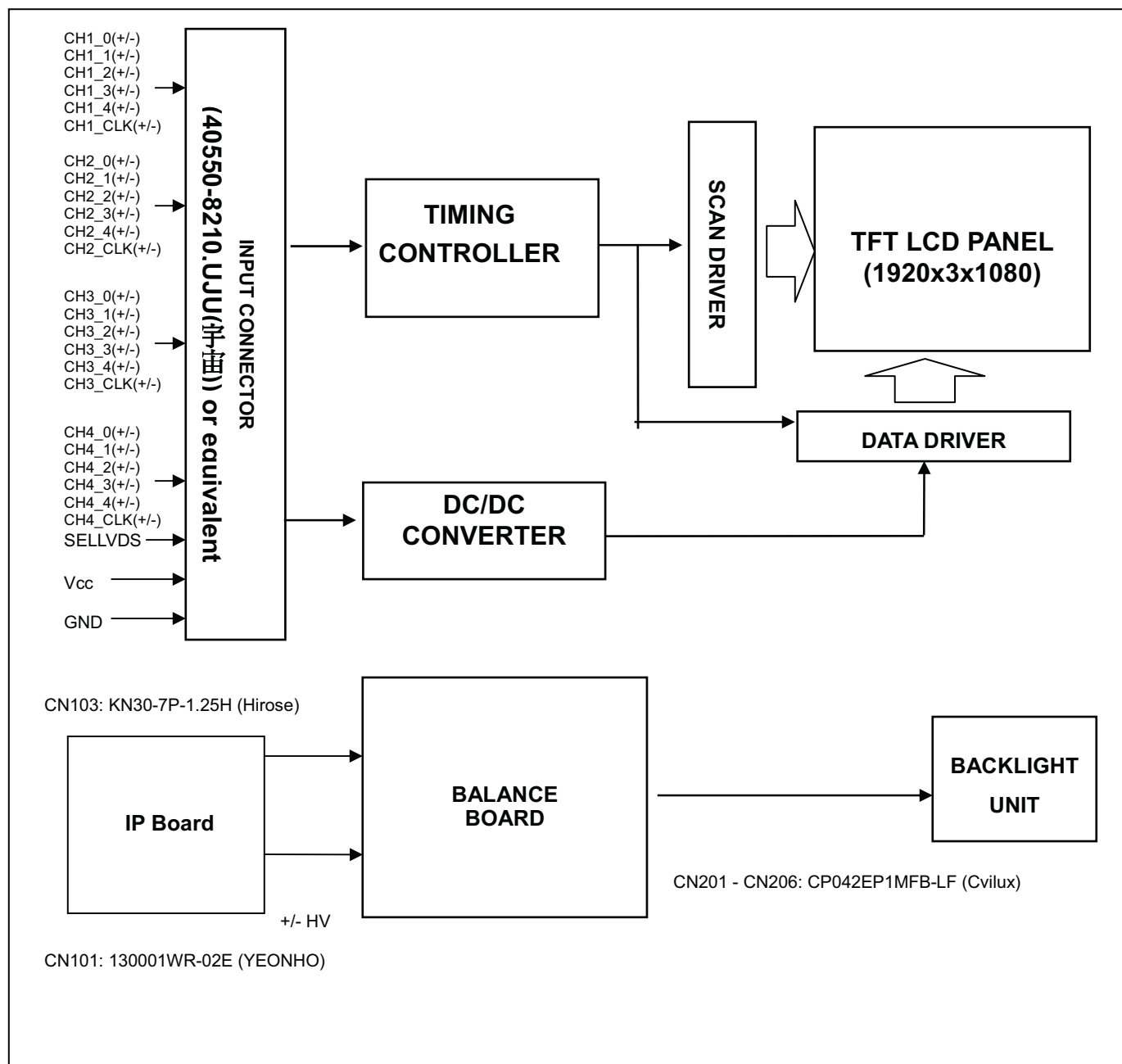
Note (3) Asymmetric ratio must be from 90% to 110% ( $0.9 < I_p / I_{rms@T/2X\sqrt{2}} < 1.1$ )





## 4. BLOCK DIAGRAM

### 4.1 TFT LCD MODULE





## 5. INTERFACE PIN CONNECTION

### 5.1 TFT LCD MODULE

**CNF1 Connector Pin Assignment** (40550-8210,UJU(宇宙) or equivalent)

Pin	Name	Description	Note
1	VCC	+12V power supply	
2	VCC	+12V power supply	
3	VCC	+12V power supply	
4	VCC	+12V power supply	
5	VCC	+12V power supply	
6	N.C.	No Connection	(1)
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	CH1[0]-	First pixel Negative LVDS differential data input. Pair 0	
11	CH1[0]+	First pixel Positive LVDS differential data input. Pair 0	
12	CH1[1]-	First pixel Negative LVDS differential data input. Pair 1	
13	CH1[1]+	First pixel Positive LVDS differential data input. Pair 1	
14	CH1[2]-	First pixel Negative LVDS differential data input. Pair 2	
15	CH1[2]+	First pixel Positive LVDS differential data input. Pair 2	
16	GND	Ground	
17	CH1CLK-	First pixel Negative LVDS differential clock input.	
18	CH1CLK+	First pixel Positive LVDS differential clock input.	
19	GND	Ground	
20	CH1[3]-	First pixel Negative LVDS differential data input. Pair 3	
21	CH1[3]+	First pixel Positive LVDS differential data input. Pair 3	
22	CH1[4]-	First pixel Negative LVDS differential data input. Pair 4	
23	CH1[4]+	First pixel Positive LVDS differential data input. Pair 4	
24	GND	Ground	
25	CH3[0]-	Third pixel Negative LVDS differential data input. Pair 0	
26	CH3[0]+	Third pixel Positive LVDS differential data input. Pair 0	
27	CH3[1]-	Third pixel Negative LVDS differential data input. Pair 1	
28	CH3[1]+	Third pixel Positive LVDS differential data input. Pair 1	
29	CH3[2]-	Third pixel Negative LVDS differential data input. Pair 2	
30	CH3[2]+	Third pixel Positive LVDS differential data input. Pair 2	
31	GND	Ground	
32	CH3CLK-	Third pixel Negative LVDS differential clock input.	
33	CH3CLK+	Third pixel Positive LVDS differential clock input.	



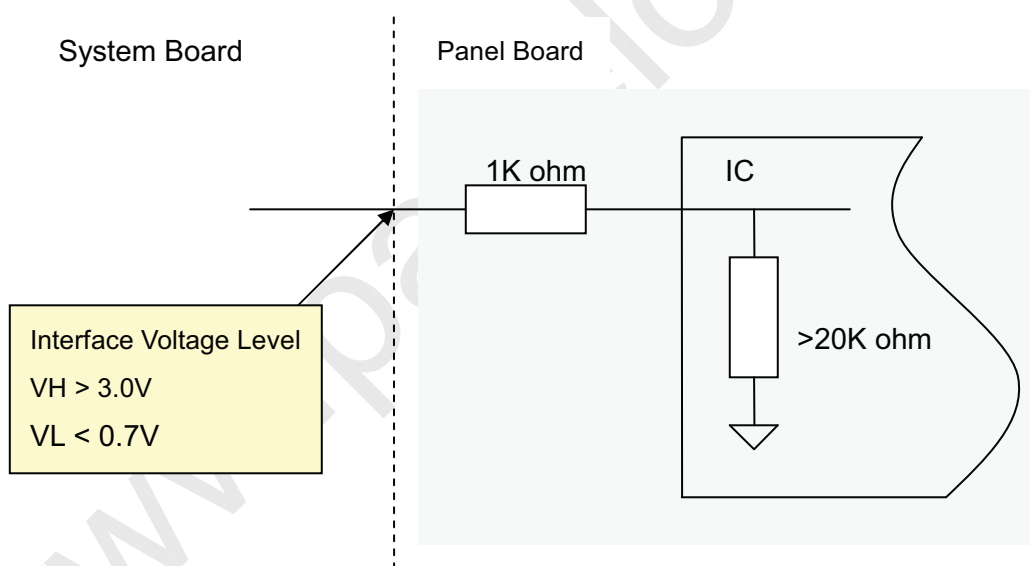
34	GND	Ground	
35	CH3[3]-	Third pixel Negative LVDS differential data input. Pair 3	
36	CH3[3]+	Third pixel Positive LVDS differential data input. Pair 3	
37	CH3[4]-	Third pixel Negative LVDS differential data input. Pair 4	
38	CH3[4]+	Third pixel Positive LVDS differential data input. Pair 4	
39	GND	Ground	
40	SCL	I2C Bus	
41	N.C.	No Connection	(1)
42	N.C.	No Connection	(1)
43	WP	Write Protection for EEPROM	
44	SDA	I2C Bus	
45	LVDS_SEL	LVDS Data Format Selection	(2)
46	N.C.	No Connection	(1)
47	N.C.	No Connection	(1)
48	N.C.	No Connection	(1)
49	N.C.	No Connection	(1)
50	N.C.	No Connection	(1)
51	N.C.	No Connection	(1)
52	GND	Ground	
53	CH4[4]+	Fourth pixel Positive LVDS differential data input. Pair 4	
54	CH4[4]-	Fourth pixel Negative LVDS differential data input. Pair 4	
55	CH4[3]+	Fourth pixel Positive LVDS differential data input. Pair 3	
56	CH4[3]-	Fourth pixel Negative LVDS differential data input. Pair 3	
57	GND	Ground	
58	CH4CLK+	Fourth pixel Positive LVDS differential clock input.	
59	CH4CLK-	Fourth pixel Negative LVDS differential clock input.	
60	GND	Ground	
61	CH4[2]+	Fourth pixel Positive LVDS differential data input. Pair 2	
62	CH4[2]-	Fourth pixel Negative LVDS differential data input. Pair 2	
63	CH4[1]+	Fourth pixel Positive LVDS differential data input. Pair 1	
64	CH4[1]-	Fourth pixel Negative LVDS differential data input. Pair 1	
65	CH4[0]+	Fourth pixel Positive LVDS differential data input. Pair 0	
66	CH4[0]-	Fourth pixel Negative LVDS differential data input. Pair 0	
67	GND	Ground	
68	CH2[4]+	Second pixel Positive LVDS differential data input. Pair 4	
69	CH2[4]-	Second pixel Negative LVDS differential data input. Pair 4	
70	CH2[3]+	Second pixel Positive LVDS differential data input. Pair 3	

71	CH2[3]-	Second pixel Negative LVDS differential data input. Pair 3	
72	GND	Ground	
73	CH2CLK+	Second pixel Positive LVDS differential clock input.	
74	CH2CLK-	Second pixel Negative LVDS differential clock input.	
75	GND	Ground	
76	CH2[2]+	Second pixel Positive LVDS differential data input. Pair 2	
77	CH2[2]-	Second pixel Negative LVDS differential data input. Pair 2	
78	CH2[1]+	Second pixel Positive LVDS differential data input. Pair 1	
79	CH2[1]-	Second pixel Negative LVDS differential data input. Pair 1	
80	CH2[0]+	Second pixel Positive LVDS differential data input. Pair 0	
81	CH2[0]-	Second pixel Negative LVDS differential data input. Pair 0	
82	GND	Ground	

Note (1) Reserved for internal use. Please leave it open.

Note (2) High=connect to +3.3V or Open: VESA Format; Low= connect to GND: JEIDA Format.

Note (3) Interface optional pin has internal scheme as following diagram. Customer should keep the interface voltage level requirement as below.



Note (4) LVDS 4-port Data Mapping

Port	Channel of LVDS	Data Stream
1st Port	First Pixel	1, 5, 9, .....1913, 1917
2nd Port	Second Pixel	2, 6, 10, ....1914, 1918
3rd Port	Third Pixel	3, 7, 11, ....1915, 1919
4th Port	Fourth Pixel	4, 8, 12, ....1916, 1920

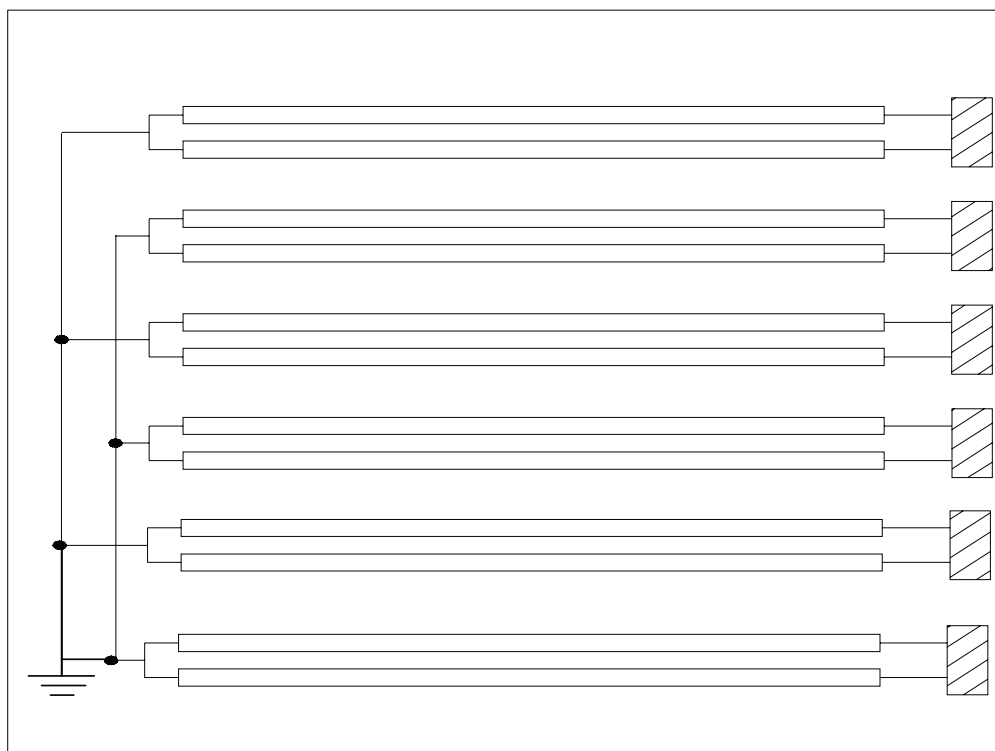
## 5.2 BACKLIGHT UNIT

The pin configuration for the housing and leader wire is shown in the table below.

CN201-CN210 (Housing): BDAMR-02VAS-3 (JST)

Pin No.	Symbol	Description	Wire Color
1	HV	High Voltage	Blue
2	HV	High Voltage	White

Note (1) The backlight interface housing for high voltage side is a model CP042ESFA00 (Cvilux), manufactured by Cvilux. The mating header on inverter part number is CP042EP1MFB-LF (Cvilux).



**5.3 BALANCE BOARD UNIT**

CN127 (Header): 130001WR-02E (YEONHO)

Pin No.	Symbol	Description
1	HV+(-)	High Voltage Input
2	HV+(-)	High Voltage Input

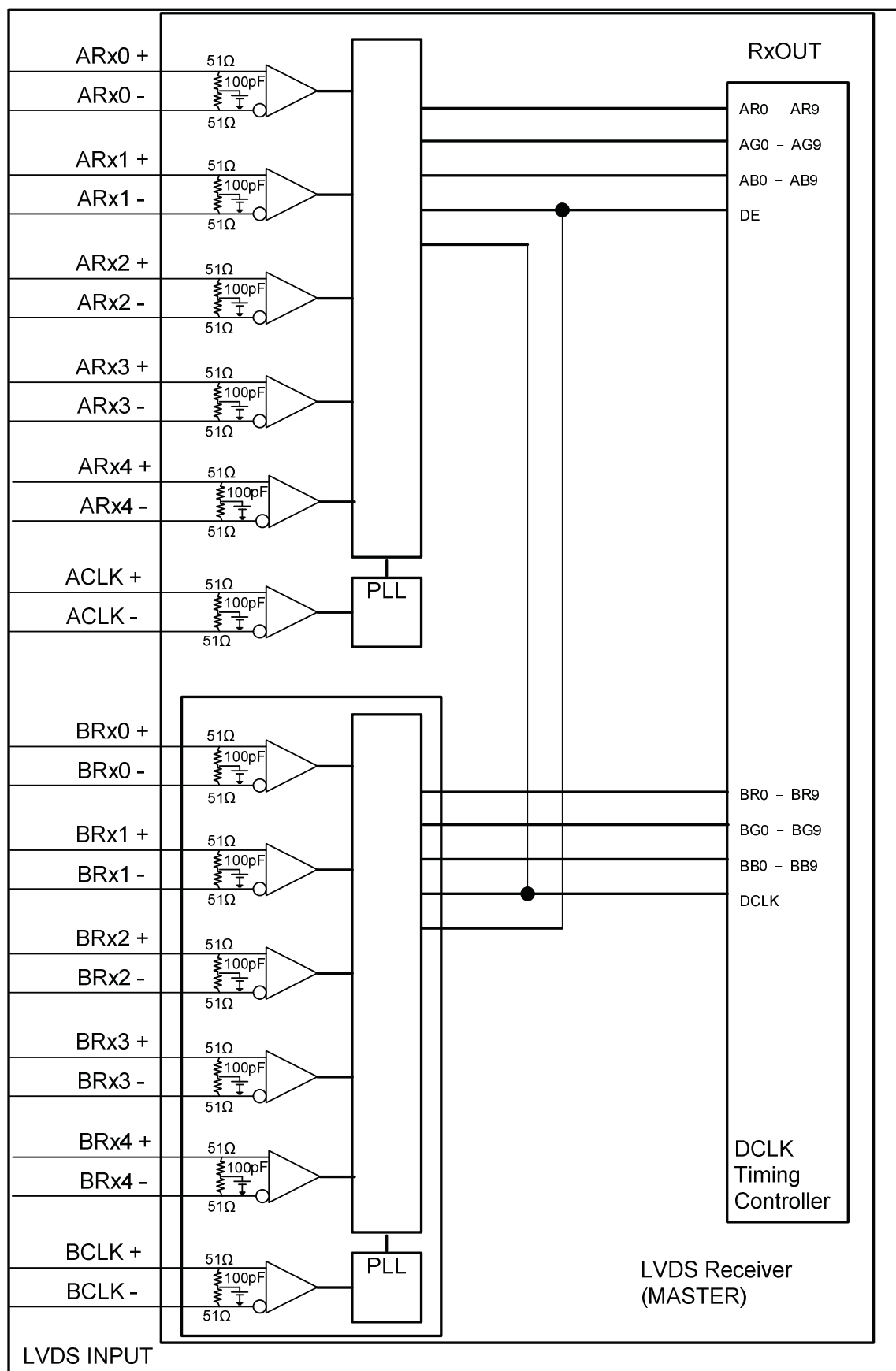
CN101-CN106 (Header): CP042EP1MFB-LF (Cvilux)

Pin No.	Symbol	Description
1	HV	CCFL High Voltage
2	HV	CCFL High Voltage

CN125 (Header): KN30-7P-1.25H (Hirose)

Pin No.	Symbol	Description
1	VCC	Power Supply for Protection Circuit
2	FB	Lamp Current Detected Voltage
3	FB	Lamp Current Detected Voltage
4	GND	Signal Ground
5	GND	Signal Ground
6	LD	CCFL Connector Open & Non-lighting signal
7	LD	CCFL Connector Open & Non-lighting signal

## 5.4 BLOCK DIAGRAM OF INTERFACE



AR0~AR9: First pixel R data

AG0~AG9: First pixel G data

AB0~AB9: First pixel B data

BR0~BR9: Second pixel R data

BG0~BG9: Second pixel G data

BB0~BB9: Second pixel B data

DE: Data enable signal

DCLK: Data clock signal

The third and fourth pixel are followed the same rules.

CR0~CR9: Third pixel R data

CG0~CG9: Third pixel G data

CB0~CB9: Third pixel B data

DR0~DR9: Fourth pixel R data

DG0~DG9: Fourth pixel G data

DB0~DB9: Fourth pixel B data

Note (1) A ~ D channel are first, second, third and fourth pixel respectively.

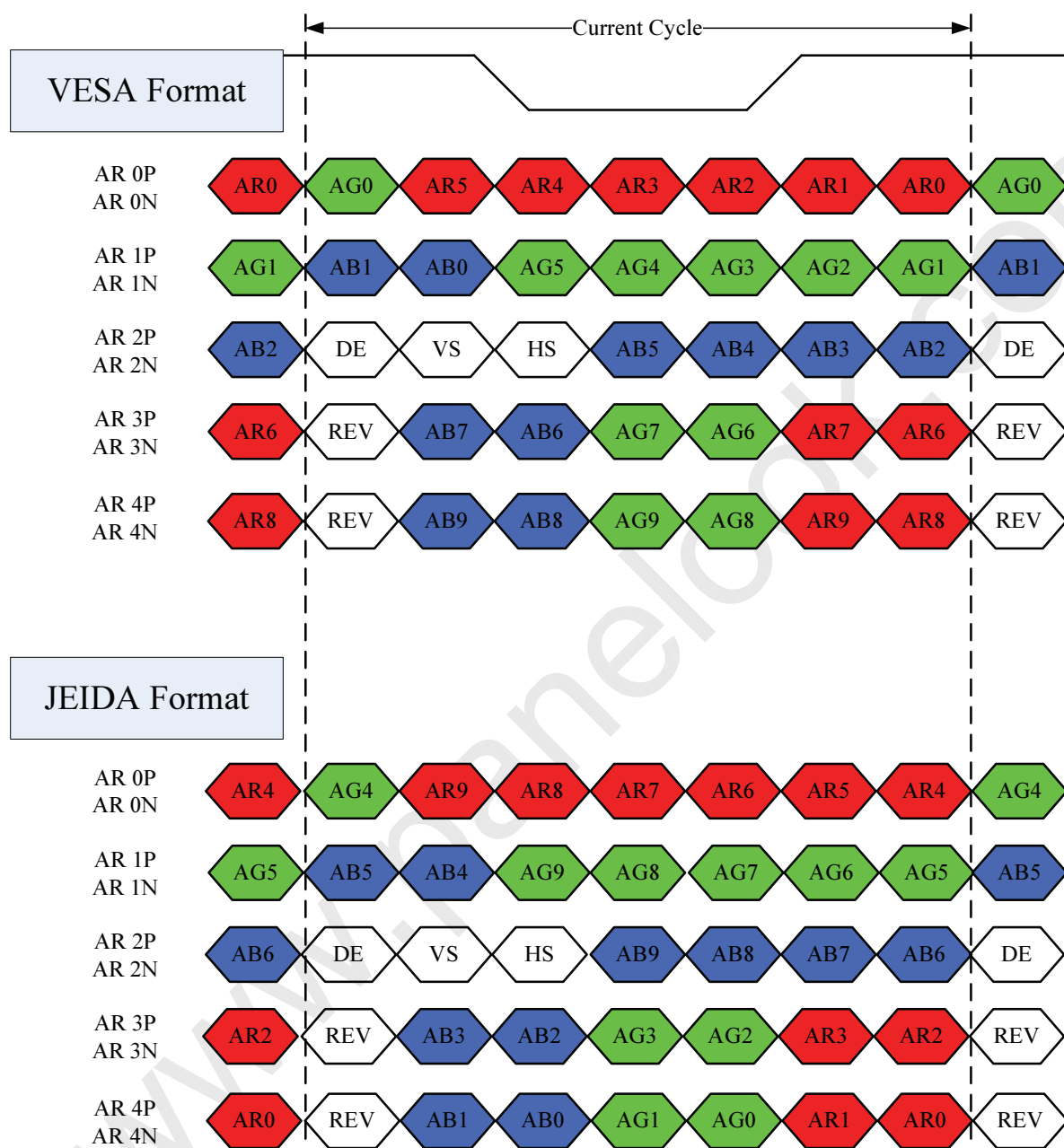
Note (2) The system must have the transmitter to drive the module.

Note (3) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

## 5.5 LVDS INTERFACE

VESA Format : SELLVDS = H or Open

JEIDA Format : SELLVDS = L



AR0~AR9: First Pixel R Data (9; MSB, 0; LSB)

AG0~AG9: First Pixel G Data (9; MSB, 0; LSB)

AB0~AB9: First Pixel B Data (9; MSB, 0; LSB)

DE: Data enable signal

DCLK: Data clock signal

RSV: Reserved



## 5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																												
		Red										Green										Blue								
R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Green	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	
	Cyan	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	Magenta	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red (1)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red (2)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	Green (1021)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0
	Green (1022)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	
	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	

Note (1) 0: Low Level Voltage, 1: High Level Voltage

## 6. INTERFACE TIMING

### 6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	$F_{\text{clkin}}$ (=1/TC)	60	74.25	80	MHz	
	Input cycle to cycle jitter	$T_{\text{rcl}}$	-	-	200	ps	(3)
	Spread spectrum modulation range	$F_{\text{clkin\_mod}}$	$F_{\text{clkin}}-2\%$	-	$F_{\text{clkin}}+2\%$	MHz	(4)
	Spread spectrum modulation frequency	$F_{\text{SSM}}$	-	-	200	KHz	
LVDS Receiver Data	Setup Time	$T_{\text{lvsu}}$	600	-	-	ps	(5)
	Hold Time	$T_{\text{lvhd}}$	600	-	-	ps	
Vertical Active Display Term	Frame Rate	$F_{\text{r5}}$	97	100	103	Hz	(6)
		$F_{\text{r6}}$	117	120	123	Hz	
	Total	$T_{\text{v}}$	1115	1125	1135	Th	$T_{\text{v}}=T_{\text{vd}}+T_{\text{vb}}$
	Display	$T_{\text{vd}}$	1080	1080	1080	Th	—
	Blank	$T_{\text{vb}}$	35	45	55	Th	—
Horizontal Active Display Term	Total	$T_{\text{h}}$	540	550	575	$T_{\text{c}}$	$T_{\text{h}}=T_{\text{hd}}+T_{\text{hb}}$
	Display	$T_{\text{hd}}$	480	480	480	$T_{\text{c}}$	—
	Blank	$T_{\text{hb}}$	60	70	95	$T_{\text{c}}$	—

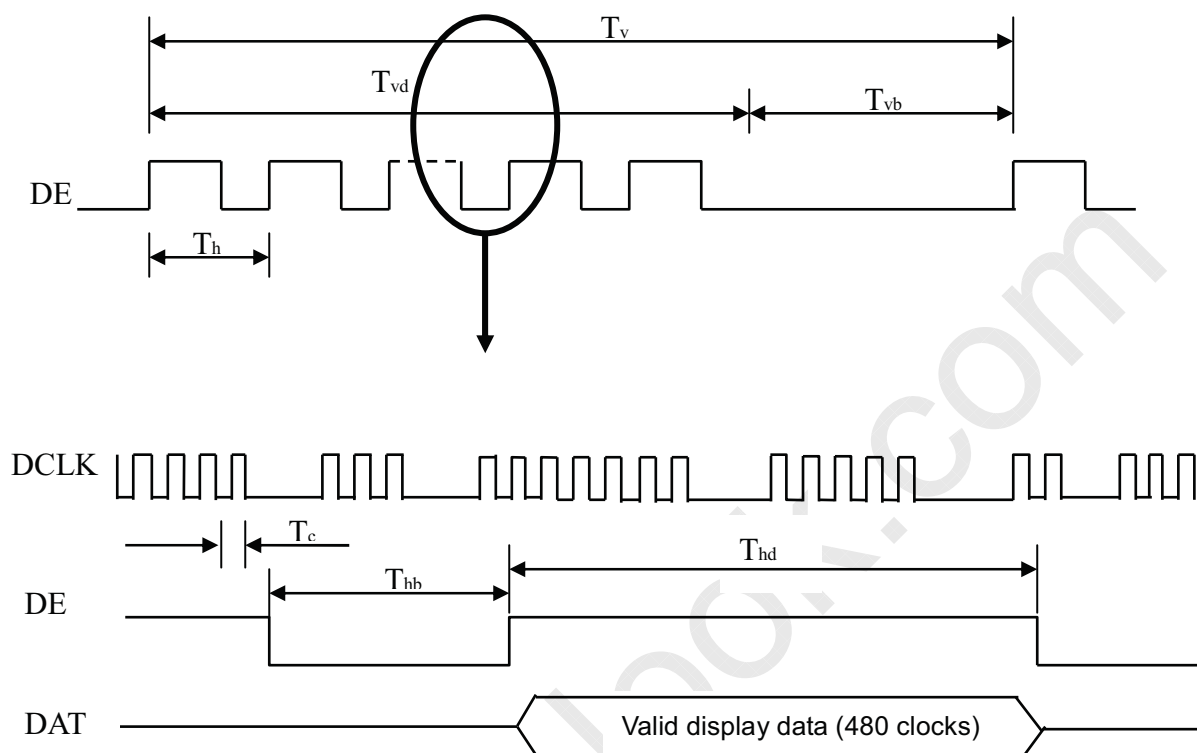
Note (1) Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

Note (2) Please make sure the range of pixel clock has follow the below equation:

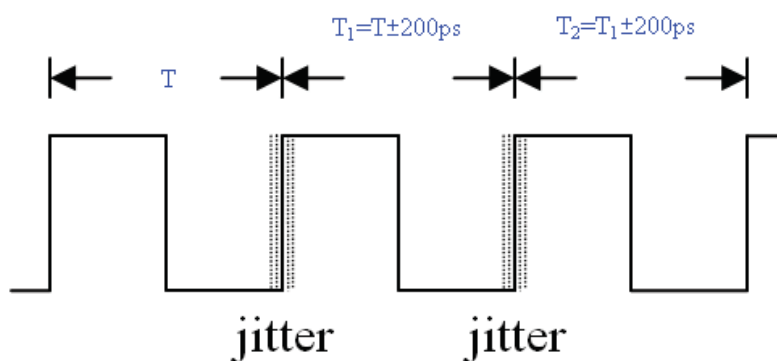
$$F_{\text{clkin}}(\text{max}) \geq F_{\text{r6}} \times T_{\text{v}} \times T_{\text{h}}$$

$$F_{\text{r5}} \times T_{\text{v}} \times T_{\text{h}} \geq F_{\text{clkin}}(\text{min})$$

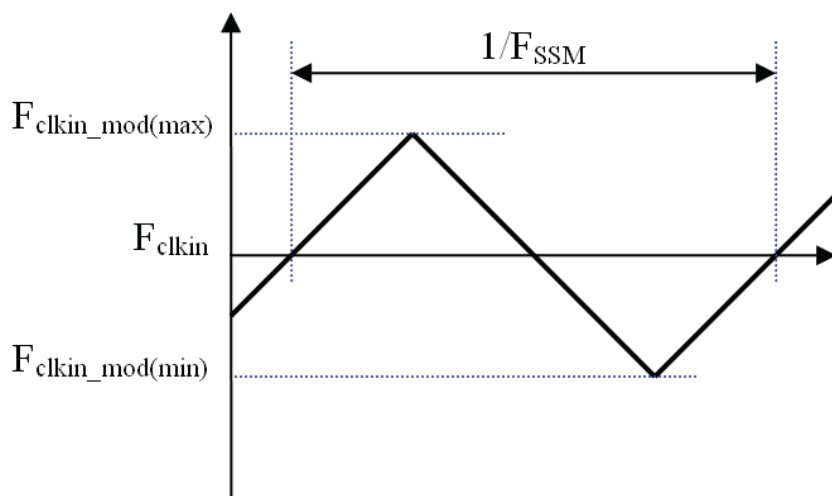
## INPUT SIGNAL TIMING DIAGRAM



Note (3) The input clock cycle-to-cycle jitter is defined as below figures.  $Trcl = |T_1 - T_1|$

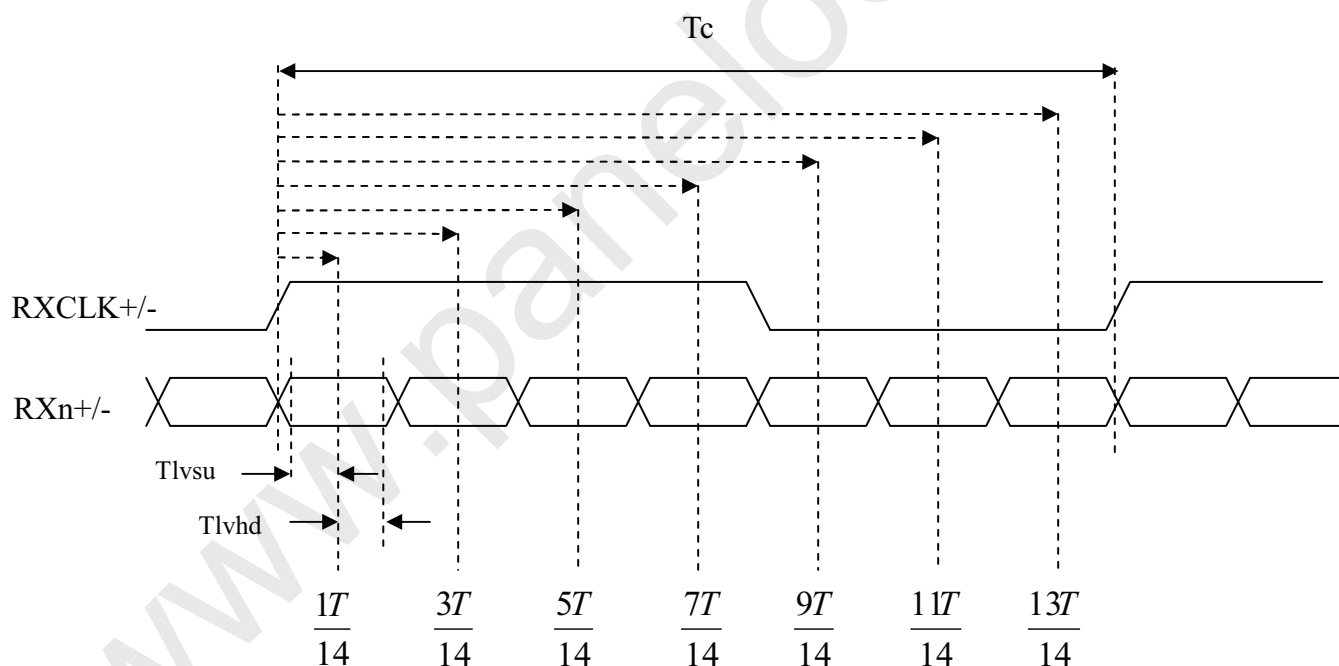


Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

## LVDS RECEIVER INTERFACE TIMING DIAGRAM

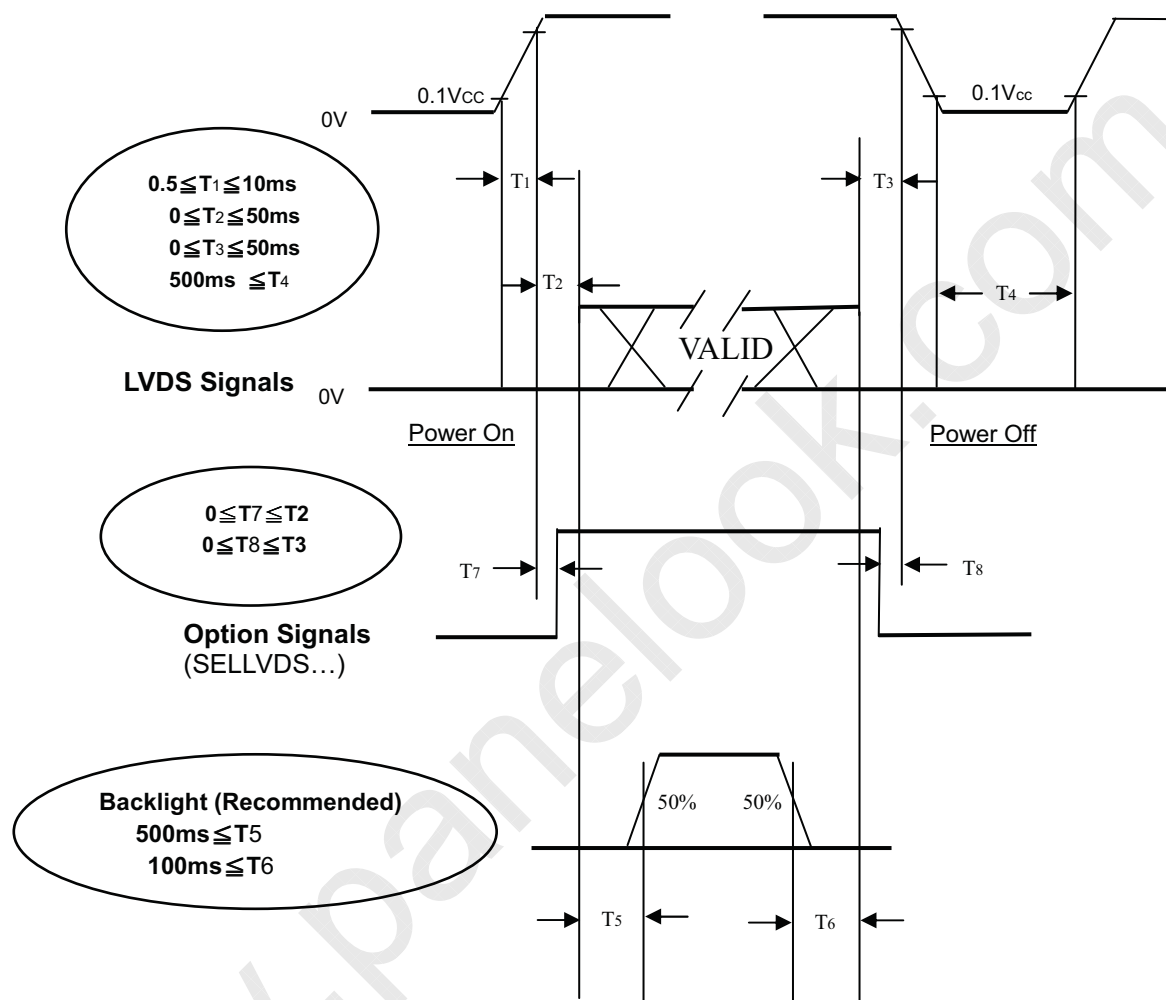


Note (6) (ODSEL) = H/L or open for 100/120Hz frame rate. Please refer to 5.1 for detail information

## 6.2 POWER ON/OFF SEQUENCE

( $T_a = 25 \pm 2^\circ\text{C}$ )

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



**Power ON/OFF Sequence**

Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance. If  $T2 < 0$ , that maybe cause electrical overstress failure.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

## 7. OPTICAL CHARACTERISTICS

### 7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V <sub>CC</sub>	12	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current(HV)	I <sub>L</sub>	14.5 ± 0.5	mA
Oscillating Frequency (Balance Board)	F <sub>w</sub>	47±2	KHz
Frame rate		120	Hz

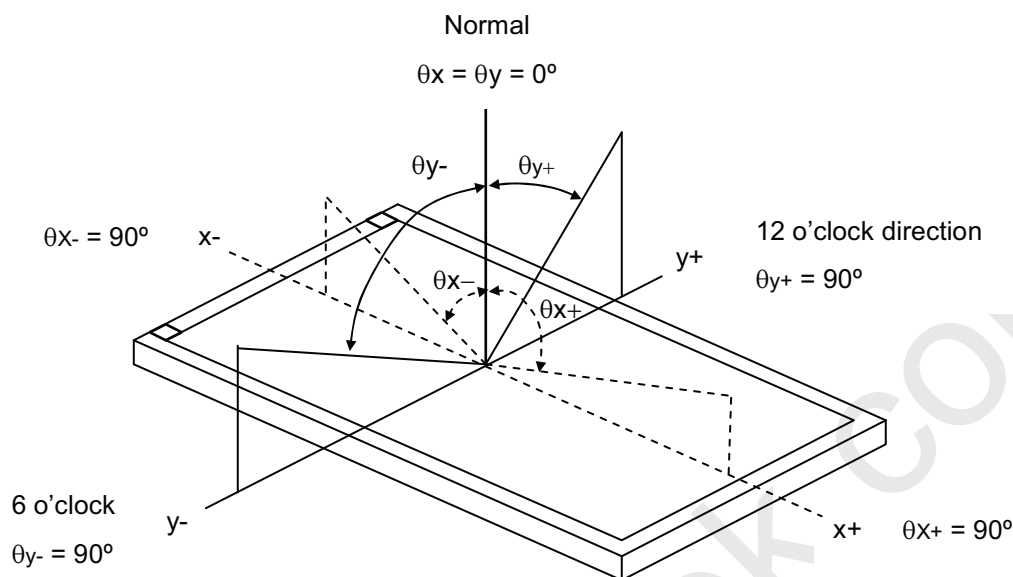
### 7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	$\theta_x=0^\circ, \theta_y=0^\circ$ Viewing angle at Normal direction	4600	6500	-	-	(2)
Response Time		Gray to gray average		-	4.5	9	ms	(3)
Center Luminance of White		L <sub>C</sub>		400	500	-	cd/	(4)
White Variation		$\delta W$		-	-	1.3	-	(7)
Cross Talk		CT		-	-	4.0	%	(5)
Color Chromaticity	Red	R <sub>x</sub>		Typ. - 0.03	0.630	Typ. + 0.03	-	(6)
		R <sub>y</sub>			0.323		-	
	Green	G <sub>x</sub>			0.290		-	
		G <sub>y</sub>			0.597		-	
	Blue	B <sub>x</sub>			0.148		-	
		B <sub>y</sub>			0.049		-	
	White	W <sub>x</sub>			0.280		-	
		W <sub>y</sub>			0.290		-	
	Color Gamut	CG		-	72	-	%	NTSC
Viewing Angle	Horizontal	$\theta_{x+}$	CR≥20	80	88	-	Deg ·	(1)
		$\theta_{x-}$		80	88	-		
	Vertical	$\theta_{y+}$		80	88	-		
		$\theta_{y-}$		80	88	-		
				80	88	-		

Note (1) Definition of Viewing Angle ( $\theta_x$ ,  $\theta_y$ ):

Viewing angles are measured by Autronic Conoscope Cono-80



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

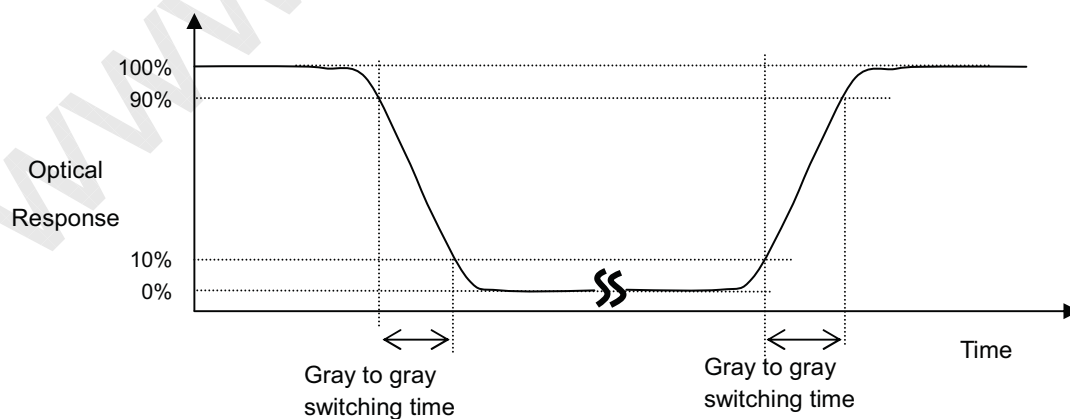
$$\text{Contrast Ratio (CR)} = L_{255} / L_0$$

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (7).

Note (3) Definition of Gray to Gray Switching Time :



The driving signal means the signal of gray level 0, 63, 127, 191, 255.

Gray to gray average time means the average switching time of gray level 0, 63, 127, 191, 255 to each other.

Note (4) Definition of Luminance of White ( $L_C$ ,  $L_{AVE}$ ):

Measure the luminance of gray level 255 at center point and 5 points

$$L_C = L(5)$$

$$L_{AVE} = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$$

where  $L(x)$  is corresponding to the luminance of the point X at the figure in Note (7).

Note (5) Definition of Cross Talk (CT):

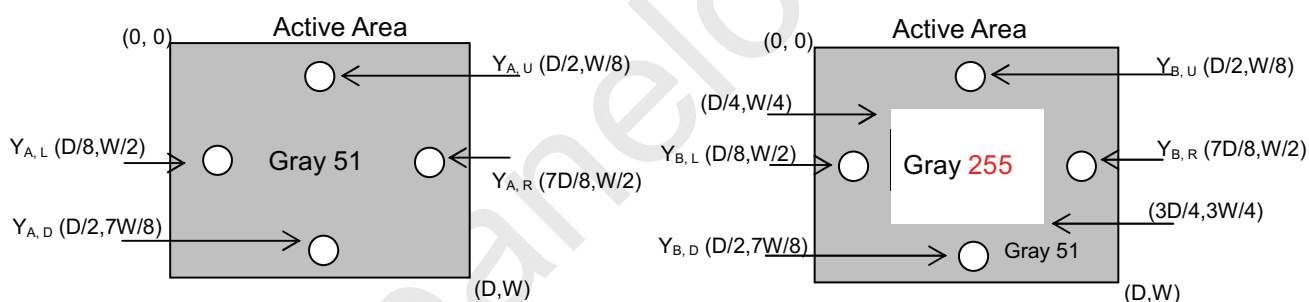
$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where:

(a)

$Y_A$  = Luminance of measured location without gray level 255 pattern ( $\text{cd/m}^2$ )

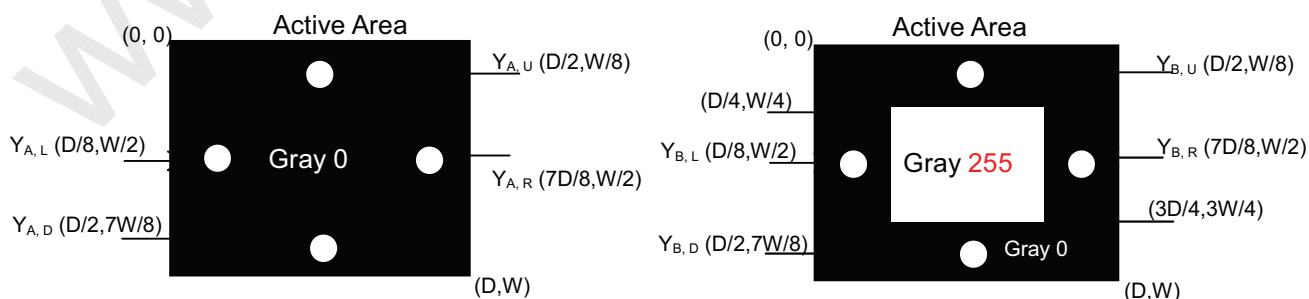
$Y_B$  = Luminance of measured location with gray level 255 pattern ( $\text{cd/m}^2$ )



(b)

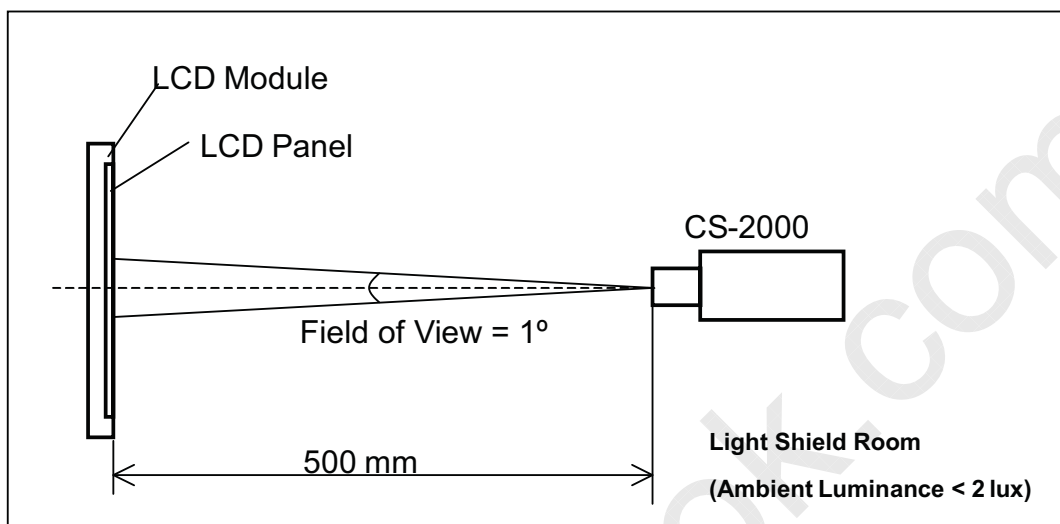
$Y_A$  = Luminance of measured location without gray level 255 pattern ( $\text{cd/m}^2$ )

$Y_B$  = Luminance of measured location with gray level 255 pattern ( $\text{cd/m}^2$ )



## Note (6) Measurement Setup:

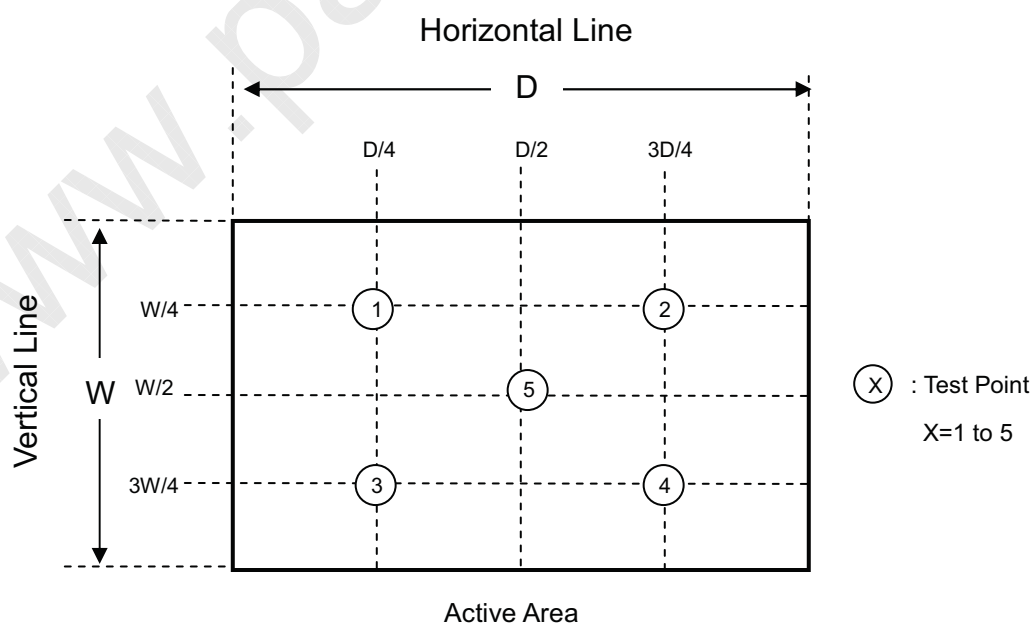
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 1 hour in a windless room.



## Note (7) Definition of White Variation ( $\delta W$ ):

Measure the luminance of gray level 255 at 5 points

$$\delta W = \text{Maximum} [L(1), L(2), L(3), L(4), L(5)] / \text{Minimum} [L(1), L(2), L(3), L(4), L(5)]$$



## 8. DEFINITION OF LABELS

### 8.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



- (a) Model Name: V400H1-LH9
- (b) Revision: Rev. XX, for example: A0, A1... B1, B2... or C1, C2...etc.
- (c) Production Locations / Factory ID: IN TAIWAN (GEMN) or IN CHINA (LEOO or CAPG or CANO)
- (d) CMO barcode definition:

Serial ID: XX-XX-X-XX-YMD-L-NNNN

Code	Meaning	Description
XX	CMO internal use	-
XX	Revision	Cover all the change
X-XX	CMO internal use	-
YMD	Year, month, day	Year: 2001=1, 2002=2, 2003=3, 2004=4... Month: Jan. ~ Dec.=1, 2, 3, ~, 9, A, B, C Day: 1 <sup>st</sup> to 31 <sup>st</sup> =1, 2, 3, ~, 9, A, B, C, ~, W, X, Y, exclude I, O, and U
L	Product line #	Line 1=1, Line 2=2, Line 3=3, ...
NNNN	Serial number	Manufacturing sequence of product

- (e) Customer's barcode definition:

Serial ID: CM-40H19-X-X-X-XX-L-XX-L-YMD-NNNN

Code	Meaning	Description
CM	Supplier code	CMO=CM
40H19	Model number	V400H1-LH9=40H19
X	Revision code	C1=A, C2=B, .....C9=I
X	Source driver IC code	Century=1, CLL=2, Demos=3, Epson=4, Fujitsu=5, Himax=6, Hitachi=7, Hynix=8, LDI=9, Matsushita=A, NEC=B, Novatec=C, OKI=D, Philips=E, Renasas=F, Samsung=G, Sanyo=H, Sharp=I, TI=J, Topro=K, Toshiba=L, Windbond=M
X	Gate driver IC code	
XX	Cell location	Tainan, Taiwan=TN
L	Cell line #	1~12=0~C
XX	Module location	Tainan, Taiwan=TN
L	Module line #	1~12=0~C
YMD	Year, month, day	Year: 2001=1, 2002=2, 2003=3, 2004=4... Month: Jan. ~ Dec.=1, 2, 3, ~, 9, A, B, C Day: 1 <sup>st</sup> to 31 <sup>st</sup> =1, 2, 3, ~, 9, A, B, C, ~, W, X, Y, exclude I, O, and U
NNNN	Serial number	By LCD supplier

## 9. PACKAGING

### 9.1 PACKING SPECIFICATIONS

- (1) 5 LCD TV modules / 1 Box
- (2) Box dimensions : 1060(L)x378(W)x650(H)mm
- (3) Weight : Approx. 51.88Kg(5 modules per carton)

### 9.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method

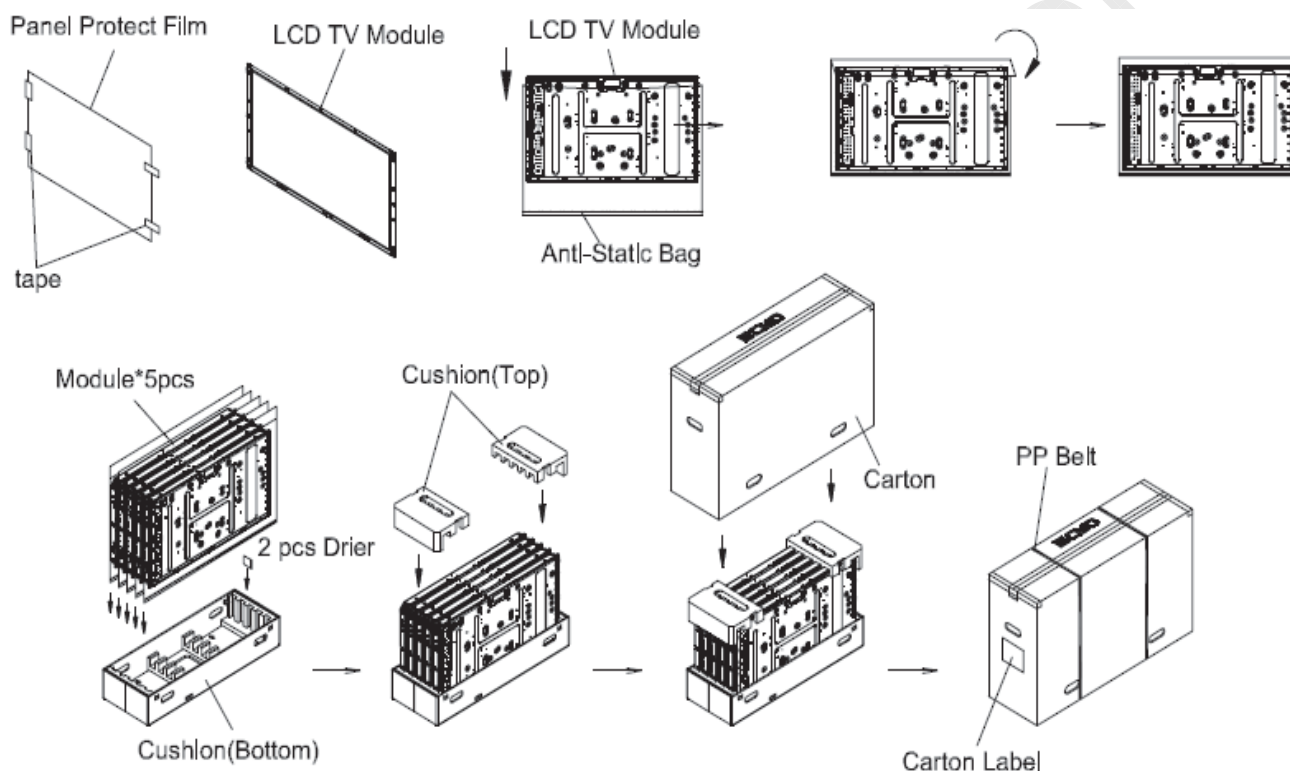
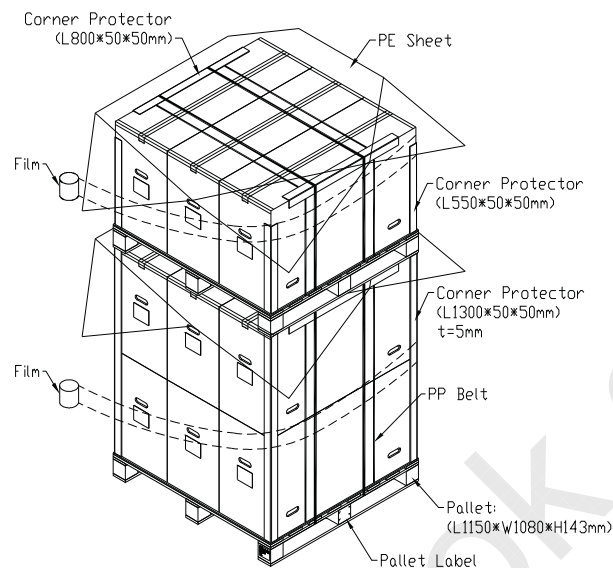
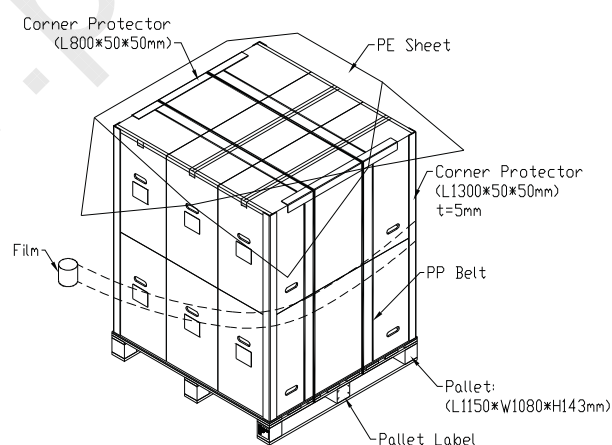


Figure.9-1 packing method

**Sea / Land Transportation  
(40ft Container)****Air Transportation****Figure. 9-2 Packing method**



## 10. PRECAUTIONS

### 10.1 ASSEMBLY AND HANDLING PRECAUTIONS

- (1) Do not apply rough force such as bending or twisting to the module during assembly.
- (2) It is recommended to assemble or to install a module into the user's system in clean working areas.  
The dust and oil may cause electrical short or worsen the polarizer.
- (3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and backlight.
- (4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.
- (5) Do not plug in or pull out the I/F connector while the module is in operation.
- (6) Do not disassemble the module.
- (7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- (8) Moisture can easily penetrate into LCD module and may cause the damage during operation.
- (9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.
- (10) When ambient temperature is lower than 10°C, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

### 10.2 SAFETY PRECAUTIONS

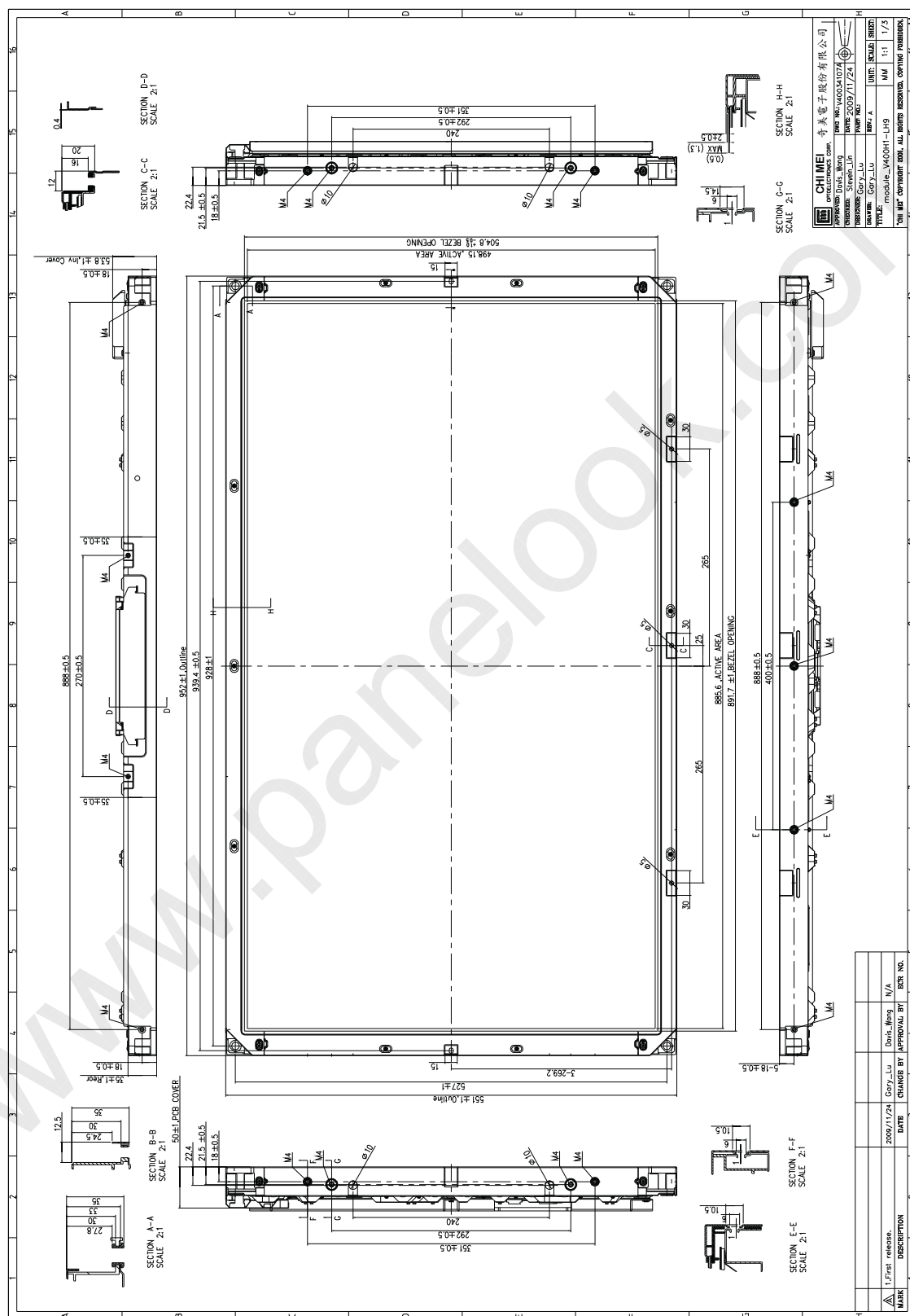
- (1) The startup voltage of a backlight is over 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the backlight unit.
- (2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- (3) After the module's end of life, it is not harmful in case of normal operation and storage.

### 10.3 SAFETY STANDARDS

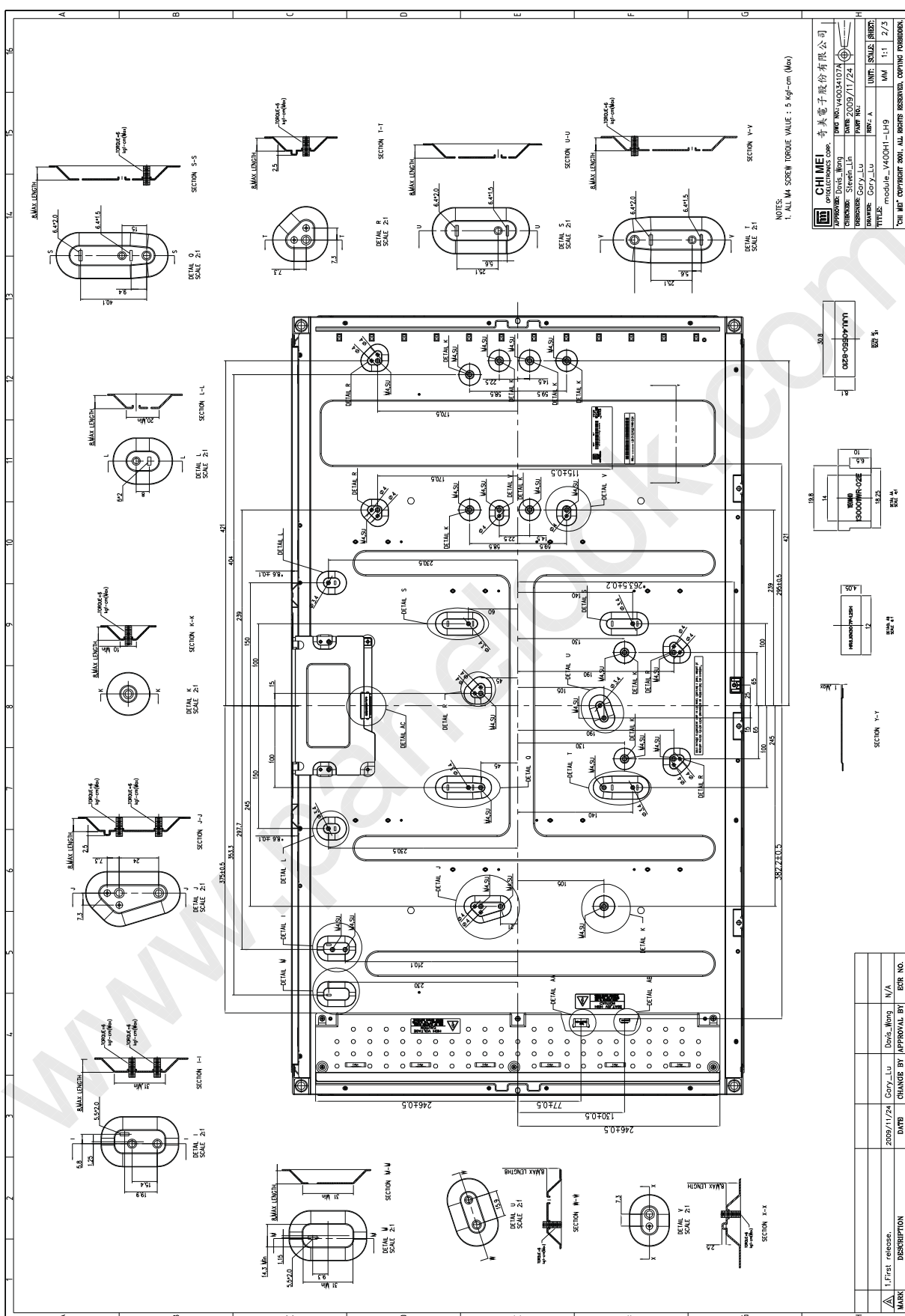
The LCD module should be certified with safety regulations as follows:

Regulatory	Item	Standard
Information Technology equipment	UL	UL 60950-1: 2007
	cUL	CAN/CSA C22.2 No.60950-1-03: 2007
	CB	IEC 60950 -1: 2005 EN60950-1: 2009
Audio/Video Apparatus	UL	UL 60065: 2007
	cUL	CAN/CSA C22.2 No.60065-03: 2006
	CB	IEC 60065: 2005 EN 60065: 2008

## 11. MECHANICAL CHARACTERISTICS



## PRODUCT SPECIFICATION



## PRODUCT SPECIFICATION

