CHI MEI OPTOELECTRONICS CORP.

Issued Date: Aug. 8, 2011
Model No.: V400H1 - LH5
Approval

☐ Tentative Specification
☐ Preliminary Specification
■ Approval Specification

MODEL NO.: V400H1
SUFFIX: LH5

Customer:

APPROVED BY **SIGNATURE**

Name / Title _____ _____

Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
Chao-Chun Chung	Ken Wu	Joanne Chung

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver 2.1	Aug. 08,'11	All	All	Approval Specification was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V400H1- LH5 is a 40" TFT Liquid Crystal Display module with 14-CCFL Backlight unit and 4ch-LVDS interface. This module supports 1920 x 1080 FHD format and can display true 1.07G colors (10-bits/color). The inverter module for backlight is not built-in.

1.2 FEATURES

-High brightness (500 nits)

- Ultra-high contrast ratio (4000:1)
- Faster response time (Gray to gray average 4.0ms)
- High color saturation NTSC 72%
- Ultra wide viewing angle : 176(H)/176(V) (CR>20) with Super MVA technology
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Color reproduction (nature color)
- Optimized response time for 120 Hz Frame rate
- Low color shift function
- RoHS compliance

1.3 APPLICATION

- TFT LCD TVs
- Multi-Media Display

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	885.6(H) x 498.15 (V) (40" diagonal)	mm	(1)
Bezel Opening Area	891.7 (H) x 504.2 (V)	mm	
Driver Element	a-si TFT active matrix	-	
Pixel Number	1920 x R.G.B. x 1080	pixel	
Pixel Pitch (Sub Pixel)	0.15375 (H) x 0.46125 (V)	mm	
Pixel Arrangement	RGB vertical stripe	-	
Display Colors	1.07G	color	
Display Operation Mode	Transmissive mode / Normally black	-	
Surface Treatment	Super Clear, Hard coating (3H)	-	

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	951	952	953	mm	(1)
	Vertical(V)	550	551	552	mm	(1)
	Depth(D)		47		mm	To Socket
	Depth(D)	51.2	52.2	53.2	mm	To C/B Cover
Weight		-	-	9570	-	g

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	-	50	G	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

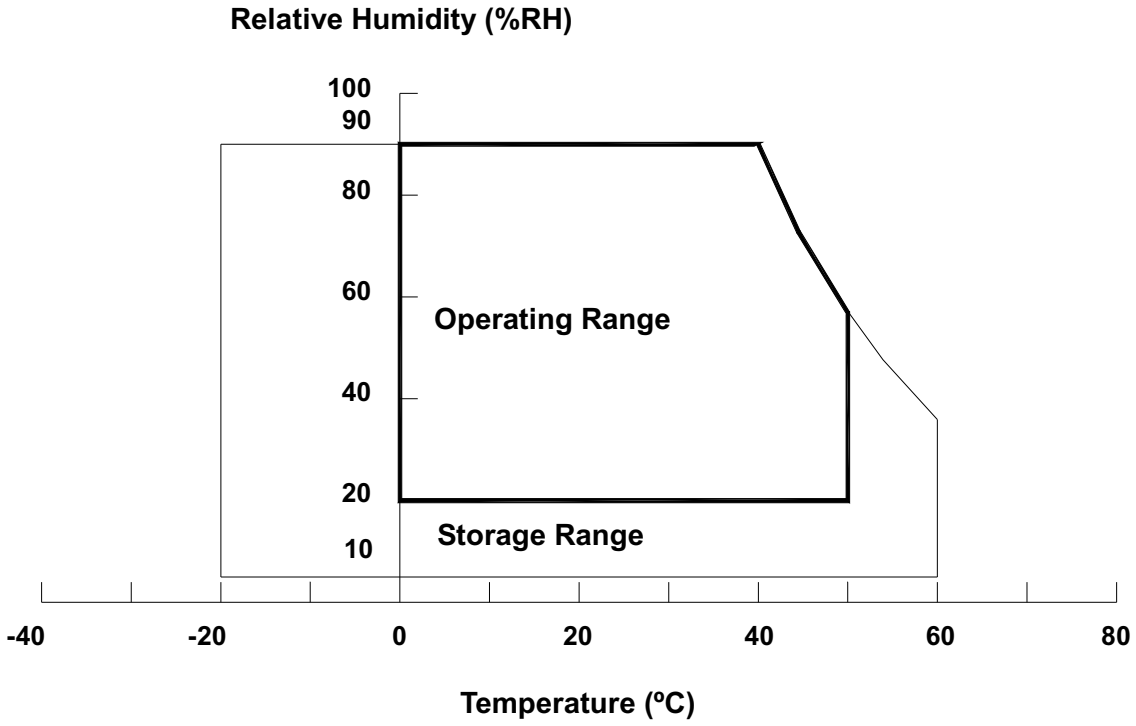
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

(a) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 ºC at normal humidity without condensation.

(b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	Vcc	-0.3	13.5	V	(1)
Input Signal Voltage	V_{IN}	-0.3	3.6	V	

2.3.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V_W	–	3000	V_{RMS}	

Note (1) No moisture condensation or freezing.

3. ELECTRICAL CHARACTERISTICS

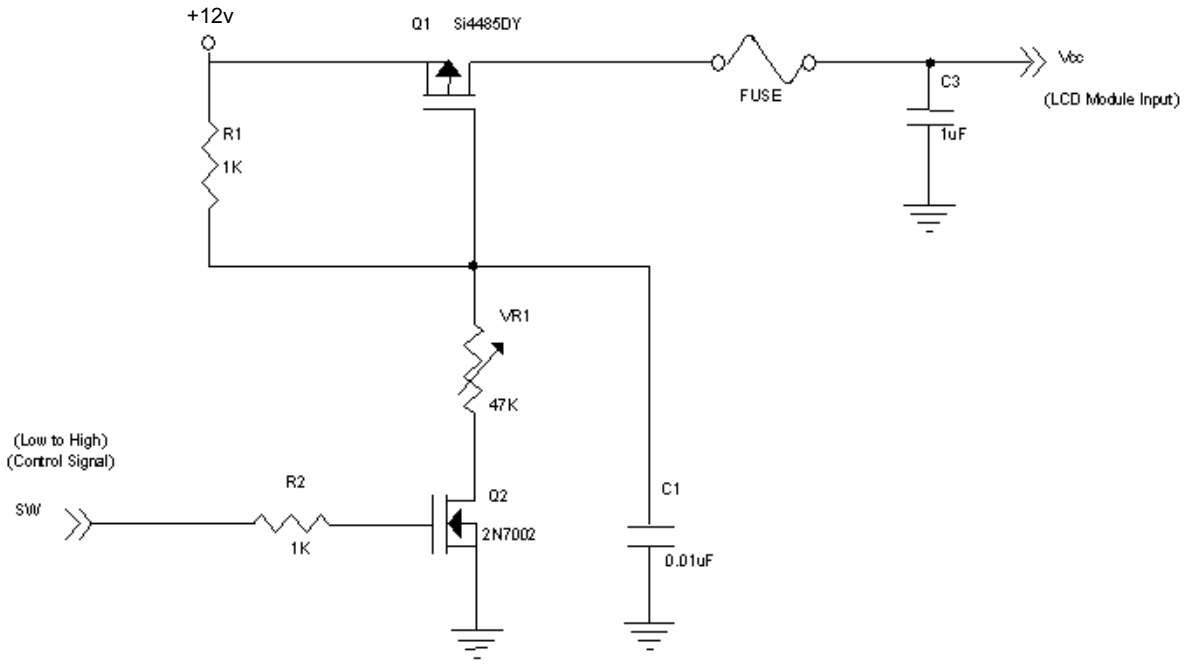
3.1 TFT LCD MODULE

Ta = 25 ± 2 ºC

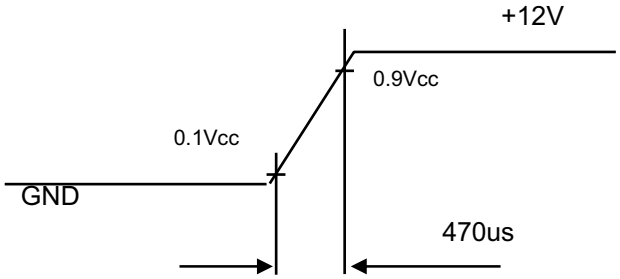
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12.0	13.2	V	(1)
Power Supply Ripple Voltage		V_{RP}	-	-	350	mV	
Rush Current		I_{RUSH}	-	-	4.5	A	(2)
Power Supply Current	White	I_{CC}	-	2.6	2.8	A	(3)
	Black		-	2	-	A	
	Vertical Stripe		-	2.6	-	A	
LVDS Interface	Common Input Voltage	V_{LVC}	1.125	1.25	1.375	V	
	Terminating Resistor	R_T	-	100	-	ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	-	0.7	V	

Note (1) The module should be always operated within above ranges.

Note (2) Measurement Conditions:



Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 ºC, f_v = 120 Hz, whereas a power dissipation check pattern below is displayed.

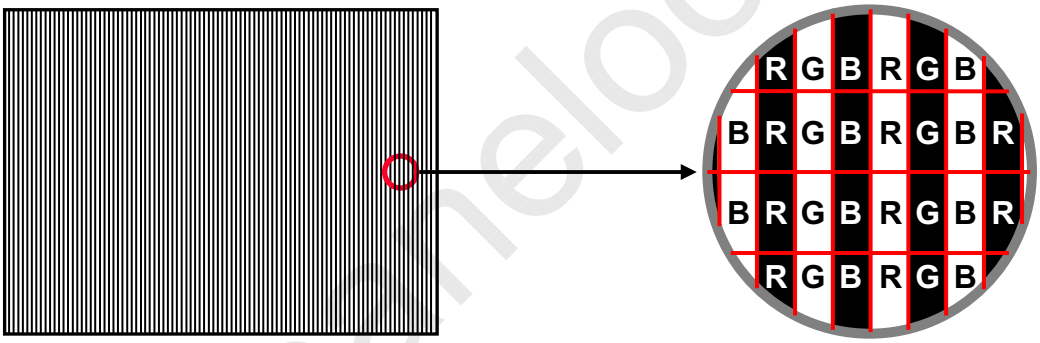
a. White Pattern

Active Area

b. Black Pattern

Active Area

c. Vertical Stripe Pattern



Active Area

3.2 BACKLIGHT UNIT

3.2.1 CCFL (Cold Cathode Fluorescent Lamp) CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Voltage	V_W	-	1020	-	V_{RMS}	Ih =11.0mA
Lamp Current	I_L	10.7	11.0	11.3	mA_{RMS}	(1)
Lamp Starting Voltage	V_S	-	-	1680	V_{RMS}	(2), Ta = 0 ºC
		-	-	1400	V_{RMS}	(2), Ta = 25 ºC
Operating Frequency	F_O	30	-	80	kHz	(3)
Lamp Life Time	L_{BL}	50,000	-	-	Hrs	(4), at 11.5mA

Note (1) Lamp current is measured by utilizing AC current probe and its value is average by measuring master and slave board.:

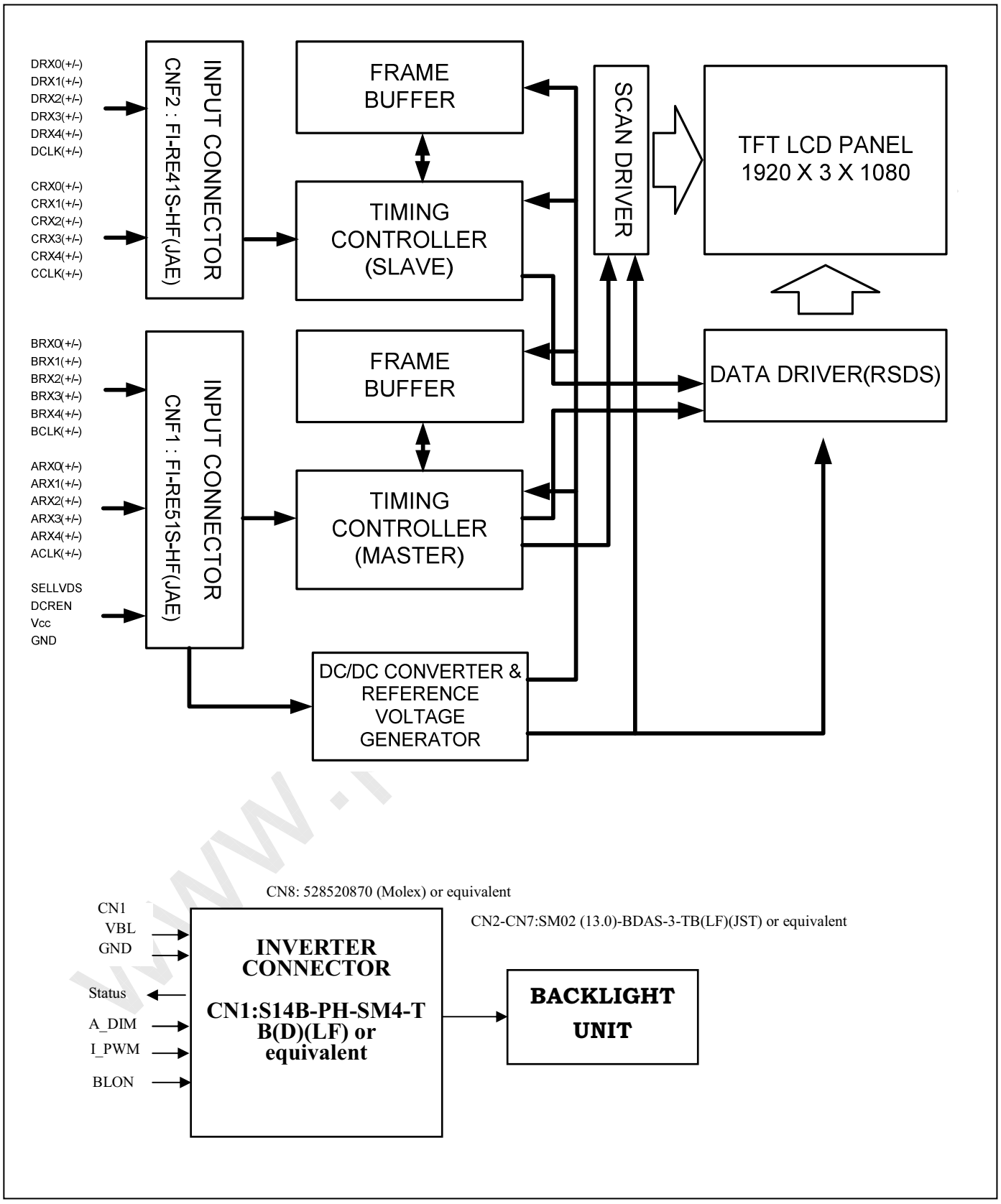
Note (2) The lamp starting voltage V_S should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency of the display input signals, and it may result in line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) The life time of a lamp is defined as when the brightness is larger than 50% of its original value and the effective discharge length is longer than 80% of its original length (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at the center point of lamp.) as the time in which it continues to operate under the condition at Ta = 25 ±2℃ and IL = 7.5~8.5 mArms.

4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



5. INTERFACE PIN CONNECTION

5.1 TFT LCD MODULE

CNF1 Connector Pin Assignment (FI-RE51S-HF(JAE) or equivalent)

Pin	Name	Description	Note
1	N.C.	No Connection	
2	N.C.	No Connection	(1)
3	N.C.	No Connection	(1)
4	AGE	Aging Mode Selection(0V~0.7V/Open→Disable, 2.7V ~ 3.3V →Enable)	
5	LUT1	Overdrive Lookup Table Selection(0V~0.7V/Open→60Hz, 2.7V ~ 3.3V →50Hz)	
6	FDOT	Force dot inversion (0V~0.7V/Open→Disable, 2.7V ~ 3.3V →Enable)	
7	SELLVDS	LVDS Data Format Selection	
8	N.C.	No Connection	(1)
9	N.C.	No Connection	(1)
10	N.C.	No Connection	(1)
11	GND	Ground	
12	ARX0-	First pixel Negative LVDS differential data input. Channel 0	(2)
13	ARX0+	First pixel Positive LVDS differential data input. Channel 0	
14	ARX1-	First pixel Negative LVDS differential data input. Channel 1	
15	ARX1+	First pixel Positive LVDS differential data input. Channel 1	
16	ARX2-	First pixel Negative LVDS differential data input. Channel 2	
17	ARX2+	First pixel Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	ACLK-	First pixel Negative LVDS differential clock input.	
20	ACLK+	First pixel Positive LVDS differential clock input.	
21	GND	Ground	
22	ARX3-	First pixel Negative LVDS differential data input. Channel 3	(2)
23	ARX3+	First pixel Positive LVDS differential data input. Channel 3	
24	ARX4-	First pixel Negative LVDS differential data input. Channel 4	
25	ARX4+	First pixel Positive LVDS differential data input. Channel 4	
26	N.C.	No Connection	(1)

27	N.C.	No Connection	(1)
28	BRX0-	Second pixel Negative LVDS differential data input. Channel 0	(2)
29	BRX0+	Second pixel Positive LVDS differential data input. Channel 0	
30	BRX1-	Second pixel Negative LVDS differential data input. Channel 1	
31	BRX1+	Second pixel Positive LVDS differential data input. Channel 1	
32	BRX2-	Second pixel Negative LVDS differential data input. Channel 2	
33	BRX2+	Second pixel Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	BCLK-	Second pixel Negative LVDS differential clock input.	
36	BCLK+	Second pixel Positive LVDS differential clock input.	
37	GND	Ground	
38	BRX3-	Second pixel Negative LVDS differential data input. Channel 3	(2)
39	BRX3+	Second pixel Positive LVDS differential data input. Channel 3	
40	BRX4-	Second pixel Negative LVDS differential data input. Channel 4	
41	BRX4+	Second pixel Positive LVDS differential data input. Channel 4	
42	N.C.	No Connection	(1)
43	N.C.	No Connection	(1)
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	N.C.	No Connection	(1)
48	VCC	+12V power supply	
49	VCC	+12V power supply	
50	VCC	+12V power supply	
51	VCC	+12V power supply	

CNF2 Connector Pin Assignment (FI-RE41S(JAE) or equivalent)

Pin	Name	Description	Note
1	GND	Ground	
2	N.C.	No Connection	(1)
3	N.C.	No Connection	(1)
4	N.C.	No Connection	(1)
5	N.C.	No Connection	(1)
6	N.C.	No Connection	(1)
7	N.C.	No Connection	(1)
8	N.C.	No Connection	(1)
9	GND	Ground	
10	CRX0-	Third pixel Negative LVDS differential data input. Channel 0	(2)
11	CRX0+	Third pixel Positive LVDS differential data input. Channel 0	
12	CRX1-	Third pixel Negative LVDS differential data input. Channel 1	
13	CRX1+	Third pixel Positive LVDS differential data input. Channel 1	
14	CRX2-	Third pixel Negative LVDS differential data input. Channel 2	
15	CRX2+	Third pixel Positive LVDS differential data input. Channel 2	
16	GND	Ground	
17	CCLK-	Third pixel Negative LVDS differential clock input.	
18	CCLK+	Third pixel Positive LVDS differential clock input.	
19	GND	Ground	
20	CRX3-	Third pixel Negative LVDS differential data input. Channel 3	(2)
21	CRX3+	Third pixel Positive LVDS differential data input. Channel 3	
22	CRX4-	Third pixel Negative LVDS differential data input. Channel 4	
23	CRX4+	Third pixel Positive LVDS differential data input. Channel 4	
24	N.C.	No Connection	(1)
25	N.C.	No Connection	(1)
26	DRX0-	Fourth pixel Negative LVDS differential data input. Channel 0	(2)
27	DRX0+	Fourth pixel Positive LVDS differential data input. Channel 0	
28	DRX1-	Fourth pixel Negative LVDS differential data input. Channel 1	
29	DRX1+	Fourth pixel Positive LVDS differential data input. Channel 1	

30	DRX2-	Fourth pixel Negative LVDS differential data input. Channel 2	
31	DRX2+	Fourth pixel Positive LVDS differential data input. Channel 2	
32	GND	Ground	
33	DCLK-	Fourth pixel Negative LVDS differential clock input.	
34	DCLK+	Fourth pixel Positive LVDS differential clock input.	
35	GND	Ground	
36	DRX3-	Fourth pixel Negative LVDS differential data input. Channel 3	(2)
37	DRX3+	Fourth pixel Positive LVDS differential data input. Channel 3	
38	DRX4-	Fourth pixel Negative LVDS differential data input. Channel 4	
39	DRX4+	Fourth pixel Positive LVDS differential data input. Channel 4	
40	N.C.	No Connection	(1)
41	N.C.	No Connection	(1)

Note (1) Please be reserved to open.

Note (2) LVDS 4-port Data Mapping

Port	Channel of LVDS	Data Stream
1st Port	First Pixel	1, 5, 9, ……1913, 1917
2nd Port	Second Pixel	2, 6, 10, ….1914, 1918
3rd Port	Third Pixel	3, 7, 11, ….1915, 1919
4th Port	Fourth Pixel	4, 8, 12, ….1916, 1920

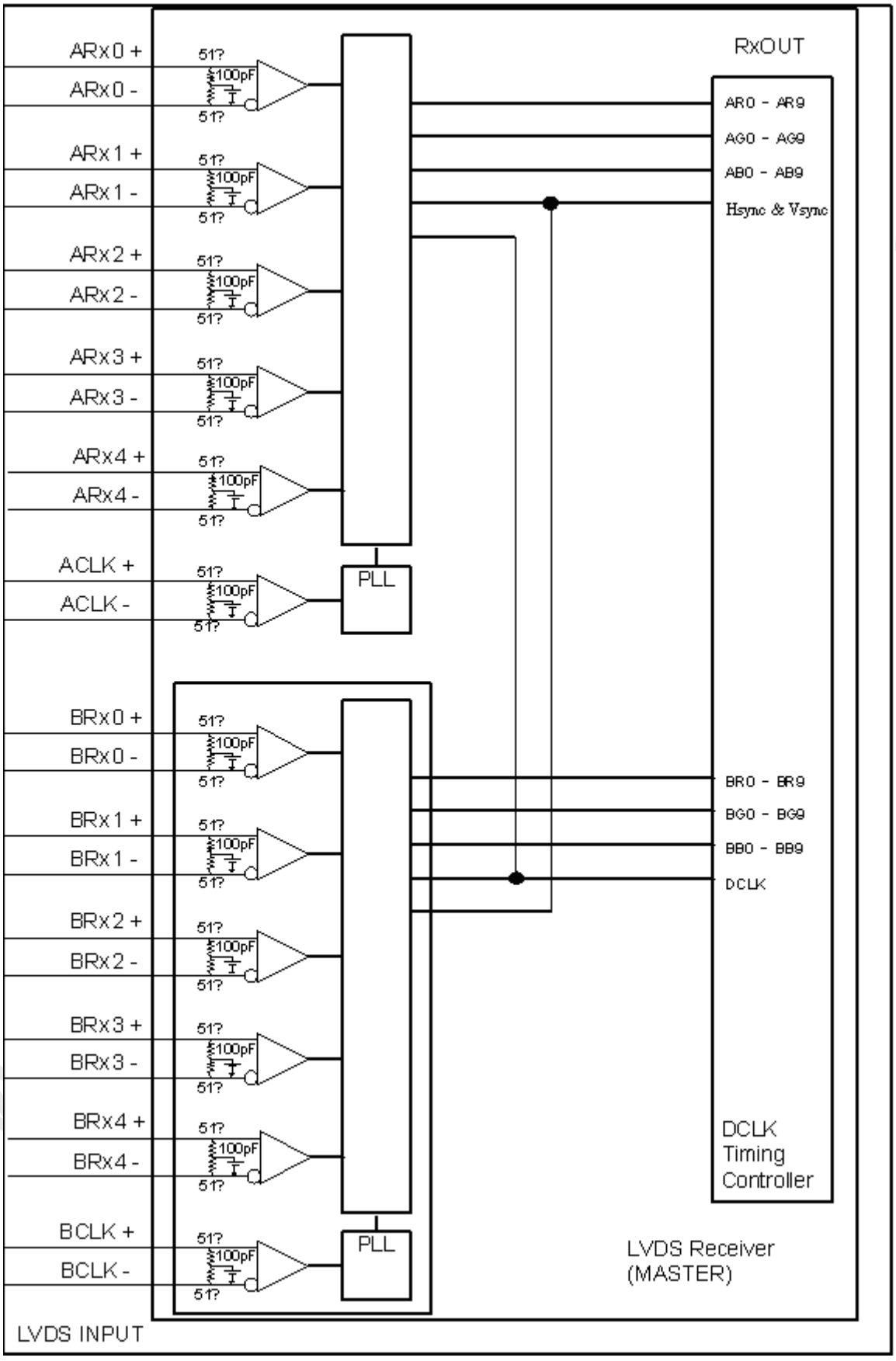
5.2 BACKLIGHT UNIT

The pin configuration for the housing and leader wire is shown in the table below.

Pin No.	Symbol	Description	Wire Color
NA	NA	NA	NA

Note (1) The backlight interface housing for high voltage side is a model 90050GS-40GLQ (SOCKET), manufactured by YEONHO.

5.3 BLOCK DIAGRAM OF INTERFACE



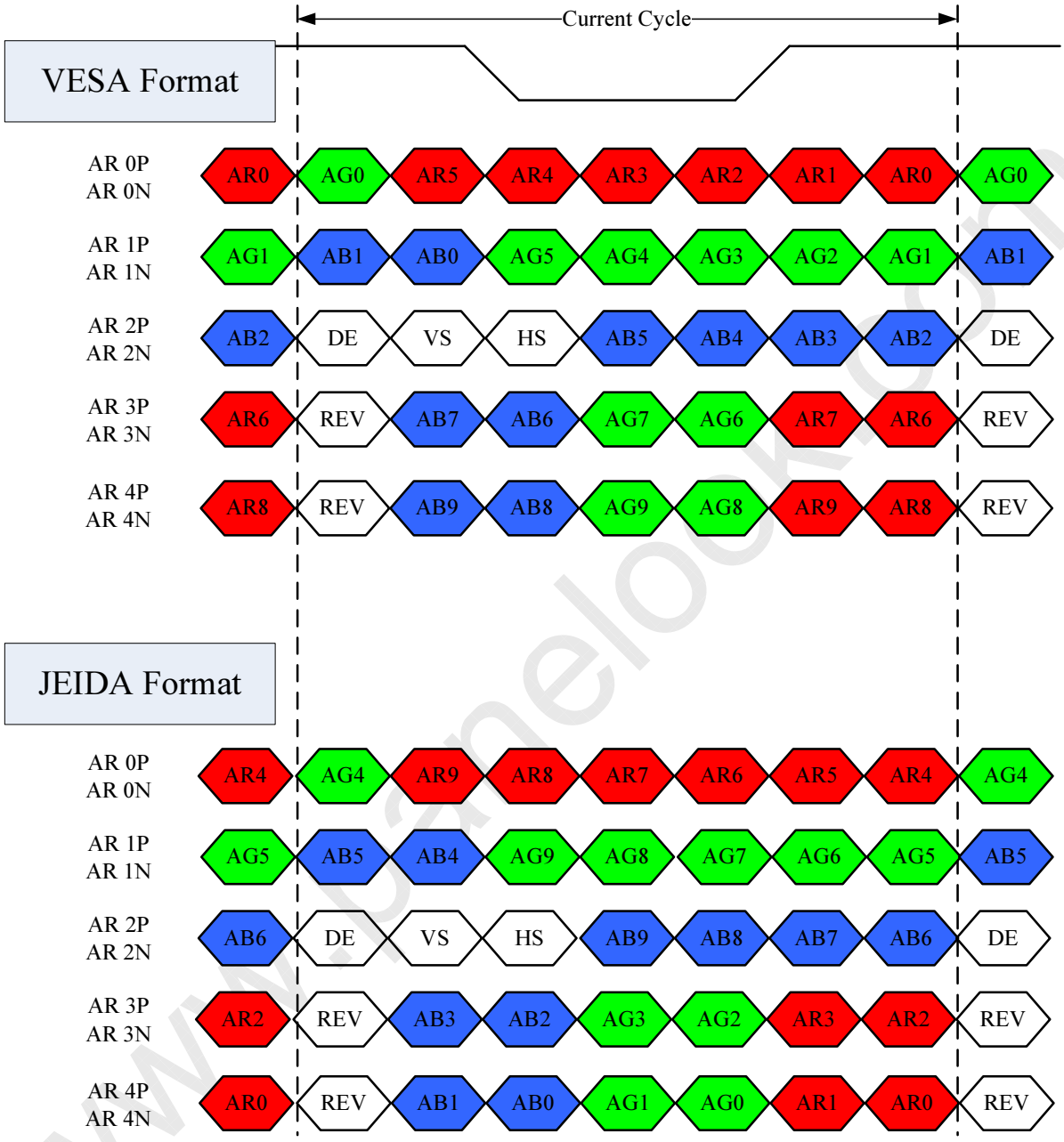
ER0~ER9 : Even pixel R data
EG0~EG9 : Even pixel G data
EB0~EB9 : Even pixel B data
OR0~OR9 : Odd pixel R data
OG0~OG9 : Odd pixel G data
OB0~OB9 : Odd pixel B data
DE : Data enable signal
DCLK : Data clock signal

Note (1) The system must have the transmitter to drive the module.
Note (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.
Note (3) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

5.4 LVDS INTERFACE

VESA Format : SELLVDS = L or Open

JEIDA Format : SELLVDS = H



AR0~AR9: First Pixel R Data (9; MSB, 0; LSB)

AG0~AG9: First Pixel G Data (9; MSB, 0; LSB)

AB0~AB9: First Pixel B Data (9; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

RSVD : Reserved

5.5 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																													
		Red										Green										Blue									
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
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	Green (1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	Green (1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1
	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

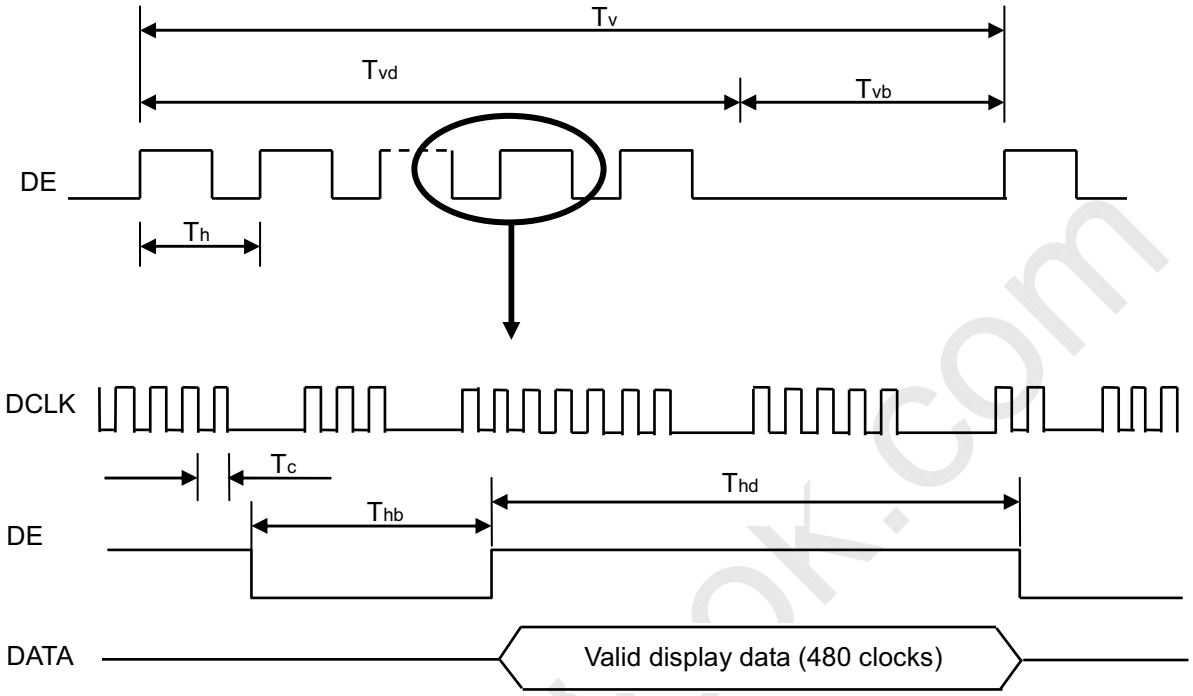
6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

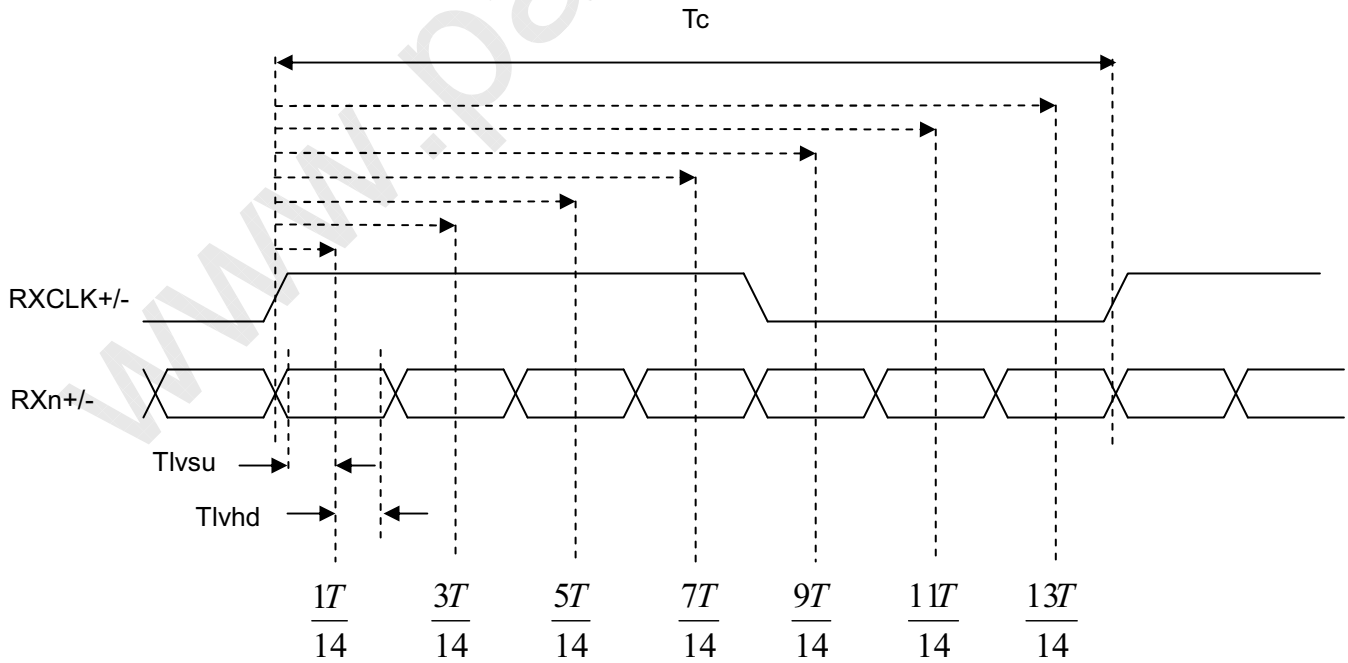
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	1/Tc	60	74.25	80-	MHz	
	Input cycle to cycle jitter	Trcl	-	-	200	ps	
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	
	Hold Time	Tlvhd	600	-	-	ps	
Vertical Active Display Term	Frame Rate	Fr	108.2	120	125	Hz	
	Total	Tv	1090	1125	1380	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	-
	Blank	Tvb	10	45	300	Th	-
Horizontal Active Display Term	Total	Th	520	550	680	Tc	Th=Thd+Thb
	Display	Thd	480	480	480	Tc	-
	Blank	Thb	40	70	200	Tc	-

Note (1) Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

INPUT SIGNAL TIMING DIAGRAM

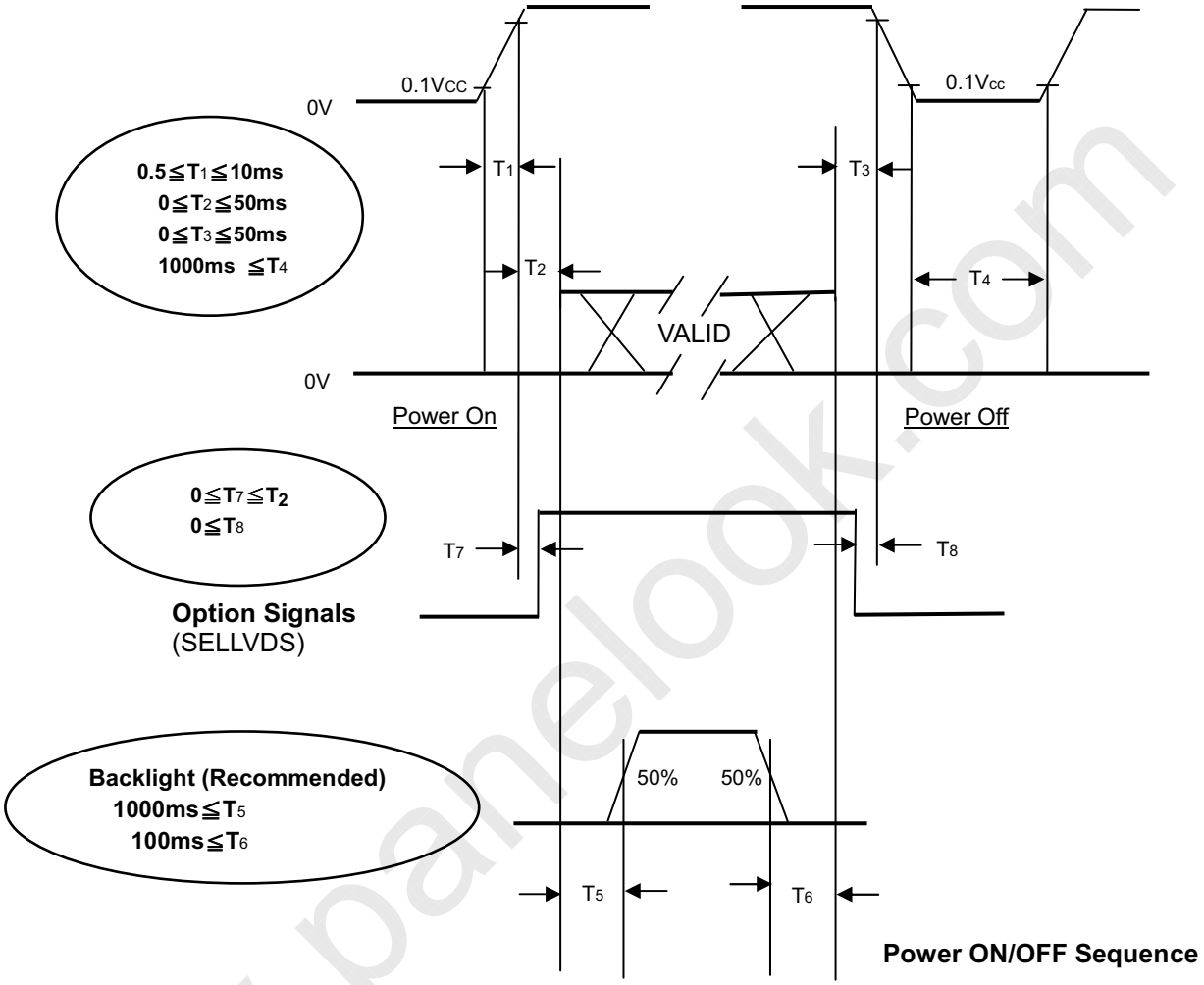


LVDS RECEIVER INTERFACE TIMING DIAGRAM



6.3 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	12	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current(HV)	I_L	8.0 ± 0.3	mA
Oscillating Frequency (Balance Board)	F_W	48±3	KHz
Frame rate		120	Hz

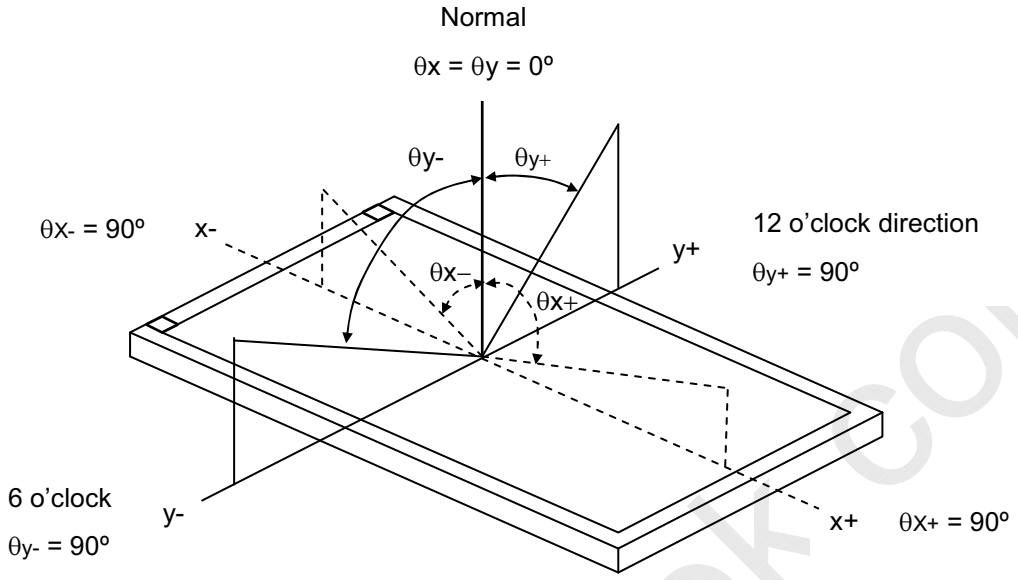
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing angle at Normal direction	3000	4000	-	-	(2)
Response Time		Gray to gray average		-	4	8	ms	(3)
Center Luminance of White		L_C		450	500	-	cd/	(4)
White Variation		δW		-	-	1.3	-	(7)
Cross Talk		CT		-	-	4.0	%	(5)
Color Chromaticity	Red	Rx		Typ. – 0.03	0.635	Typ. + 0.03	-	(6)
		Ry			0.323		-	
	Green	Gx			0.285		-	
		Gy			0.602		-	
	Blue	Bx			0.148		-	
		By			0.056		-	
	White	Wx			0.280		-	
		Wy			0.290		-	
	Color Gamut	CG		70	72		%	NTSC
Viewing Angle	Horizontal	θ_x+	CR≥20	80	88	-	Deg.	(1)
		θ_x-		80	88	-		
	Vertical	θ_Y+		80	88	-		
		θ_Y-		80	88	-		

Note (1) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by EZ-Contrast 160R (Eldim)



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

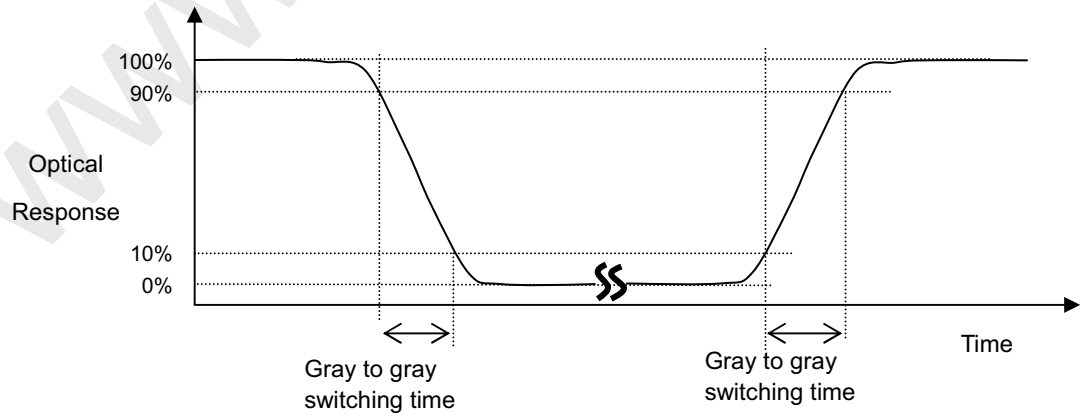
Contrast Ratio (CR) = L1023 / L0

L1023: Luminance of gray level 1023

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (7).

Note (3) Definition of Gray to Gray Switching Time :



The driving signal means the signal of gray level 0, 252, 508, 764, 1023.

Gray to gray average time means the average switching time of gray level 0, 252, 508, 764, 1023 to each other.

Note (4) Definition of Luminance of White (L_C, L_{AVE}):

Measure the luminance of gray level 1023 at center point and 5 points

$L_C = L(5)$

$L_{AVE} = [L(1)+ L(2)+ L(3)+ L(4)+ L(5)] / 5$

where L (x) is corresponding to the luminance of the point X at the figure in Note (7).

Note (5) Definition of Cross Talk (CT):

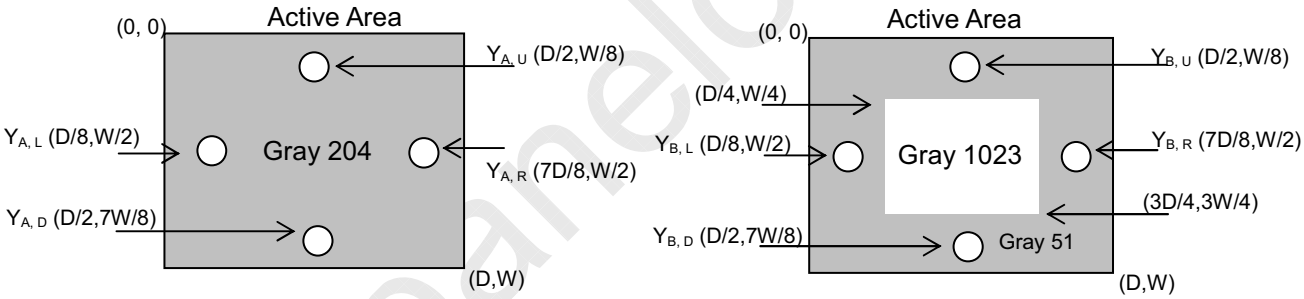
$CT = | Y_B – Y_A | / Y_A \times 100$ (%)

Where:

(a)

Y_A = Luminance of measured location without gray level 1023 pattern (cd/m^2)

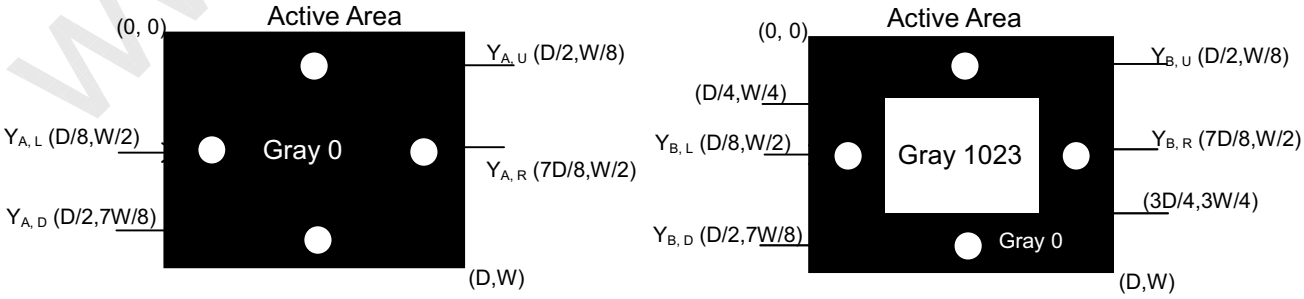
Y_B = Luminance of measured location with gray level 1023 pattern (cd/m^2)



(b)

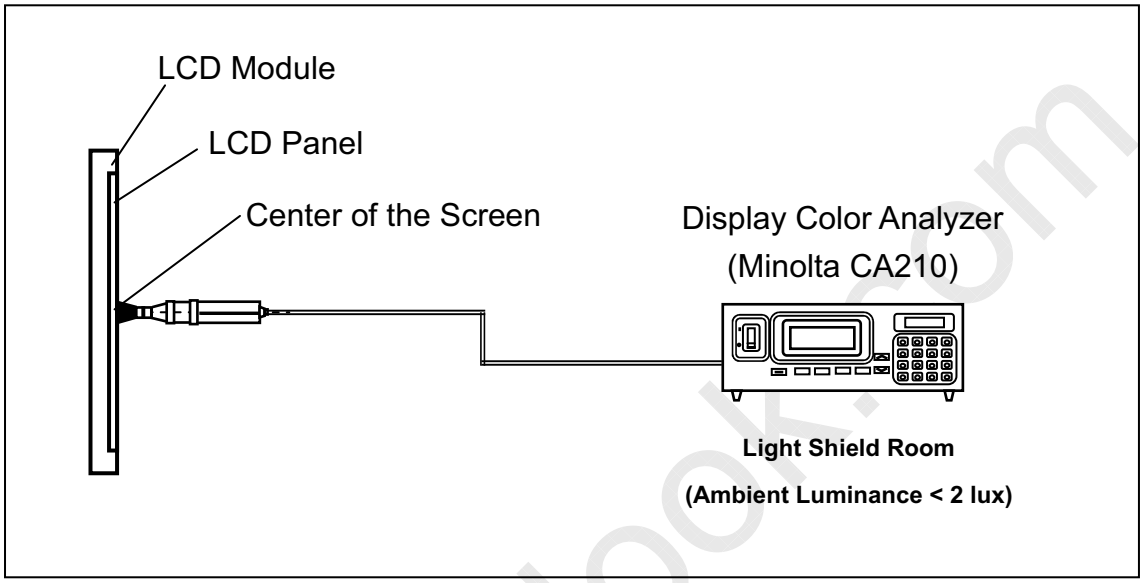
Y_A = Luminance of measured location without gray level 1023 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 1023 pattern (cd/m^2)



Note (6) Measurement Setup:

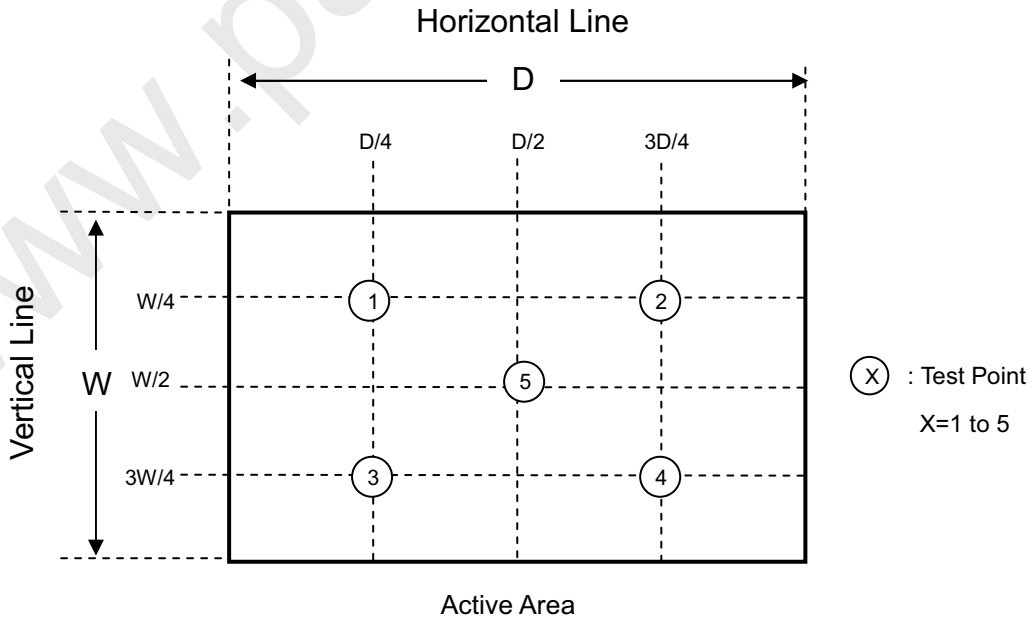
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 1 hour in a windless room.



Note (7) Definition of White Variation (δW):

Measure the luminance of gray level 1023 at 5 points

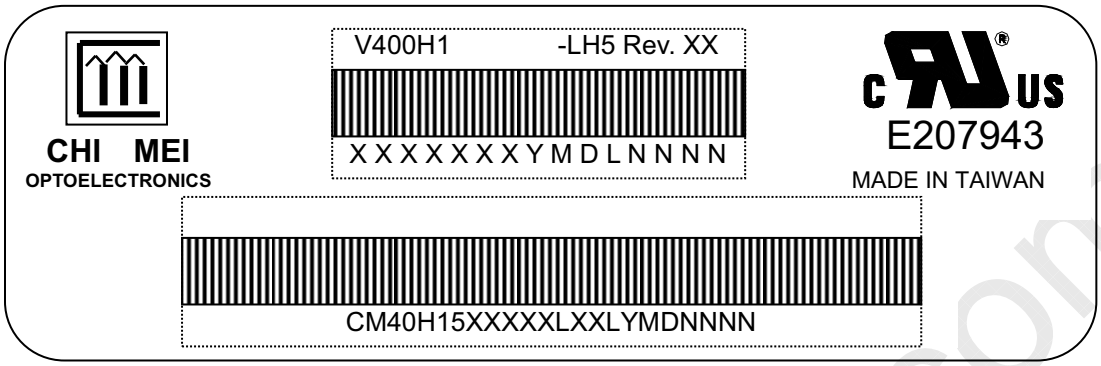
δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



8. DEFINITION OF LABELS

8.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: V400H1-LH5

(b) Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

(c) CMO barcode definition:

Serial ID: XX-XX-X-XX-YMD-L-NNNN

Code	Meaning	Description
XX	CMO internal use	-
XX	Revision	Cover all the change
X-XX	CMO internal use	-
YMD	Year, month, day	Year: 2001=1, 2002=2, 2003=3, 2004=4… Month: Jan. ~ Dec.=1, 2, 3, ~, 9, A, B, C Day: 1st to 31st =1, 2, 3, ~, 9, A, B, C, ~, W, X, Y, exclude I, O, and U
L	Product line #	Line 1=1, Line 2=2, Line 3=3, …
NNNN	Serial number	Manufacturing sequence of product

(d) Customer's barcode definition:

Serial ID: CM-40H15-X-X-X-XX-L-XX-L-YMD-NNNN

Code	Meaning	Description
CM	Supplier code	CMO=CM
40H15	Model number	V400H1-LH5=40H15
X	Revision code	C1=A, C2=B, ……C9=I
X	Source driver IC code	Century=1, CLL=2, Demos=3, Epson=4, Fujitsu=5, Himax=6, Hitachi=7, Hynix=8, LDI=9, Matsushita=A, NEC=B, Novatec=C, OKI=D, Philips=E, Renasas=F, Samsung=G, Sanyo=H, Sharp=I, TI=J, Topro=K, Toshiba=L, Windbond=M
X	Gate driver IC code	
XX	Cell location	Tainan, Taiwan=TN
L	Cell line #	1~12=0~C
XX	Module location	Tainan, Taiwan=TN
L	Module line #	1~12=0~C
YMD	Year, month, day	Year: 2001=1, 2002=2, 2003=3, 2004=4… Month: Jan. ~ Dec.=1, 2, 3, ~, 9, A, B, C Day: 1st to 31st =1, 2, 3, ~, 9, A, B, C, ~, W, X, Y, exclude I, O, and U
NNNN	Serial number	By LCD supplier

9. PACKAGING

9.1 PACKING SPECIFICATIONS

(1) 4 LCD TV modules / 1 Box

(2) Box dimensions：1040(L) X 310 (W) X 640(H)

(3) Weight：approximately 47Kg (4 modules per box)

9.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method

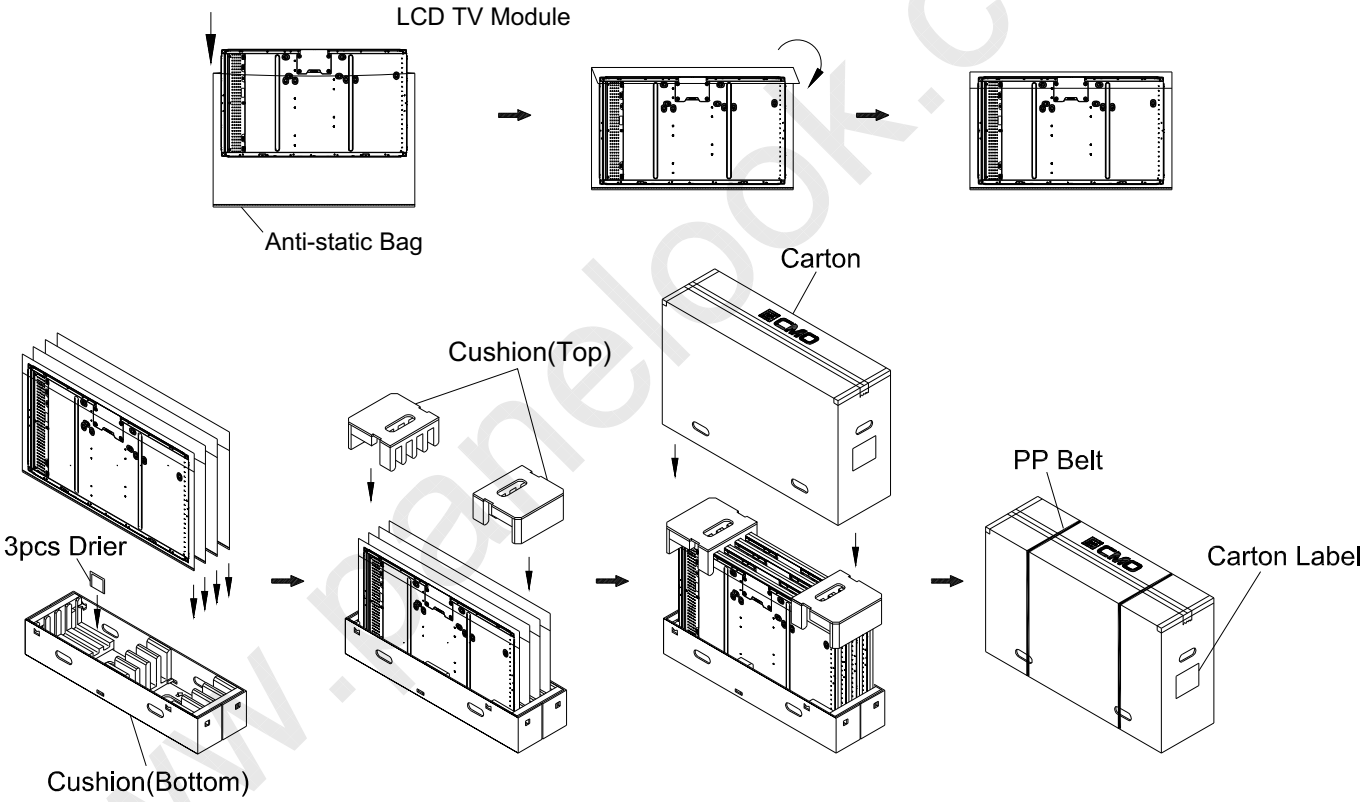
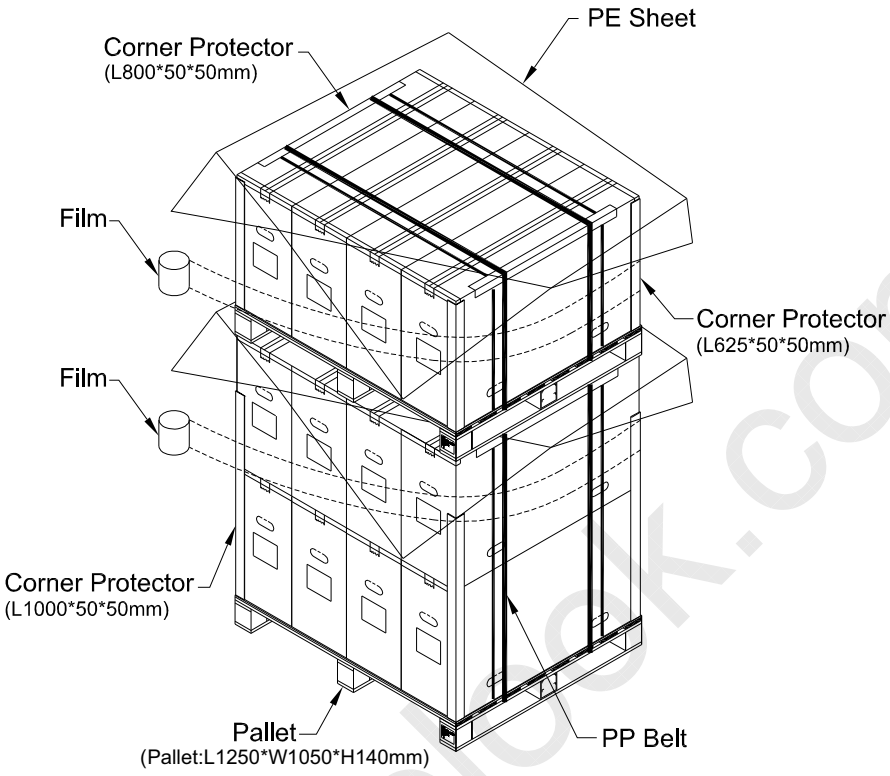


Figure.9-1 packing method

Sea / Land Transportation (40ft Container)



Air Transportation

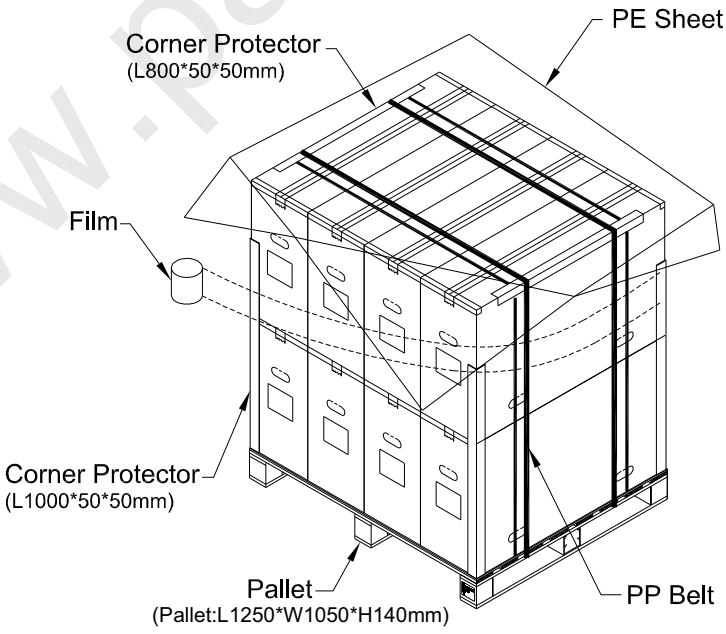


Figure. 9-2 Packing method

10. PRECAUTIONS

10.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and backlight.

(4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

(5) Do not plug in or pull out the I/F connector while the module is in operation.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) Moisture can easily penetrate into LCD module and may cause the damage during operation.

(9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.

(10) When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

10.2 SAFETY PRECAUTIONS

(1) The startup voltage of a backlight is over 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the backlight unit.

(2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(3) After the module's end of life, it is not harmful in case of normal operation and storage.

10.3 SAFETY STANDARDS

The LCD module should be certified with safety regulations as follows:

Regulatory	Item	Standard
Information Technology equipment	UL	UL 60950-1:2006
	cUL	CAN/CSA C22.2 No.60950-1-03: 2006
	CB	IEC 60950 -1:2005
Audio/Video Apparatus	UL	UL 60065:2006
	cUL	CAN/CSA C22.2 No.60065-03: 2006
	CB	IEC 60065:2006

11. MECHANICAL CHARACTERISTICS