



- ☐ Tentative Specification
- ☐ Preliminary Specification
- ☒ Approval Specification

MODEL NO.: V400H1
SUFFIX: L12

Customer: SEC

APPROVED BY

SIGNATURE

Name / Title

Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
Chao-Chun Chung	Josh Chi	Joanne Chung

**CONTENTS**

1. GENERAL DESCRIPTION	5
1.1 OVERVIEW	5
1.2 FEATURES	5
1.3 APPLICATION	5
1.4 GENERAL SPECIFICATIONS	5
1.5 MECHANICAL SPECIFICATIONS	6
2. ABSOLUTE MAXIMUM RATINGS	7
2.1 ABSOLUTE RATINGS OF ENVIRONMENT	7
2.2 PACKAGE STORAGE	8
2.3 ELECTRICAL ABSOLUTE RATINGS	8
2.3.1 TFT LCD MODULE	8
2.3.2 BACKLIGHT BALANCE BOARD UNIT	8
3. ELECTRICAL CHARACTERISTICS	9
3.1 TFT LCD MODULE	9
3.2 BACKLIGHT CONNECTOR PIN CONFIGURATION	12
3.2.1 LAMP SPECIFICATION (Ta = 25 ± 2 °C)	12
3.2.2 ELECTRICAL SPECIFICATION	12
4. BLOCK DIAGRAM OF INTERFACE	15
4.1 TFT LCD MODULE	15
5. INPUT TERMINAL PIN ASSIGNMENT	16
5.1 TFT LCD Module Input	16
5.2 BACKLIGHT UNIT	18
5.3 BALANCE BOARD UNIT	18
5.4 BLOCK DIAGRAM OF INTERFACE	20
5.5 LVDS INTERFACE	22
5.6 COLOR DATA INPUT ASSIGNMENT	23
6. INTERFACE TIMING	24
6.1 INPUT SIGNAL TIMING SPECIFICATIONS	24
6.2 POWER ON/OFF SEQUENCE	27
7. OPTICAL CHARACTERISTICS	28
7.1 TEST CONDITIONS	28



7.2 OPTICAL SPECIFICATIONS	29
8. PRECAUTIONS	34
8.1 ASSEMBLY AND HANDLING PRECAUTIONS	34
8.2 SAFETY PRECAUTIONS	34
9. DEFINITION OF LABELS	35
9.1 CMI MODULE LABEL	35
10. PACKAGING	36
10.1 PACKAGING SPECIFICATIONS	36
10.2 PACKAGING METHOD	37
11. MECHANICAL CHARACTERISTIC	39

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V400H1-L12 is a 40" TFT Liquid Crystal Display module with 12-CCFL Backlight unit and 2ch-LVDS interface. This module supports 1920 x 1080 Full HDTV format and can display 16.7M colors (8-bit). The balance board module for backlight is built-in.

1.2 FEATURES

- High brightness (500 nits)
- High contrast ratio (6000:1)
- Fast response time (Gray to gray average 8.5 ms)
- High color saturation (NTSC 72%)
- Full HDTV (1920 x 1080 pixels) resolution, true HDTV format
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 60 Hz frame rate
- Ultra wide viewing angle : Super MVA technology
- Viewing Angle : 160(H)/150(V) (CR>10) TN Technology
- RoHs compliance

1.3 APPLICATION

- Standard Living Room TVs
- Public Display Application
- Home Theater Application
- MFM Application

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	885.6(H) x 498.15 (V) (40" diagonal)	mm	(1)
Bezel Opening Area	891.7 (H) x 504.8 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920 x R.G.B. x 1080	pixel	-
Pixel Pitch(Sub Pixel)	0.15375 (H) x 0.46125 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7M	color	-
Display Operation Mode	Transmissive mode / Normally Black	-	-
Surface Treatment	Anti-Glare coating (Haze 11%)	-	(2)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) The spec. of the surface treatment is temporarily for this phase. CMI reserves the rights to change this feature.

**1.5 MECHANICAL SPECIFICATIONS**

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	951	952	953	mm	(1)
	Vertical (V)	550	551	552	mm	(1)
	Depth (D)	-	-	-	mm	(2)
	Depth (D)	56.3	57.3	58.3	mm	(3)
Weight		-	9320	-	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth is between bezel to T-CON cover.

Note (3) Module Depth is between bezel to Balance board cover.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	+60	°C	(1)
Operating Ambient Temperature	TOP	0	50	°C	(1), (2)
Shock (Non-Operating)	SNOP	-	50	G	(3), (5)
Vibration (Non-Operating)	VNOP	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. ($T_a \leq 40\text{ }^{\circ}\text{C}$).

(b) Wet-bulb temperature should be 39 °C Max. ($T_a > 40\text{ }^{\circ}\text{C}$).

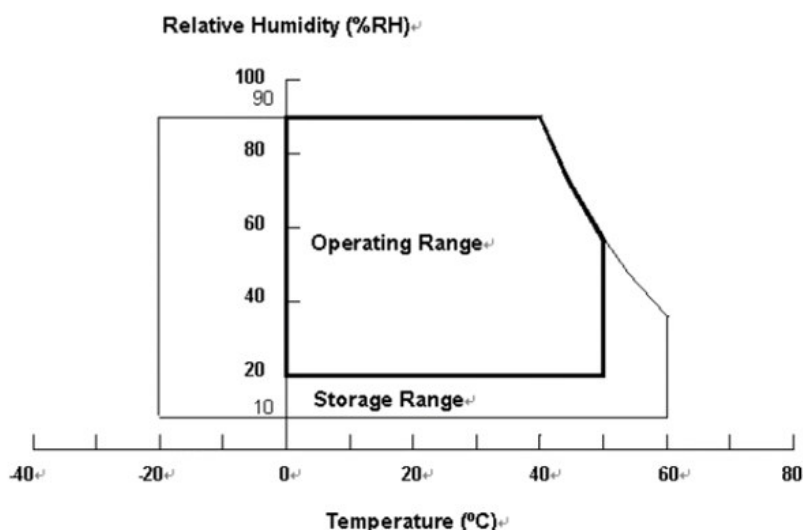
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for $\pm X$, $\pm Y$, $\pm Z$.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



**2.2 PACKAGE STORAGE**

When storing modules as spares for a long time, the following precaution is necessary.

- (a) Do not leave the module in high temperature, and high humidity for a long time, It is highly recommended to store the module with temperature from 0 to 35 °C at normal humidity without condensation.
- (b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS**2.3.1 TFT LCD MODULE**

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	13.5	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

2.3.2 BACKLIGHT BALANCE BOARD UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V	—	3000	VRMS	Lamp Voltage
IP Board Supply Voltage	High / Low	195 (Low)	390 (High)	Vrms	IP Board Supply Voltage
Control Signal Level	—	-0.3	15	V	Control Signal Level

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals include On/Off Control and Internal PWM Control.

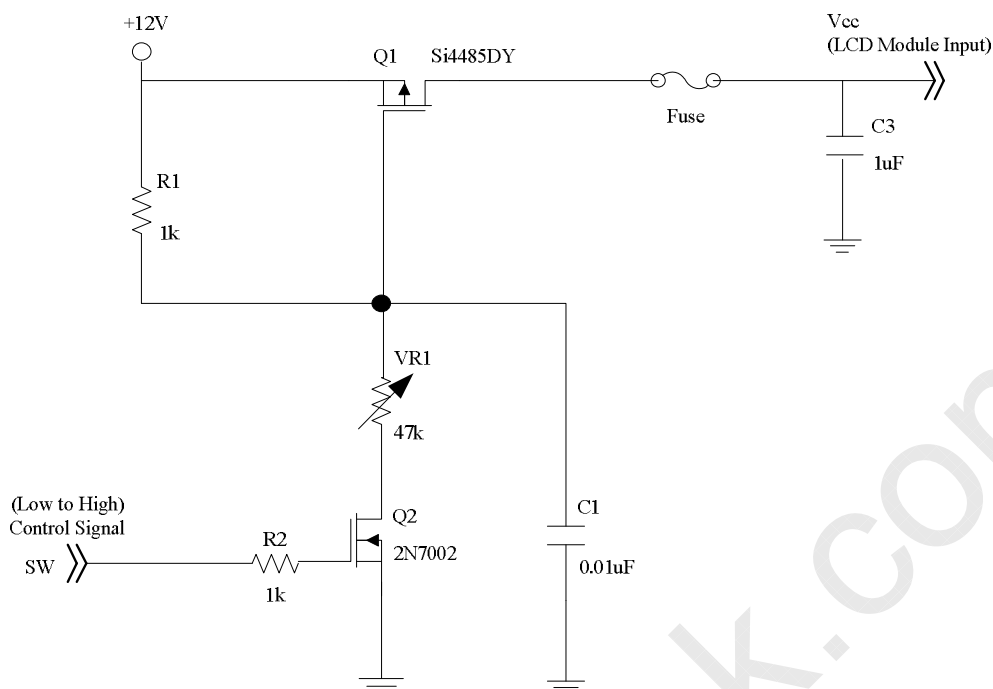
**3. ELECTRICAL CHARACTERISTICS****3.1 TFT LCD MODULE**

(Ta = 25 ± 2 °C)

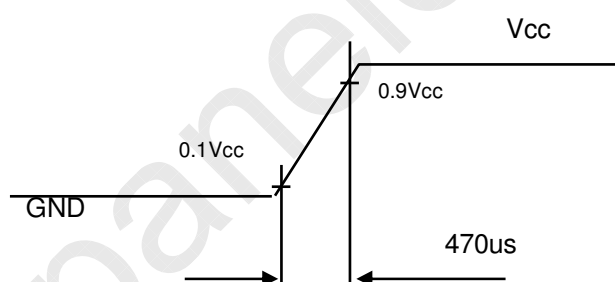
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V _{CC}	10.8	12	13.2	V	(1)
Rush Current		I _{RUSH}	—	—	2.5	A	(2)
Power consumption	White Pattern	P _T	—	10.9	13.2	W	(3)
	Black Pattern		—	7.2	9.6		
	Horizontal Stripe		—	10.8	13.2		
Power Supply Current	White Pattern	—	—	0.91	1.1	A	(3)
	Black Pattern	—	—	0.66	0.8	A	
	Horizontal Stripe	—	—	0.9	1.1	A	
LVDS interface	Differential Input High Threshold Voltage	V _{LVTH}	+100	—	—	mV	(4)
	Differential Input Low Threshold Voltage	V _{LVTL}	—	—	-100	mV	
	Common Input Voltage	V _{CM}	1.0	1.2	1.4	V	
	Differential input voltage (single-end)	V _{ID}	200	—	600	mV	
	Terminating Resistor	R _T	—	100	—	ohm	
CMIS interface	Input High Threshold Voltage	V _{IH}	2.7	—	3.3	V	
	Input Low Threshold Voltage	V _{IL}	0	—	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:

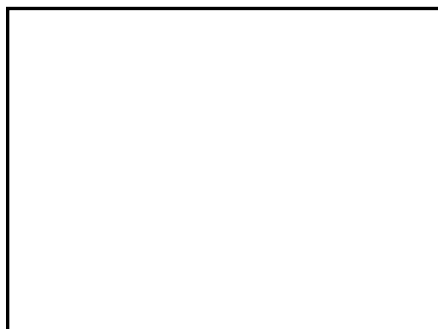


Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at $V_{cc} = 12\text{ V}$, $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$, $f_v = 60\text{ Hz}$, whereas a power dissipation check pattern below is displayed.

a. White Pattern



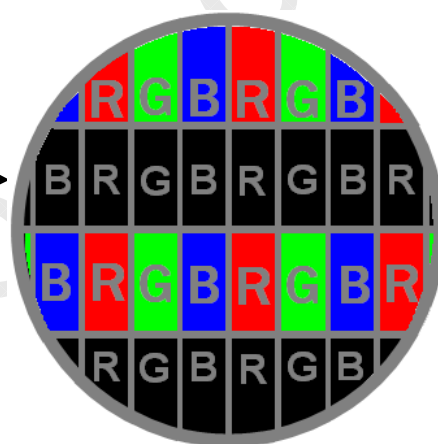
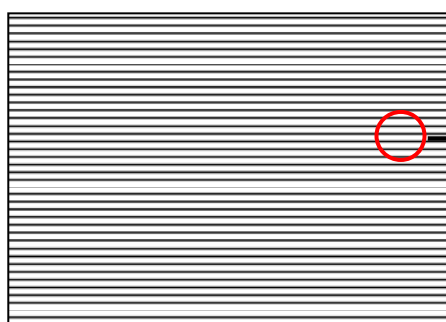
Active Area

b. Black Pattern

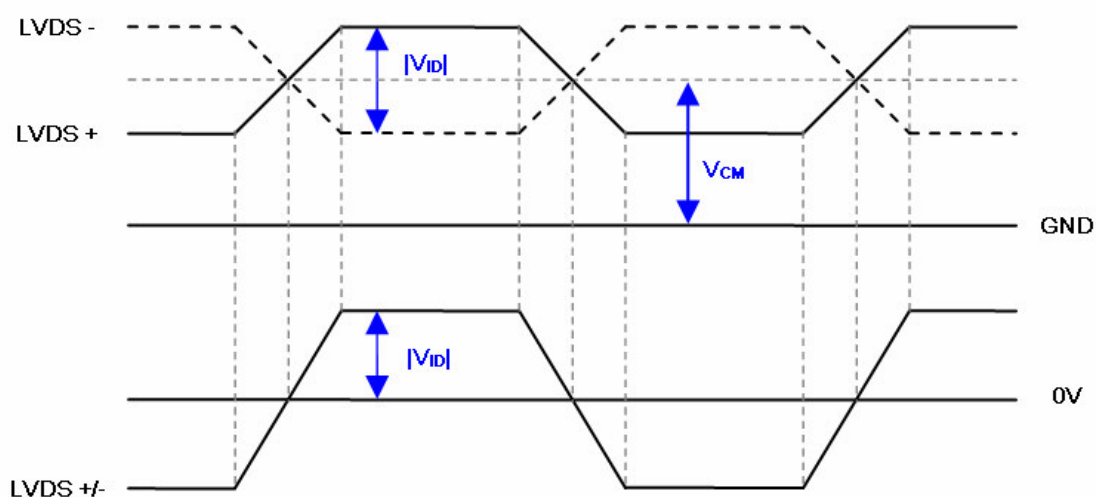


Active Area

c. Horizontal Pattern



Note (4) The LVDS input characteristics are as follows :



3.2 BACKLIGHT CONNECTOR PIN CONFIGURATION

3.2.1 LAMP SPECIFICATION (Ta = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V _W	-	840	-	V _{RMS}	I _L =14.5mA
Lamp Current	I _L	3	14.5	15	mA _{RMS}	
Lamp Turn On Voltage	V _S	-	-	1320	V _{RMS}	(1), Ta = 0 °C
		-	-	1190	V _{RMS}	(1), Ta = 25 °C
Operating Frequency	F _O	30	-	80	KHz	(2)
Lamp Life Time	L _{BL}	50,000	-	-	Hrs	(3)

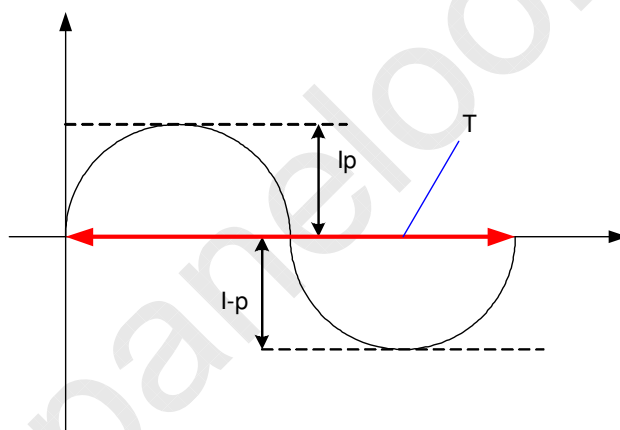
3.2.2 ELECTRICAL SPECIFICATION

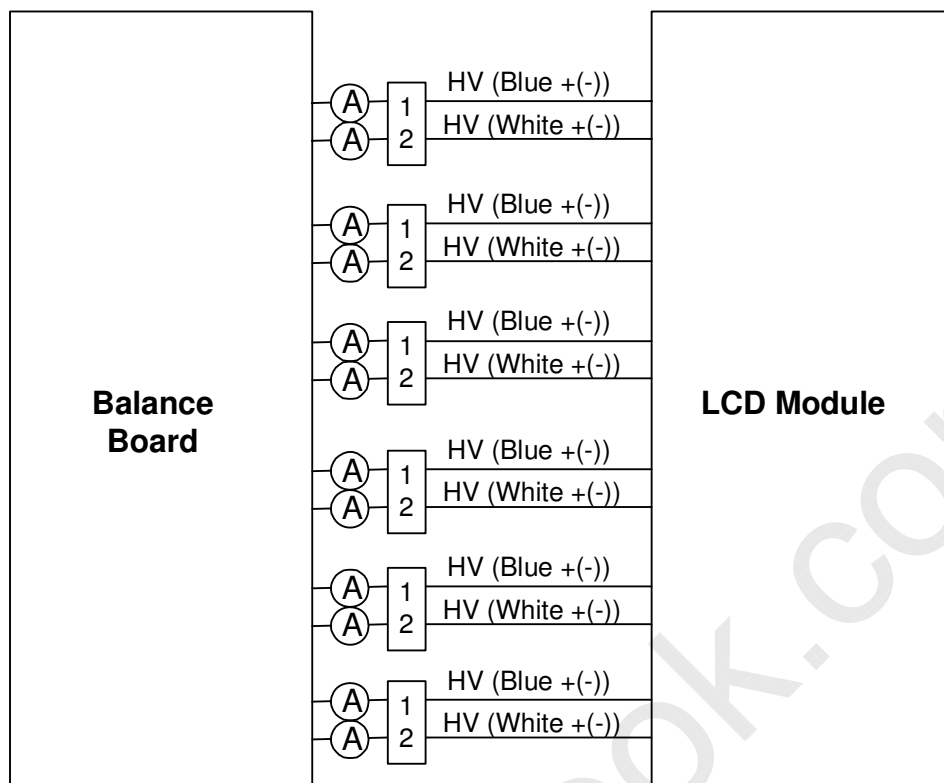
(Ta = 25 ± 2 °C)

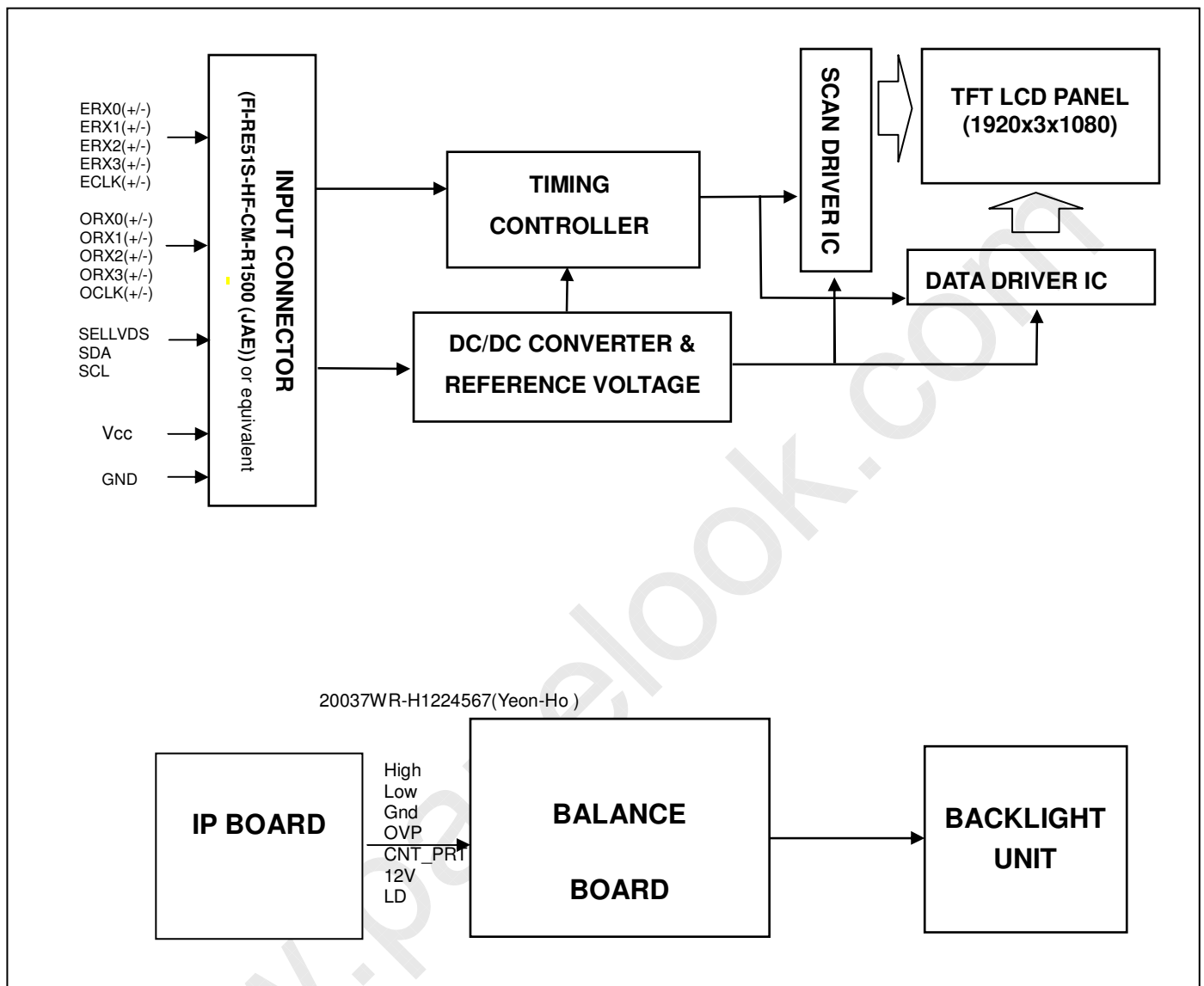
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Input High Voltage		High	380	390	400	Vrms	(6)
Input Low Voltage		Low	190	195	200	V	
Protection Circuit Supply Voltage		V _{CC}	11	13	15	V	
Power Consumption		P _{IP}	-	145	150	W	No Dimming (IPB input)
Input Current		I _{TB}		0.372	0.385	Arms	Measure TBB HIGH(390V)
Oscillating Frequency		F _W	43	45	47	kHz	
Individual Lamp Current		I _L	13.5	14.5	15.5	mA	(5)
Connector Detection	High	CNTPRT	V _{CC} -0.5	-	V _{CC}	V	Normal Operation
	Low	CNTPRT	-	-	1	V	Input Connector Open
All Lamp Open Detection	High	LD	V _{CC} -0.5	-	V _{CC}	V	Normal Operation
	Low	LD	-	-	1	V	All Lamp Open
One Lamp Open Detection	High	OVP	1.25	-	-	V	Normal Operation
	Low	OVP	0	-	0.8	V	One Lamp Open
Dimming frequency		F _B	140	150	160	Hz	
Minimum Duty Ratio		D _{MIN}	12	15	18	%	Note.8
Striking time		tsriking	1	-	2	sec	
Shutdown time		Tsd	1	1.5	2	sec	

Note (1) Lamp current is measured by utilizing AC current probe and its value is average by measuring master and slave board.:

- Note (2) The lamp starting voltage V_s should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.
- Note (3) The lamp frequency may produce interference with horizontal synchronous frequency of the display input signals, and it may result in line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.
- Note (4) The life time of a lamp is defined as when the brightness is larger than 50% of its original value and the effective discharge length is longer than 80% of its original length (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at the center point of lamp.) as the time in which it continues to operate under the condition at $T_a = 25 \pm 2^\circ\text{C}$ and $I_L = 13.5 \sim 15.5 \text{ mA}_{\text{rms}}$.
- Note (5) Lamp current is measured master board by utilizing high frequency current meters as shown below:
- Note (6) Input voltage H_v based on spec. $\pm 7\%$ tolerance.
- Note (7) Asymmetric ratio must be from 90% to 110% ($0.9 < I_p / I_{\text{rms}@T/2X\sqrt{2}} < 1.1$)
- Note (8) The minimum dimming under 3% operation should cause shutdown by protection circuit.





4. BLOCK DIAGRAM OF INTERFACE**4.1 TFT LCD MODULE**

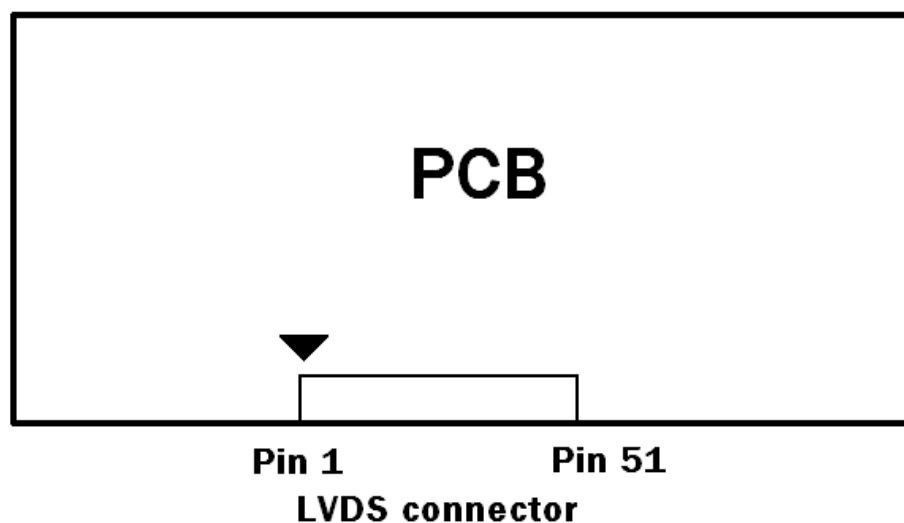
5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD Module Input

CNF1 Connector Part No.: JAE Taiwan (台灣航空電子) FI-RE51S-HF-CM-R1500 or equivalent.

Pin	Name	Description	Note
1	VCC	Power input (+12V)	
2	VCC	Power input (+12V)	
3	VCC	Power input (+12V)	
4	VCC	Power input (+12V)	
5	VCC	Power input (+12V)	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	ORX0-	Odd pixel Negative LVDS differential data input. Channel 0	(5)
11	ORX0+	Odd pixel Positive LVDS differential data input. Channel 0	
12	ORX1-	Odd pixel Negative LVDS differential data input. Channel 1	
13	ORX1+	Odd pixel Positive LVDS differential data input. Channel 1	
14	ORX2-	Odd pixel Negative LVDS differential data input. Channel 2	
15	ORX2+	Odd pixel Positive LVDS differential data input. Channel 2	
16	GND	Ground	
17	OCLK-	Odd pixel Negative LVDS differential clock input	(5)
18	OCLK+	Odd pixel Positive LVDS differential clock input	
19	GND	Ground	
20	ORX3-	Odd pixel Negative LVDS differential data input. Channel 3	(5)
21	ORX3+	Odd pixel Positive LVDS differential data input. Channel 3	
22	N.C.	No Connection	(2)
23	N.C.	No Connection	
24	GND	Ground	
25	ERX0-	Even pixel Negative LVDS differential data input. Channel 0	(5)
26	ERX0+	Even pixel Positive LVDS differential data input. Channel 0	
27	ERX1-	Even pixel Negative LVDS differential data input. Channel 1	
28	ERX1+	Even pixel Positive LVDS differential data input. Channel 1	
29	ERX2-	Even pixel Negative LVDS differential data input. Channel 2	
30	ERX2+	Even pixel Positive LVDS differential data input. Channel 2	
31	GND	Ground	
32	ECLK-	Even pixel Negative LVDS differential clock input.	(5)
33	ECLK+	Even pixel Positive LVDS differential clock input.	
34	GND	Ground	
35	ERX3-	Even pixel Negative LVDS differential data input. Channel 3	(5)
36	ERX3+	Even pixel Positive LVDS differential data input. Channel 3	
37	N.C.	No Connection	(2)
38	N.C.	No Connection	
39	GND	Ground	
40	SCL	EEPROM Serial Clock	
41	N.C.	No Connection	(2)
42	N.C.	No Connection	
43	N.C.	No Connection	
44	SDA	EEPROM Serial Data	
45	SELLVDS	LVDS data format Selection	(3)(4)
46	N.C.	No Connection	(2)
47	N.C.	No Connection	
48	N.C.	No Connection	
49	N.C.	No Connection	
50	N.C.	No Connection	
51	N.C.	No Connection	

Note (1) LVDS connector pin order defined as follows



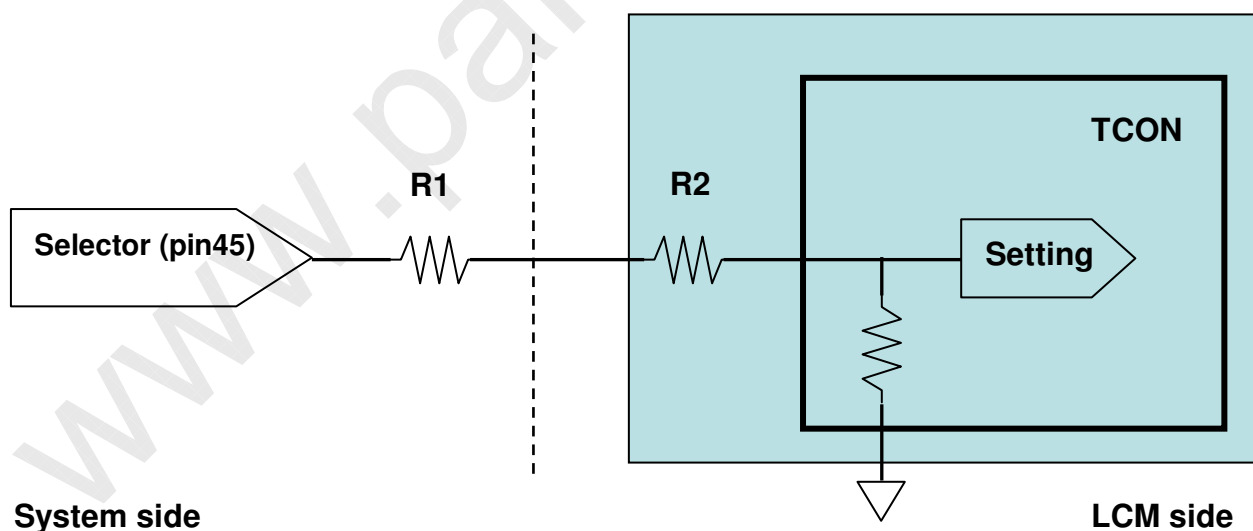
Note (2) Reserved for internal use. Please leave it open.

Note (3) Open or connect to +3.3V: VESA Format, Connect to GND: JEIDA Format.

SELLVDS	Mode
L	JEIDA
H(default)	VESA

L: Connect to GND, H: Connect to +3.3V

Note (4) LVDS signal pin connected to the LCM side has the following diagram. R1 in the system side should be less than 1K Ohm. ($R1 < 1K \text{ Ohm}$)

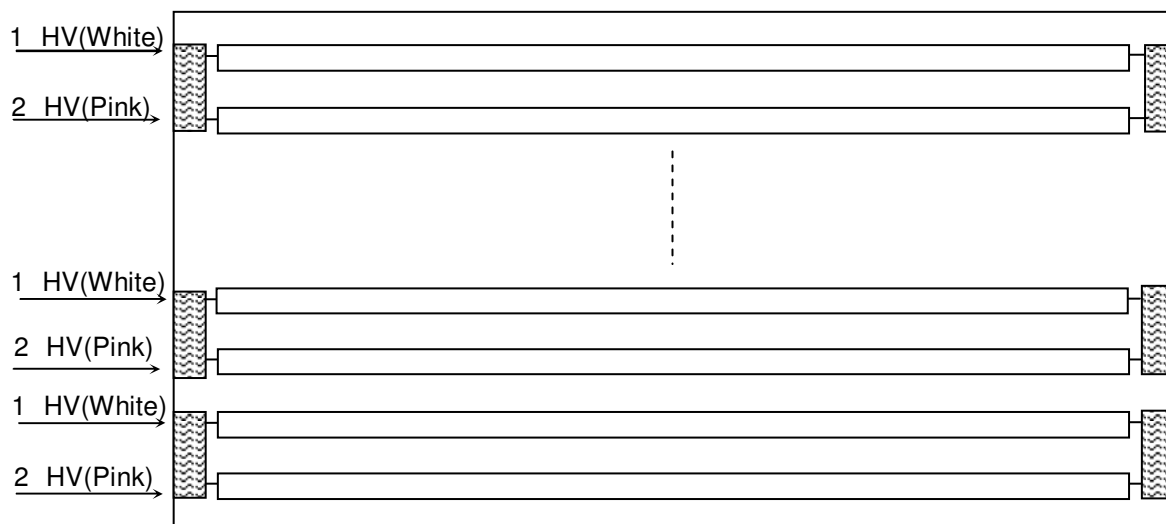


Note (5) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel

5.2 BACKLIGHT UNIT

The pin configuration for the housing and the leader wire is shown in the table below.

Pin	Name	Description	Wire Color
1	HV	High Voltage	White
2	HV	High Voltage	Pink



5.3 BALANCE BOARD UNIT

CN1(Header): 20037WR-H1224567(Yeon-Ho)

Pin №	Signal name	Feature
1	HIGH (FET)	Pulse 390V (Drive, Primary)
2	No pin	NC
3	LOW (FET)	Blocking (195Vdc, Primary)
4	No pin	NC
5	No pin	NC
6	No Pin	NC
7	No Pin	NC
8	GND	Ground (Secondary)
9	OVP	One Lamp Open Protection
10	CNT_PRT	Open Input Connector Protection (Normal 12V, Active Low)
11	12V	VCC
12	LD	All Lamp Open Protection (Normal 12V, Active Low)

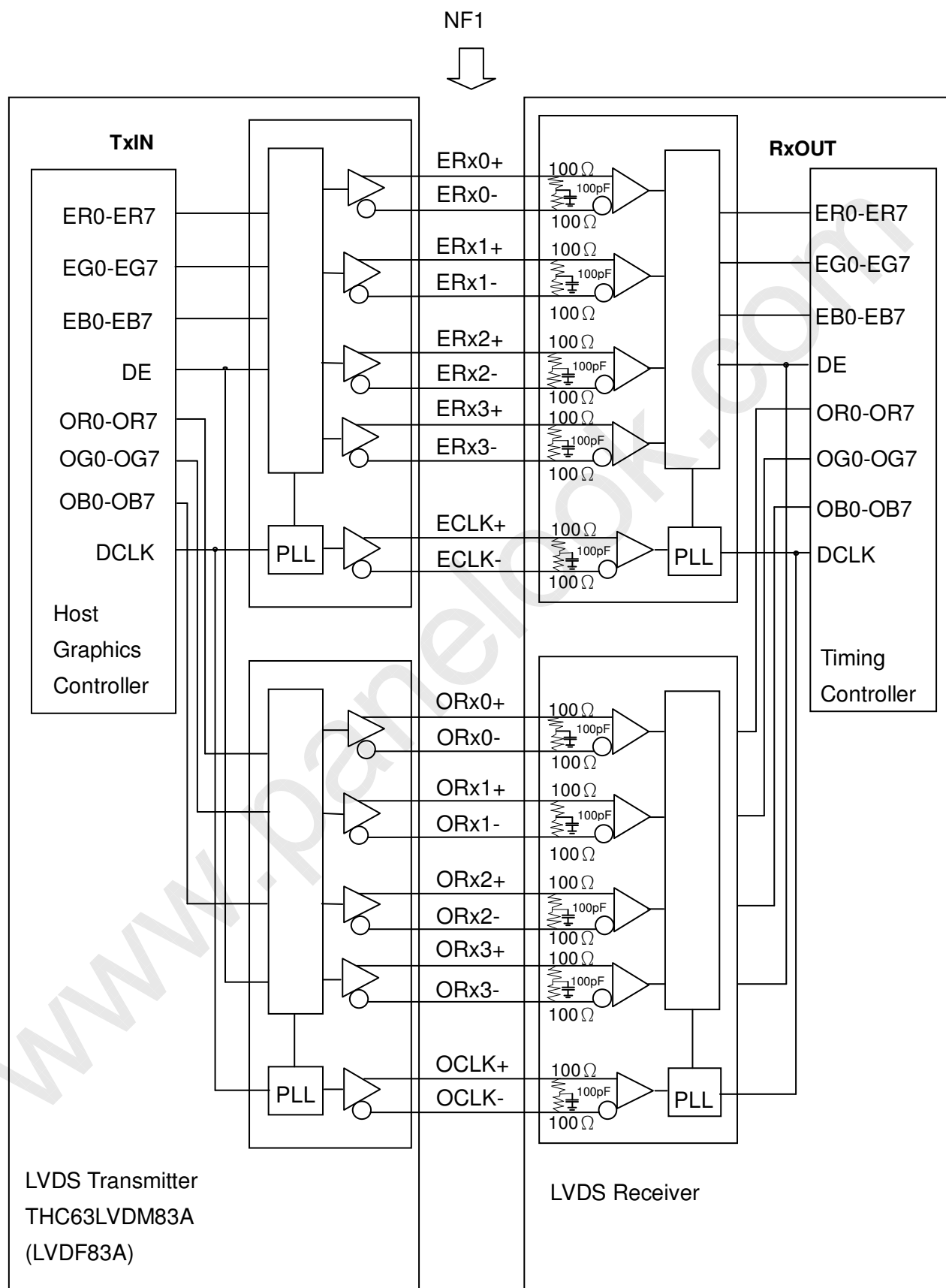


Ampower: CN2-CN7: CP042EP1MFB-LF (CviLux)

Hansol: CN11-CN16: 130001WR-02H (YEONHO)

Pin No.	Symbol	Description
1	CCFL HOT	CCFL High voltage
2	CCFL HOT	CCFL High voltage

5.4 BLOCK DIAGRAM OF INTERFACE





ER0~ER7	Even pixel R data	OR0~OR7	Odd pixel R data
EG0~EG7	Even pixel G data	OG0~OG7	Odd pixel G data
EB0~EB7	Even pixel B data	OB0~OB7	Odd pixel B data
		DE	Data enable signal
		DCLK	Data clock signal

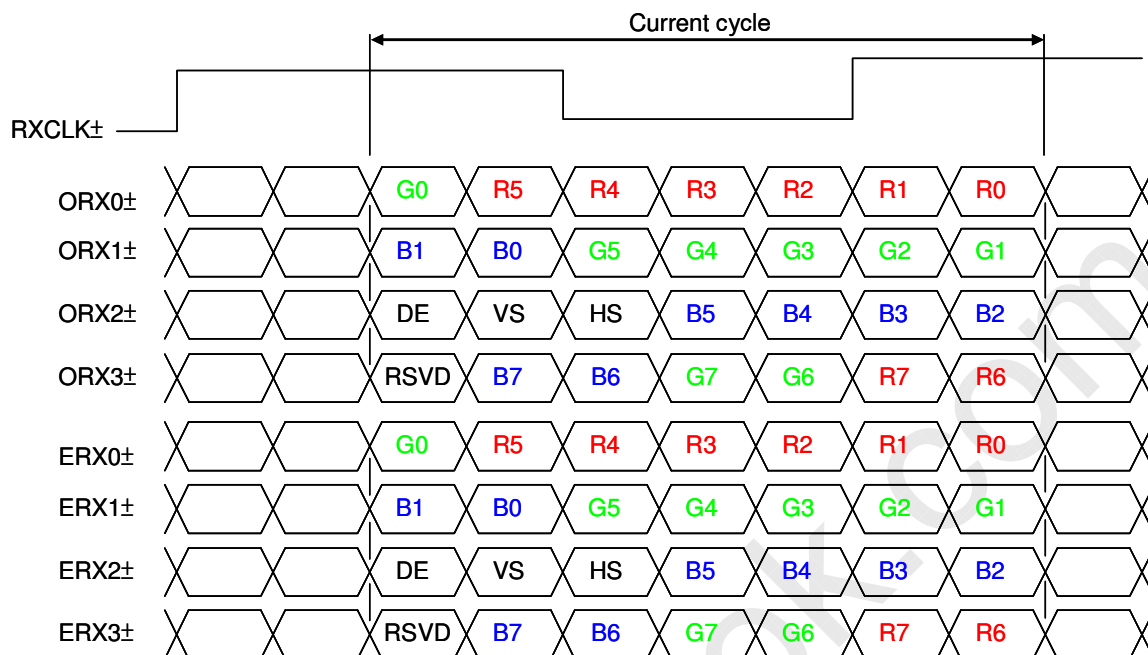
Note (1) The system must have the transmitter to drive the module.

Note (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

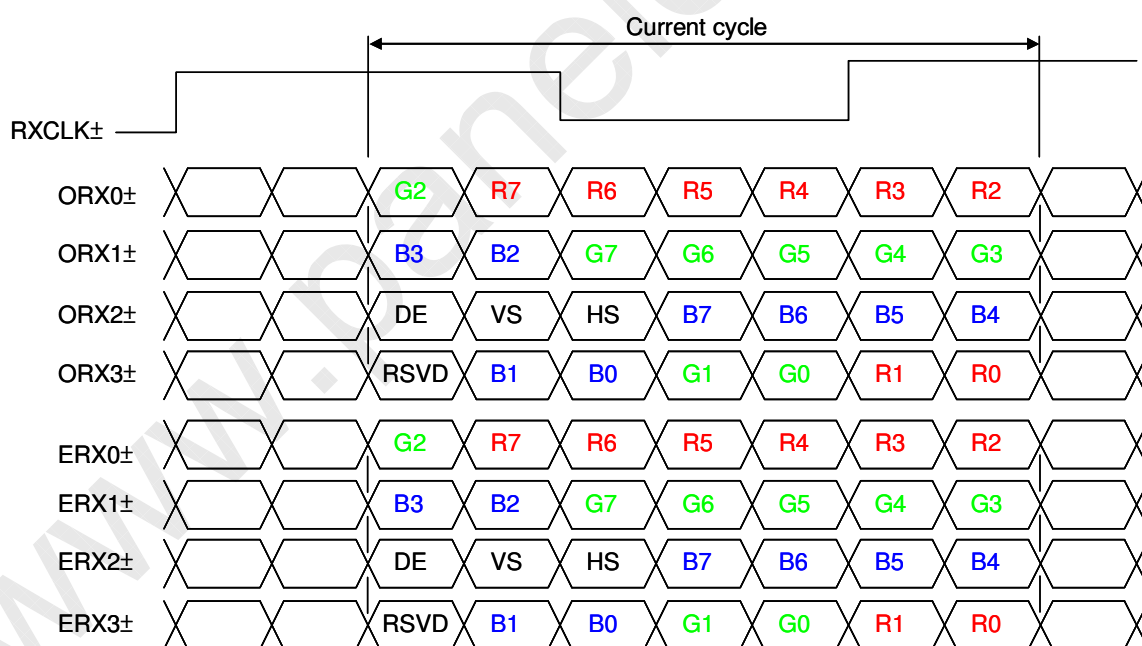
Note (3) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

5.5 LVDS INTERFACE

VESA LVDS format : (SELLVDS pin=H or open)



JEDIA LVDS format : (SELLVDS pin=L)



R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

Notes: (1) RSVD (reserved) pins on the transmitter shall be "H" or "L".

5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

**6. INTERFACE TIMING****6.1 INPUT SIGNAL TIMING SPECIFICATIONS**

(Ta = 25 ± 2 °C)

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	$F_{\text{clkin}} (=1/TC)$	60	74.25	80	MHz	(1)(5)
	Input cycle to cycle jitter	T_{rcl}	—	—	200	ps	(3)
	Spread spectrum modulation range	$F_{\text{clkin_mod}}$	$F_{\text{clkin}}-2\%$	—	$F_{\text{clkin}}+2\%$	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}	—	—	200	KHz	
LVDS Receiver Data	Setup Time	T_{lvsu}	600	—	—	ps	(5)
	Hold Time	T_{lvhd}	600	—	—	ps	
Vertical Active Display Term	Frame Rate	F_{r5}	47	50	53	Hz	(1)
		F_{r6}	57	60	62	Hz	
	Total	T_{v}	1115	1125	1135	Th	$T_{\text{v}}=T_{\text{vd}}+T_{\text{vb}}$
	Display	T_{vd}	1080	1080	1080	Th	(2)
	Blank	T_{vb}	35	45	55	Th	(2)
Horizontal Active Display Term	Total	T_{h}	1050	1100	1150	Tc	$T_{\text{h}}=T_{\text{hd}}+T_{\text{hb}}$
	Display	T_{hd}	960	960	960	Tc	(2)
	Blank	T_{hb}	90	140	190	Tc	(2)

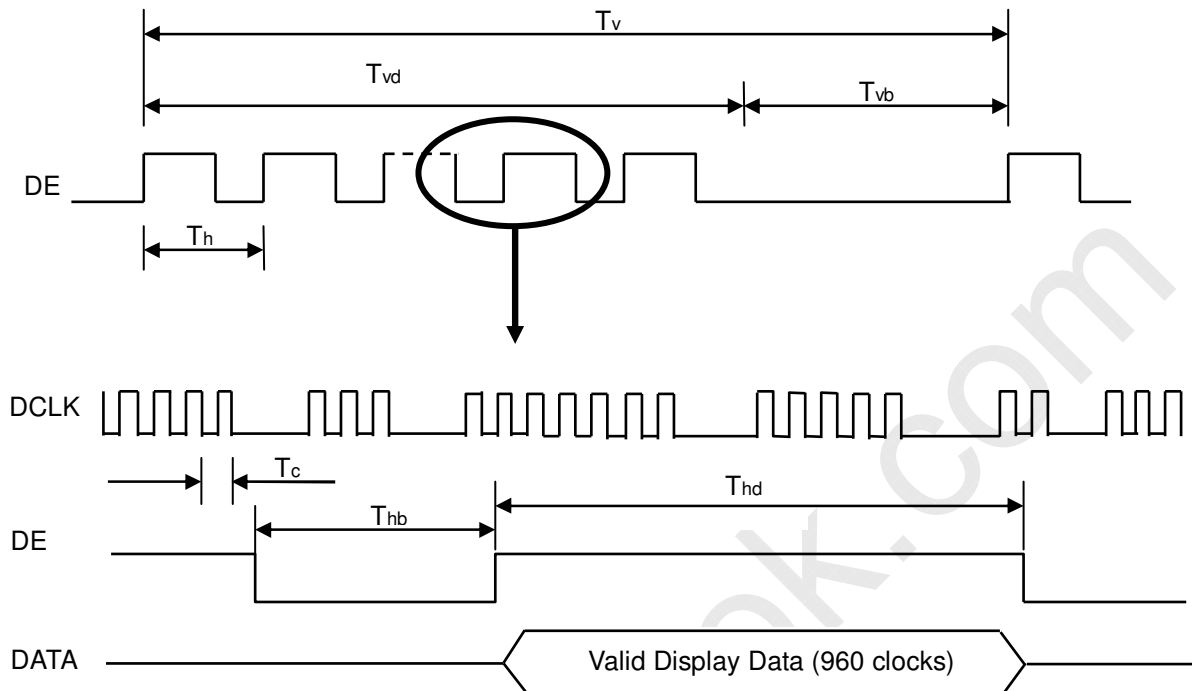
Note (1) Please make sure the range of pixel clock has follow the below equation :

$$F_{\text{clkin}}(\text{max}) \geq F_{\text{r6}} \times T_{\text{v}} \times T_{\text{h}}$$

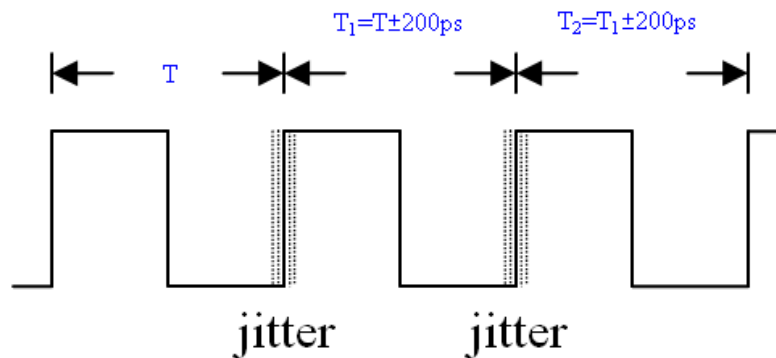
$$F_{\text{r5}} \times T_{\text{v}} \times T_{\text{h}} \geq F_{\text{clkin}}(\text{min})$$

Note (2) This module is operated in DE only mode and please follow the input signal timing diagram below :

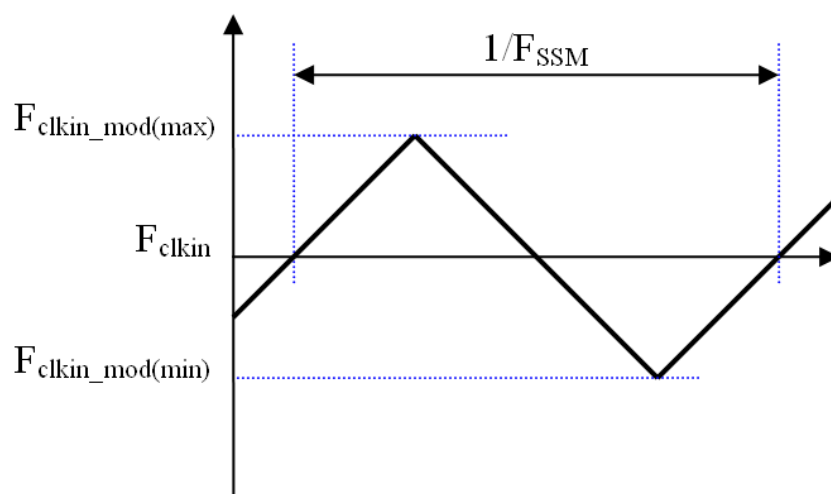
INPUT SIGNAL TIMING DIAGRAM



Note (3) The input clock cycle-to-cycle jitter is defined as below figures. $Trcl = |T_1 - T_1|$

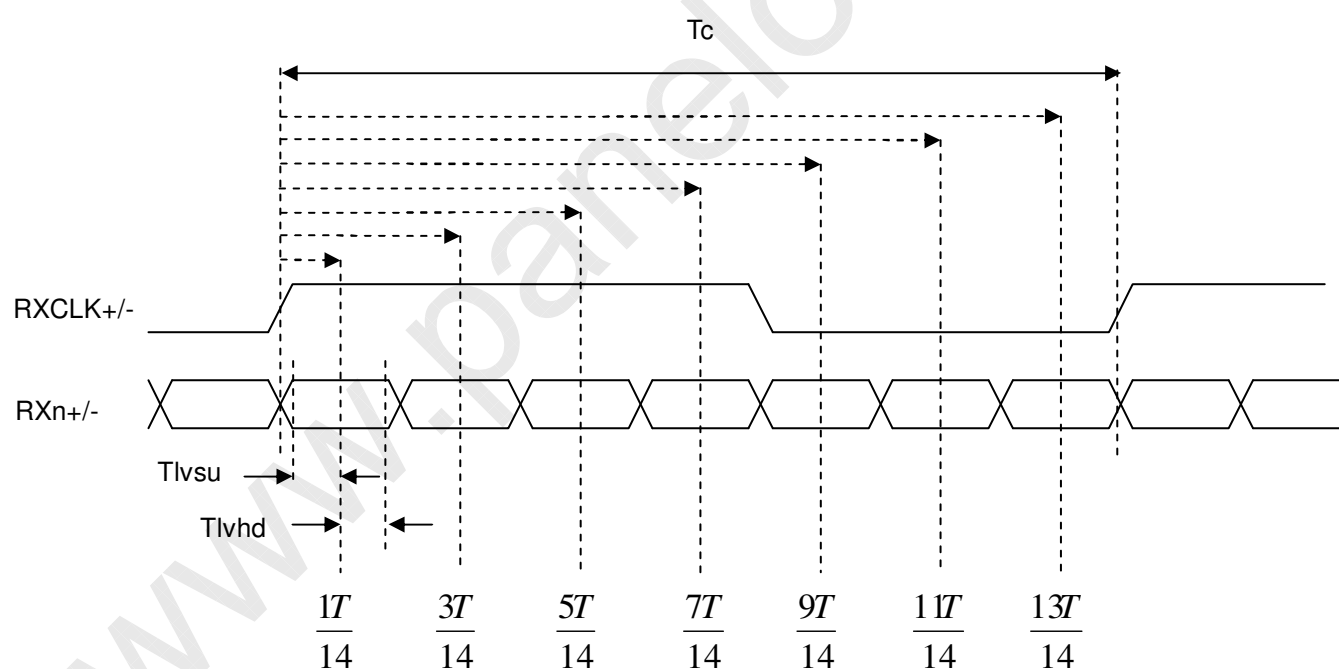


Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

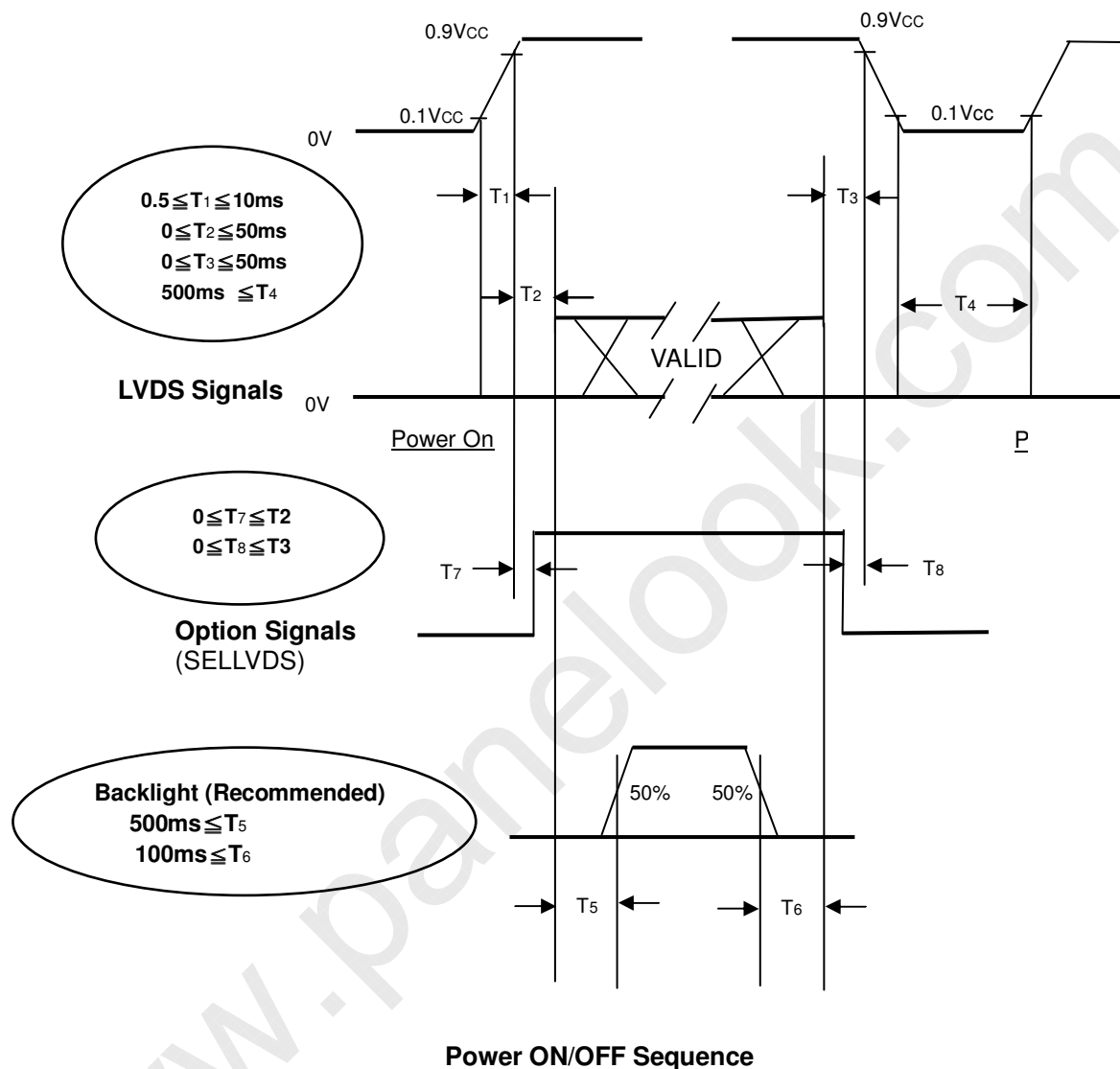
LVDS RECEIVER INTERFACE TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE

($T_a = 25 \pm 2^\circ\text{C}$)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Note (1) The supply voltage of the external system for the module input should follow the definition of V_{CC} .

Note (2) Apply the LED voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of V_{CC} is in off level, please keep the level of input signals on the low or high impedance. If $T_2 < 0$, that maybe cause electrical overstress failure.

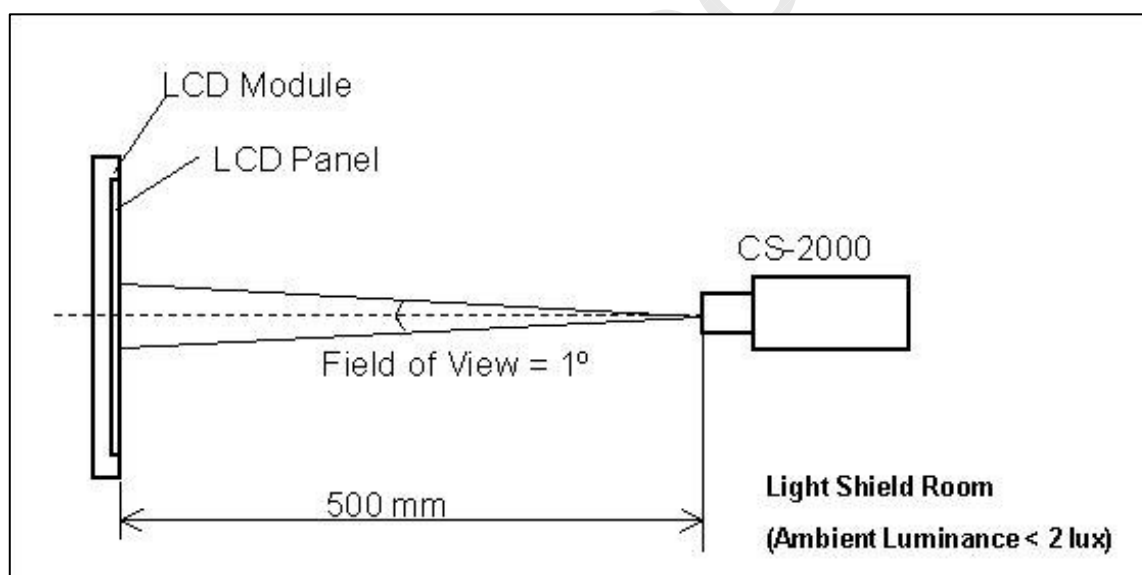
Note (4) T_4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS**7.1 TEST CONDITIONS**

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	VCC	12	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	IL	14.5	mA
Oscillating Frequency (Balance board)	FW	45±2	kHz
Vertical Frame Rate	Fr	60	Hz

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring in a windless room.



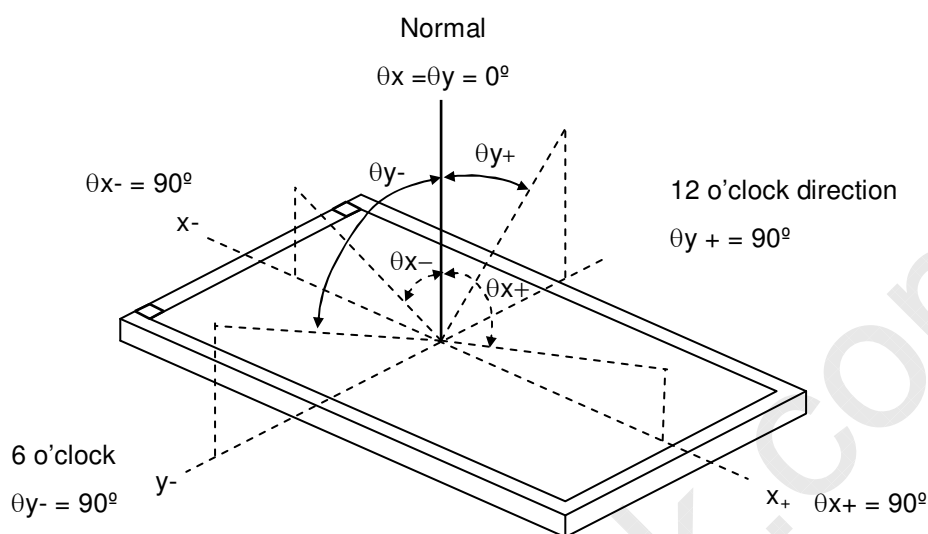
**7.2 OPTICAL SPECIFICATIONS**

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	$\theta_x=0^\circ, \theta_y=0^\circ$ Viewing angle at normal direction	4000	6000	-	-	(2)
Response Time (VA)		Gray to gray		-	8.5	17	ms	(3)
Center Luminance of White		L_c		360	500	-	cd/m ²	(4)
White Variation		δW		-	-	1.3	-	(6)
Cross Talk		CT		-	-	4	%	(5)
Color Chromaticity	Red	Rx		Typ. -0.03	0.630	Typ. +0.03	-	-
		Ry			0.320		-	
	Green	Gx			0.292		-	
		Gy			0.600		-	
	Blue	Bx			0.148		-	
		By			0.050		-	
	White	Wx			0.280		-	
		Wy			0.290		-	
	Color Gamut		C.G	-	72	-	%	NTSC
Viewing Angle	Horizontal	θ_{x+}	$CR \geq 20$ (VA) $CR \geq 10$ (TN)	80	88	-	Deg.	(1)
		θ_{x-}		80	88	-		
	Vertical	θ_{Y+}		80	88	-		
		θ_{Y-}		80	88	-		

Note (1) Definition of Viewing Angle (θ_x , θ_y) :

Viewing angles are measured by Conoscope Cono-80 (or Eldim EZ-Contrast 160R)



Note (2) Definition of Contrast Ratio (CR) :

The contrast ratio can be calculated by the following expression.

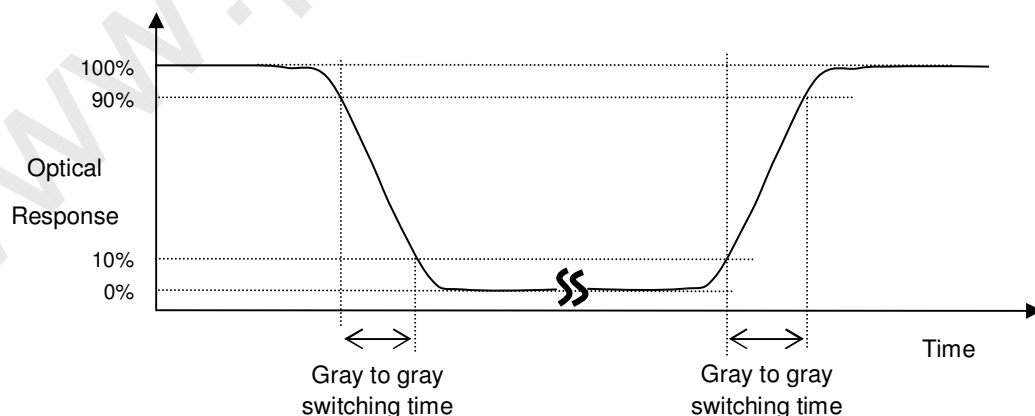
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L255}}{\text{Surface Luminance of L0}}$$

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

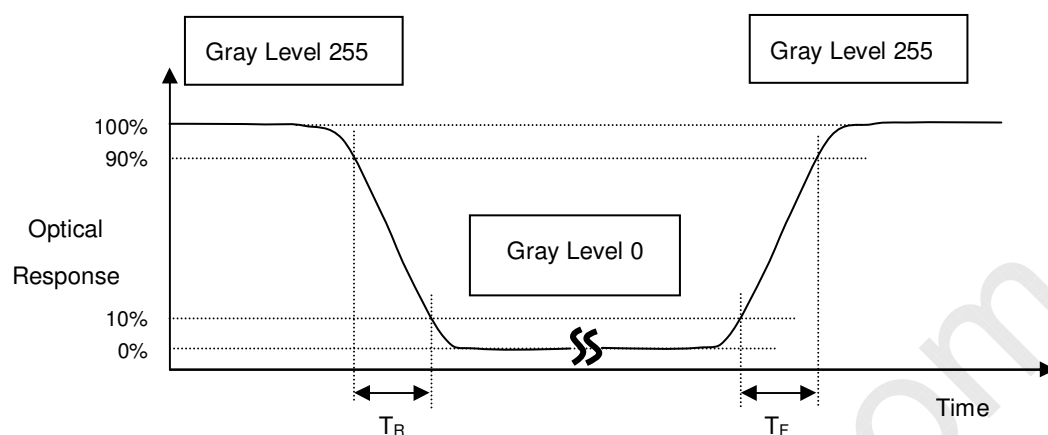
Note (3) Definition of Gray-to-Gray Switching Time:



The driving signal means the signal of gray level 0, 31, 63, 95, 127, 159, 191, 223 and 255

Gray to gray means the average switching time of gray level 0, 31, 63, 95, 127, 159, 191, 223 and 255 to each other."

Note (3) Definition of Response Time (T_R , T_F):



Note (4) Definition of Luminance of White (L_C):

Measure the luminance of gray level 255 at center point and 5 points

$L_C = L(5)$, where $L(X)$ is corresponding to the luminance of the point X at the figure in Note (6).

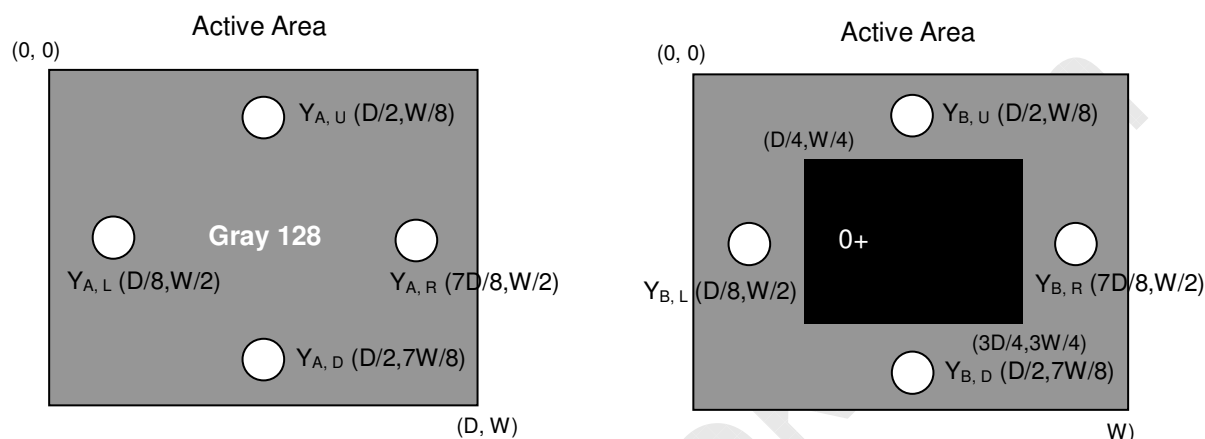
Note (5) Definition of Cross Talk (CT):

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where:

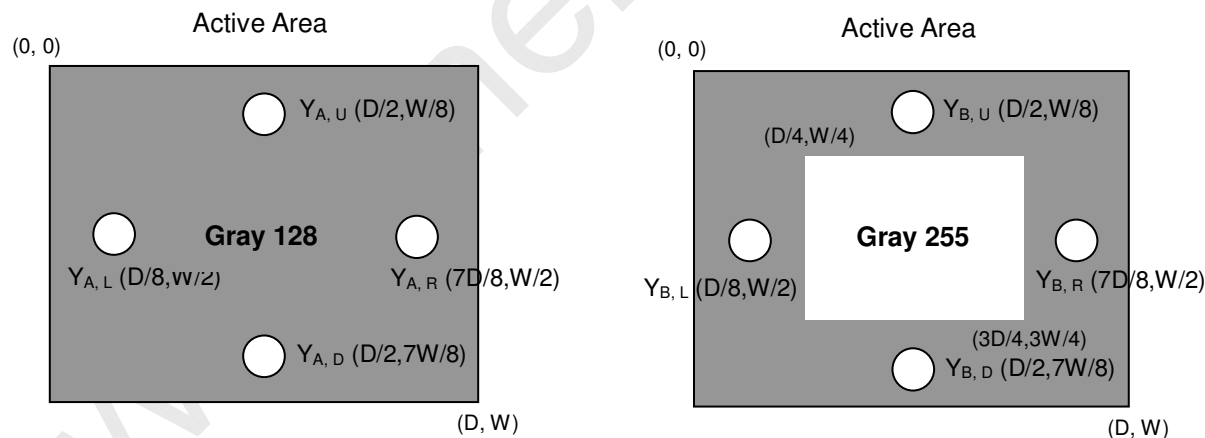
Y_A = Luminance of measured location without gray level 0 pattern (cd/m²)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m²)



Y_A = Luminance of measured location without gray level 255 pattern (cd/m²)

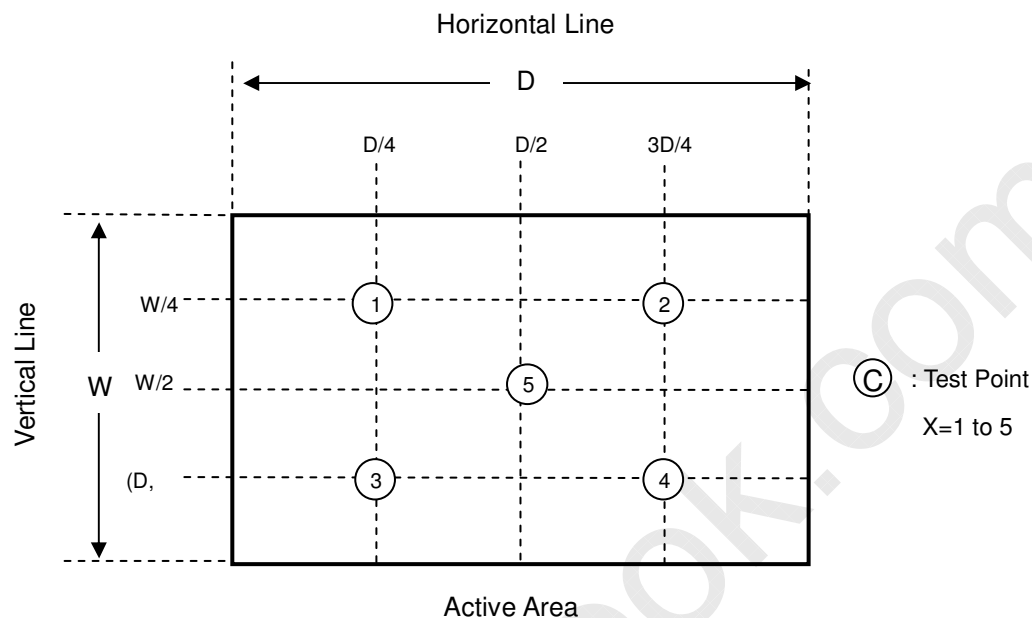
Y_B = Luminance of measured location with gray level 255 pattern (cd/m²)



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

$$\delta W = \text{Maximum } [L(1), L(2), L(3), L(4), L(5)] / \text{Minimum } [L(1), L(2), L(3), L(4), L(5)]$$



8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

- [1] Do not apply rough force such as bending or twisting to the module during assembly.
- [2] It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- [3] Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.
- [4] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMIS LSI chips.
- [5] Bezel of Set can not press or touch the panel surface. It will make light leakage or scrape.
- [6] Do not plug in or pull out the I/F connector while the module is in operation.
- [7] Do not disassemble the module.
- [8] Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- [9] Moisture can easily penetrate into LCD module and may cause the damage during operation.
- [10] When storing modules as spares for a long time, the following precaution is necessary.
 - [10.1] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35°C at normal humidity without condensation.
 - [10.2] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.
- [11] When ambient temperature is lower than 10°C, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

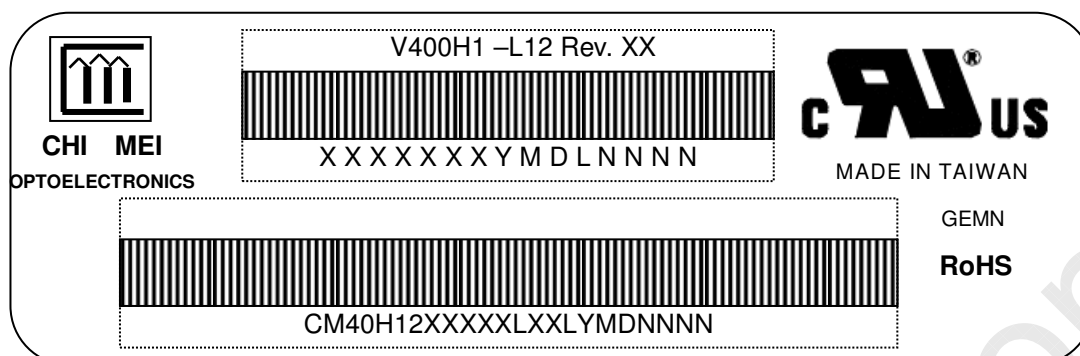
8.2 SAFETY PRECAUTIONS

- [1] The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.
- [2] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- [3] After the module's end of life, it is not harmful in case of normal operation and storage.

9. DEFINITION OF LABELS

9.1 CMI MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



- (a) Model Name: V400H1-L12
- (b) Revision: Rev. XX, for example: A0, A1... B1, B2... or C1, C2...etc.
- (c) Production Locations / Factory ID: IN TAIWAN (GEMN) or IN CHINA (LEOO or CAPG or CANO)
- (d) CMO barcode definition:

Serial ID: XX-XX-X-XX-YMD-L-NNNN

Code	Meaning	Description
XX	CMO internal use	-
XX	Revision	Cover all the change
X-XX	CMO internal use	-
YMD	Year, month, day	Year: 2001=1, 2002=2, 2003=3, 2004=4... Month: Jan. ~ Dec.=1, 2, 3, ~, 9, A, B, C Day: 1 st to 31 st =1, 2, 3, ~, 9, A, B, C, ~, W, X, Y, exclude I, O, and U
L	Product line #	Line 1=1, Line 2=2, Line 3=3, ...
NNNN	Serial number	Manufacturing sequence of product

- (e) Customer's barcode definition:

Serial ID: CM-40H12-X-X-X-XX-L-XX-L-YMD-NNNN

Code	Meaning	Description
CM	Supplier code	CMO=CM
40H12	Model number	V400H1-L12=40H12
X	Revision code	C1=1, C2=2,C9=9
X	Source driver IC code	Century=1, CLL=2, Demos=3, Epson=4, Fujitsu=5, Himax=6, Hitachi=7, Hynix=8, LDI=9, Matsushita=A, NEC=B, Novatec=C, OKI=D, Philips=E, Renasas=F, Samsung=G, Sanyo=H, Sharp=I, TI=J, Topro=K, Toshiba=L, Windbond=M
X	Gate driver IC code	OKI=D, Philips=E, Renasas=F, Samsung=G, Sanyo=H, Sharp=I, TI=J, Topro=K, Toshiba=L, Windbond=M
XX	Cell location	Tainan, Taiwan=TN
L	Cell line #	1~12=0~C
XX	Module location	Tainan, Taiwan=TN
L	Module line #	1~12=0~C
YMD	Year, month, day	Year: 2001=1, 2002=2, 2003=3, 2004=4... Month: Jan. ~ Dec.=1, 2, 3, ~, 9, A, B, C Day: 1 st to 31 st =1, 2, 3, ~, 9, A, B, C, ~, W, X, Y, exclude I, O, and U
NNNN	Serial number	By LCD supplier

10. PACKAGING**10.1 PACKAGING SPECIFICATIONS**

- (1) 5 LCD TV modules / 1 Box
- (2) Box dimensions : 1060(L)x378(W)x650(H)mm
- (3) Weight : Approx. 44Kg(5 modules per carton)
- (4) 5 LCD TV modules / 1 Box
- (5) Box dimensions : 1060(L)x378(W)x650(H)mm
- (6) Weight :
 - a. Panel module each pcs: 7.8 kg
 - b. Panel Packing Box
 - Cushion: 1.55 kg (5pcs per box)
 - Carton: 2.73 kg
 - Panel: 7.8 kg x 5pcs = 39 kg
 - Panel Packing Box Total (1 Box) =43.28 kg
 - c. Total Packing weight
 - 1) For Vessel shipment Pallet (1 Pallet =3 Box or 6 Box)
 - Pallet weight: 13.48 kg
 - Pallet Cushion: 4.65 kg or 9.3 kg
 - Pallet Packing Total = 143.32 kg or 273.16 kg
 - 2) For Air shipment Pallet (1 Pallet =6 Box)
 - Pallet weight: 13.48 kg
 - Pallet Cushion: 9.3 kg
 - Pallet Packing Total =273.16 kg

10.2 PACKAGING METHOD

Figures 10-1 and 10-2 are the packing method

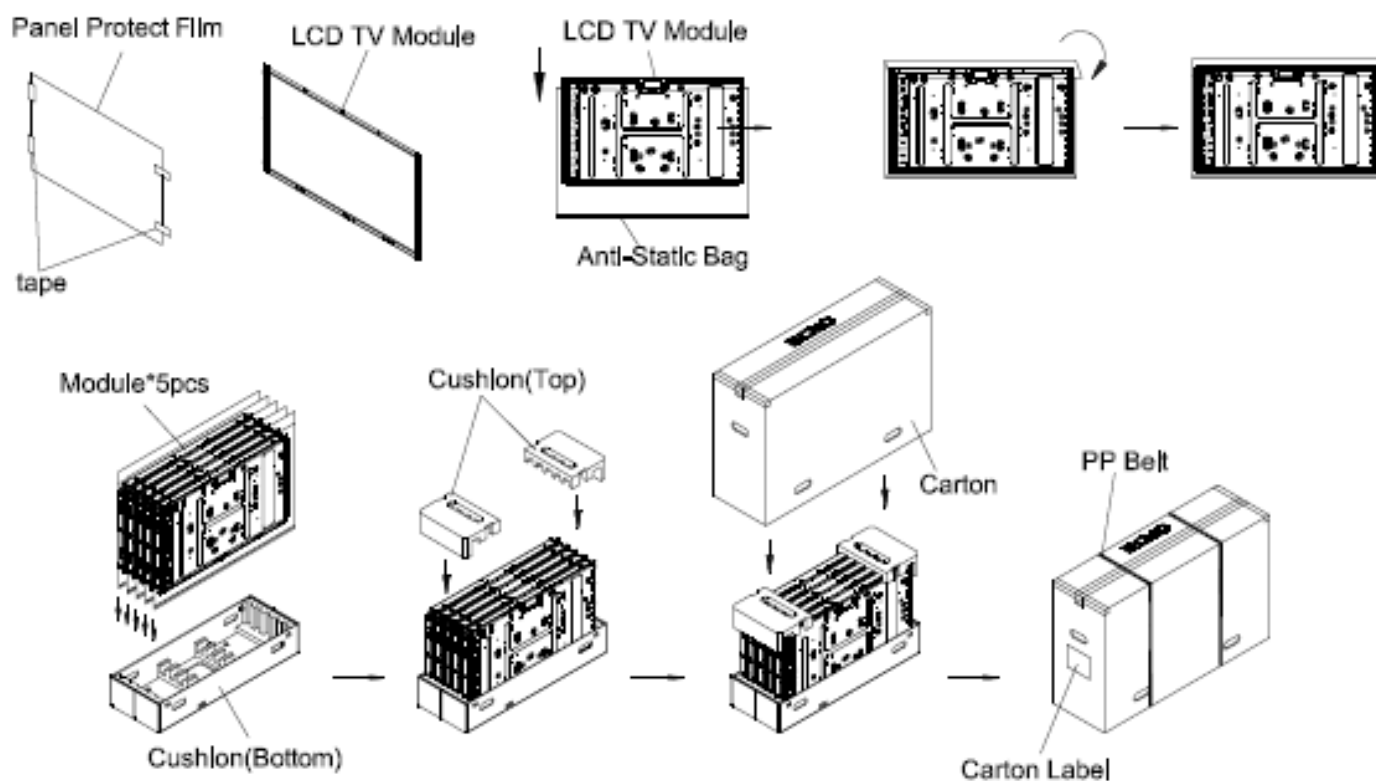
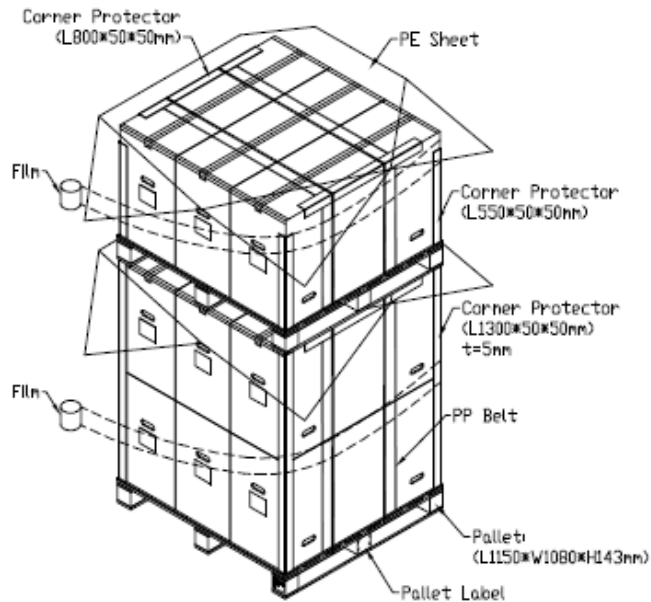


Figure 10-1 packing method

PRODUCT SPECIFICATION

Sea / Land Transportation
(40ft Container)



Air Transportation

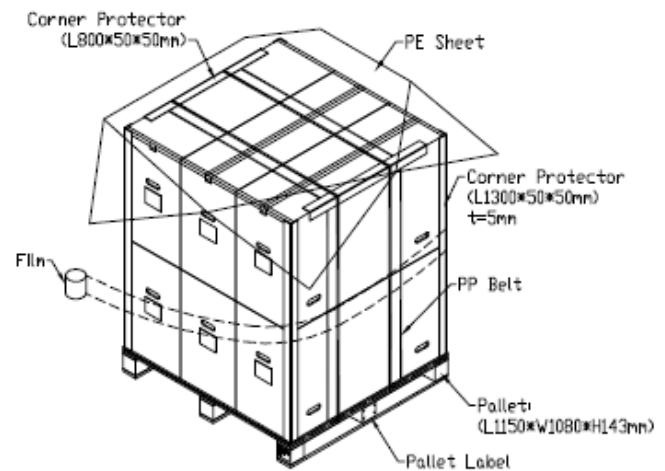
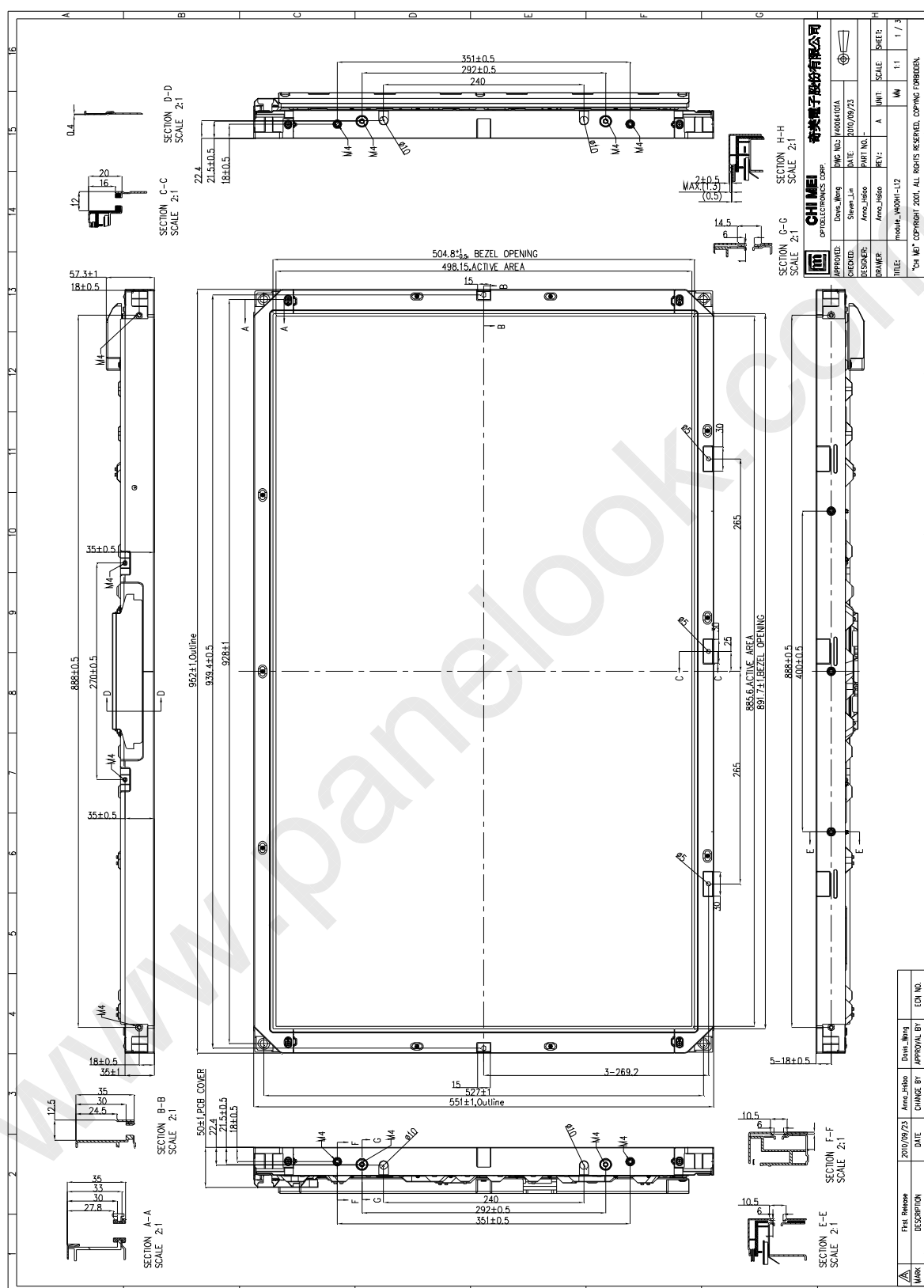
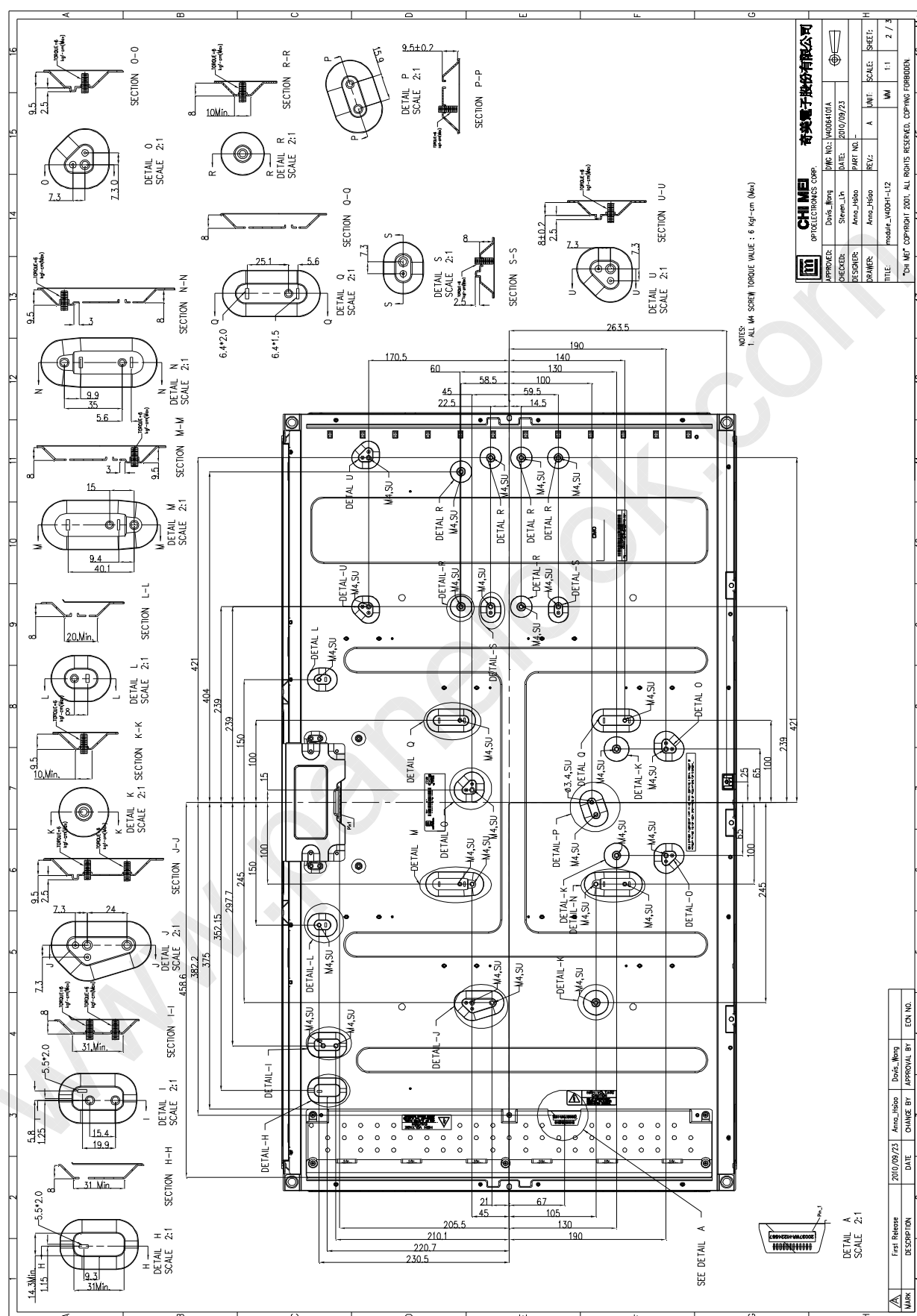


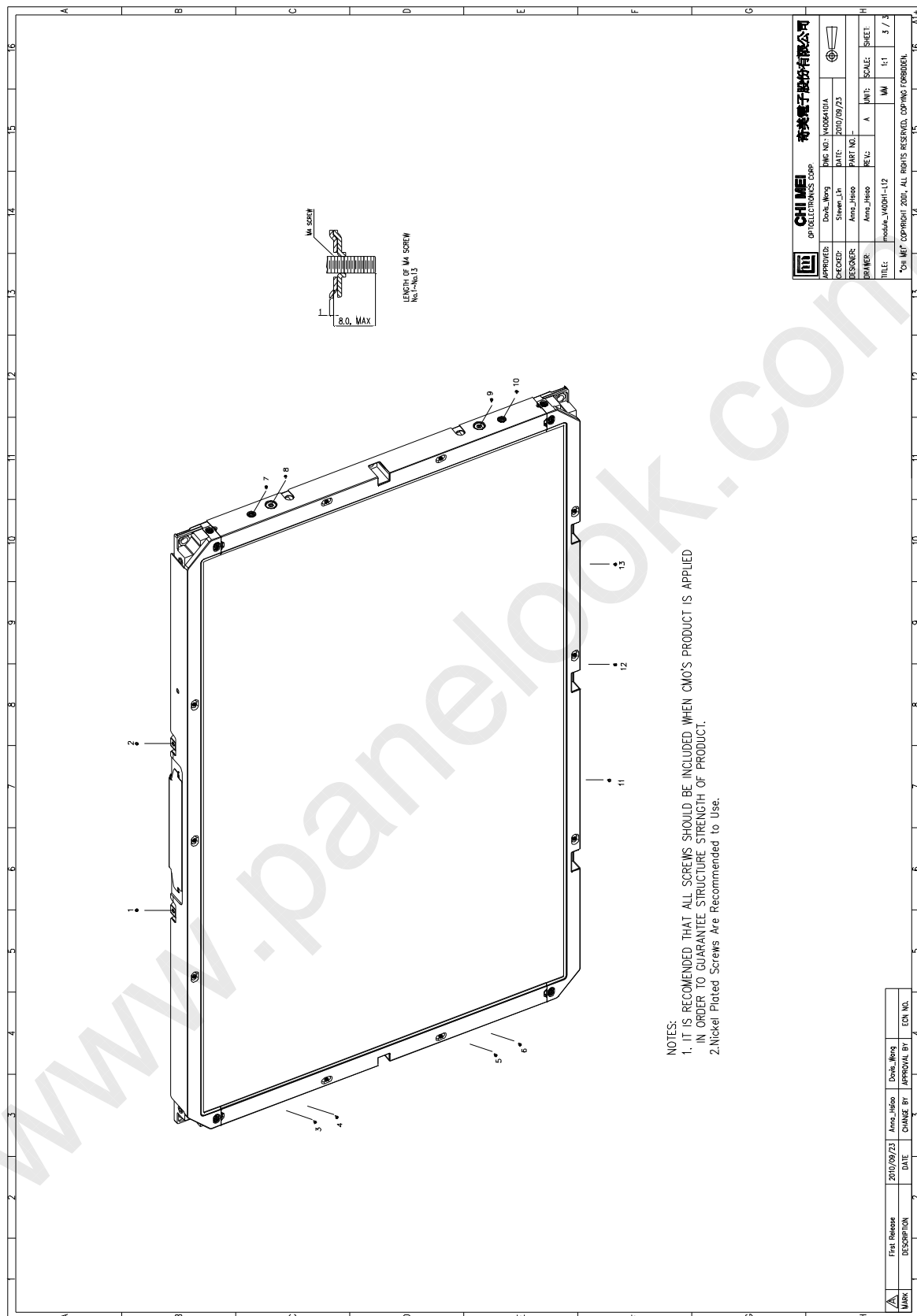
Figure 10-2 packing method

11. MECHANICAL CHARACTERISTIC



PRODUCT SPECIFICATION





CHIMEI OPTOELECTRONICS CORP.		奇美電子股份有限公司	
APPROVED:	Davis Wang	DATE:	2010/09/23
DESIGNED:	Steve Lin	PART NO.:	
DESIGNER:	Anna Jhuo	SCALE:	1:1
DATE:	2010/09/23	SHEET:	3 / 3
TITLE:	Module_V40H1-L12	UNIT:	mm
*You ME? COPYRIGHT 2004, ALL RIGHTS RESERVED. COPYING PROHIBITED.			