TFT LCD Tentative Specification

MODEL NO.: V400H1 - L02

Approved By	TVHD
	LY Chen

Reviewed By	QRA Dept.	Product Development Div.
	Tomy Chen	WT Lin

Prepared By	LCD TV Marketing and Product Management Div.	
	Denise Shieh	Gina Tsou

- CONTENTS -

REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver 0.0	May. 16,'07	All	All	Tentative Specification was first issued.
Ver 0.1	Aug. 07,'07	4	1.5	Add Min. and Max. data of Module Size.
				Modify Weight: 14500g → 13500g
		7	3.1	Modify Rush Current 4.0A → 4.5A
		8	3.2.1	Modify Lamp Voltage Typ.: 1385 → TBD
				Modify Lamp Starting Voltage Max.: 2800 → TBD(Ta = 0 ºC)
				Modify Lamp Starting Voltage Max.: 2410 → TBD(Ta = 25 ºC)
		9	3.2.2	Modify BALANCE BOARD CHARACTERISTICS
		11	4.1	Modify TFT LCD MODULE
		15	5.3	Modify CN101-CN102 (Header): SM02-BADAS-3-TB (JST) → MDF51SU-2P-13V (Hirose)
				CN103 (Header): KN30-5P-1.25H (Hirose) → KN30-7P-1.25H (Hirose)
		24	7.2	Modify Wy of Color Chromaticity: 0.290 → 0.280
		29~30	9	Modify MECHANICAL CHARACTERISTICS

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V400H1- L01 is a 40" TFT Liquid Crystal Display module with 20-CCFL Backlight unit, 2ch-LVDS interface and High color saturation NTSC 92%. This module supports 1920 x 1080 FHD format and can display true 16.7M colors (8-bit colors). The inverter module for backlight is built-in.

1.2 FEATURES

-High brightness (550 nits)
- Ultra-high contrast ratio (2000:1)
- Faster response time (Gray to gray average 6.5ms)
- High color saturation NTSC 92%
- Ultra wide viewing angle: 176(H)/176(V) (CR>20) with Super MVA technology
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Color reproduction (nature color)
- Optimized response time for both 50/60 Hz Frame rate
- Low color shift function
- RoHS compliance

1.3 APPLICATION

- TFT LCD TVs
- Multi-Media Display

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	885.6(H) x 498.15 (V) (40" diagonal)	mm	(1)
Bezel Opening Area	891.7 (H) x 504.2 (V)	mm	
Driver Element	a-si TFT active matrix	-	
Pixel Number	1920 x R.G.B. x 1080	pixel	
Pixel Pitch (Sub Pixel)	0.1730 (H) x 0.5190 (V)	mm	
Pixel Arrangement	RGB vertical stripe	-	
Display Colors	16.7M	color	
Display Operation Mode	Transmissive mode / Normally black	-	
Surface Treatment	Glare coating (Haze 25%),Hard coating (3H)	-	

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	951	952	953	mm	(1)
	Vertical(V)	550	551	552	mm	(1)
	Depth(D)	45.6	46.6	47.6	mm	To PCB cover
	Depth(D)	52.2	53.2	54.2	mm	To inverter cover
Weight		-	10350	-	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	-	50	G	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

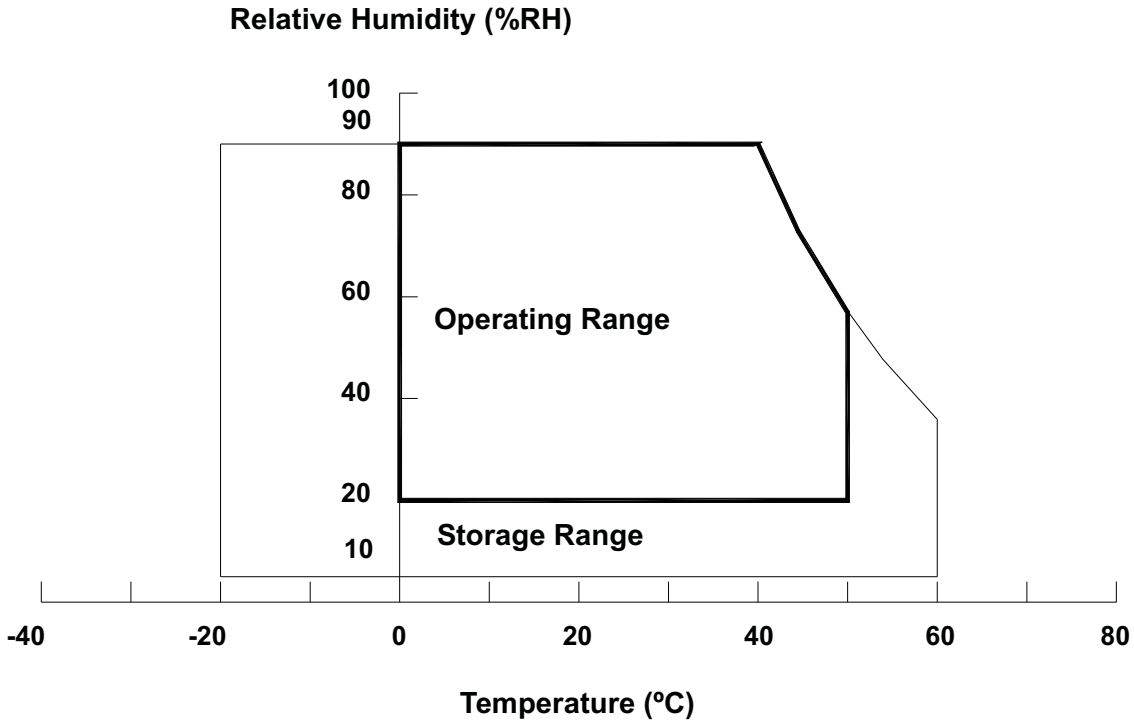
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 60 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 60 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

(a) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃ at normal humidity without condensation.

(b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	Vcc	-0.3	13.5	V	(1)
Input Signal Voltage	V_{IN}	-0.3	3.6	V	

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	Vcc	-0.3	13.5	V	(1)
Input Signal Voltage	V_{IN}	-0.3	3.6	V	

2.3.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V_W	—	3000	V_{RMS}	

Note (1) No moisture condensation or freezing.

3. ELECTRICAL CHARACTERISTICS

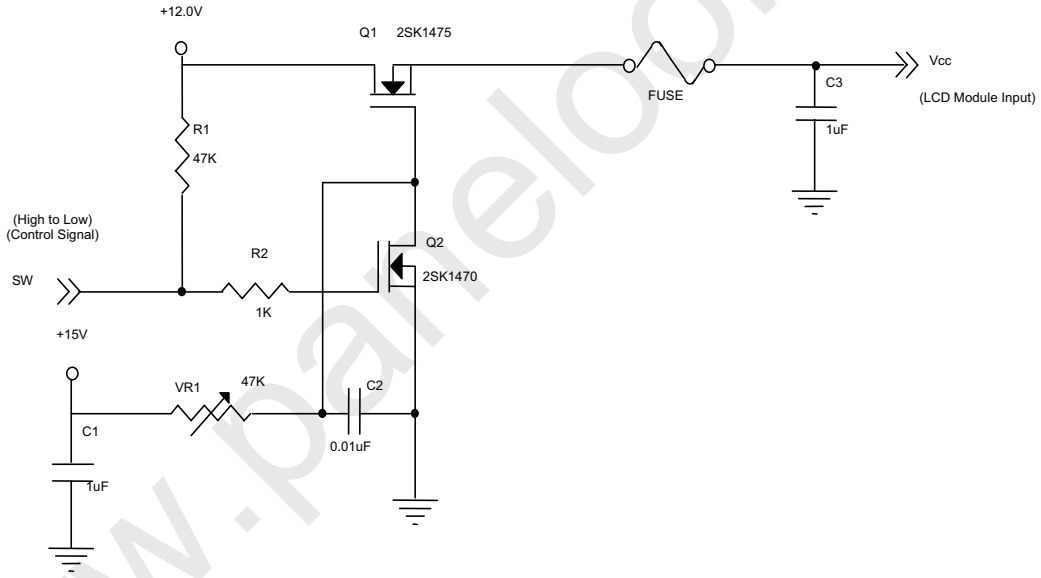
3.1 TFT LCD MODULE

Ta = 25 ± 2 ºC

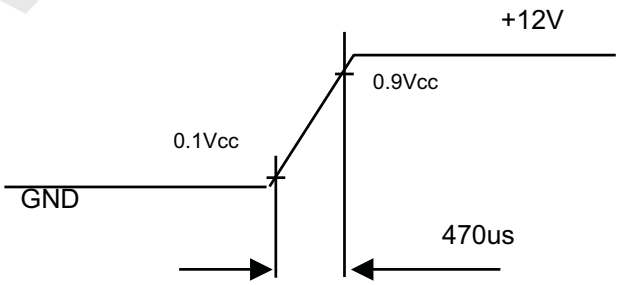
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12.0	13.2	V	(1)
Power Supply Ripple Voltage		V_{RP}	-	-	350	mV	
Rush Current		I_{RUSH}	-	-	4.5	A	(2)
Power Supply Current	White	I_{CC}	-	1.2	1.5	A	(3)
	Black		-	0.6	0.7	A	
	Vertical Stripe		-	1.0	1.2	A	
LVDS Interface	Differential Input High Threshold Voltage	V_{LVTH}	-	-	+100	mV	
	Differential Input Low Threshold Voltage	V_{LVTL}	-100	-	-	mV	
	Common Input Voltage	V_{LVC}	1.125	1.25	1.375	V	
	Terminating Resistor	R_T	-	100	-	ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	-	0.7	V	

Note (1) The module should be always operated within above ranges.

Note (2) Measurement Conditions:



Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

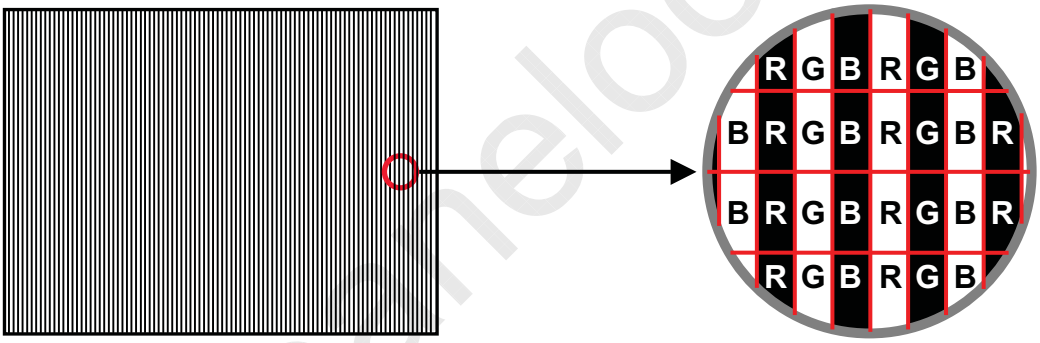
a. White Pattern

Active Area

b. Black Pattern

Active Area

c. Vertical Stripe Pattern



Active Area

3.2 BACKLIGHT UNIT

3.2.1 CCFL (Cold Cathode Fluorescent Lamp) CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Voltage	V_W	-	TBD	-	V_{RMS}	Ih = 8.5mA
Lamp Current	I_L	8.2	8.5	8.8	mA_{RMS}	(1)
Lamp Starting Voltage	V_S	-	-	TBD	V_{RMS}	(2), Ta = 0 ºC
		-	-	TBD	V_{RMS}	(2), Ta = 25 ºC
Operating Frequency	F_O	40	-	70	KHz	(3)
Lamp Life Time	L_{BL}	50,000	-	-	Hrs	(4)

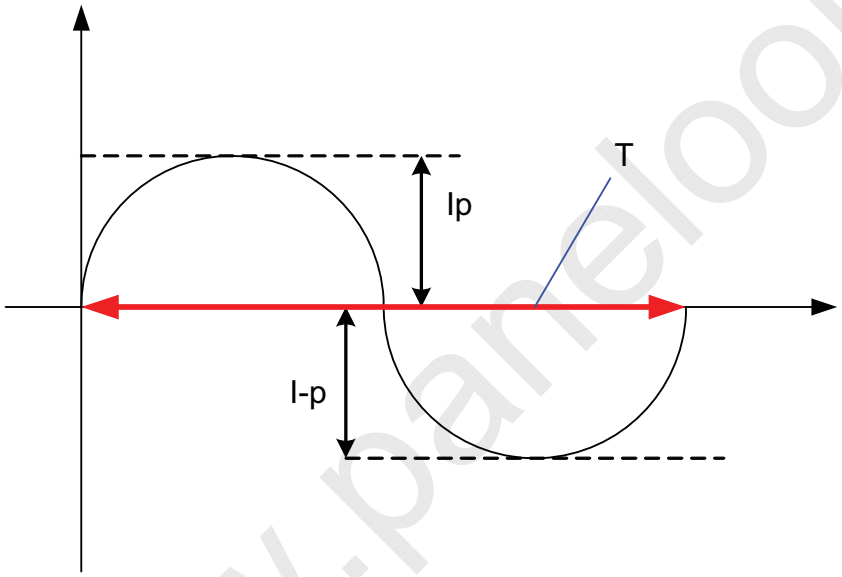
3.2.2 BALANCE BOARD CHARACTERISTICS (Ta = 25 ± 2 ºC)

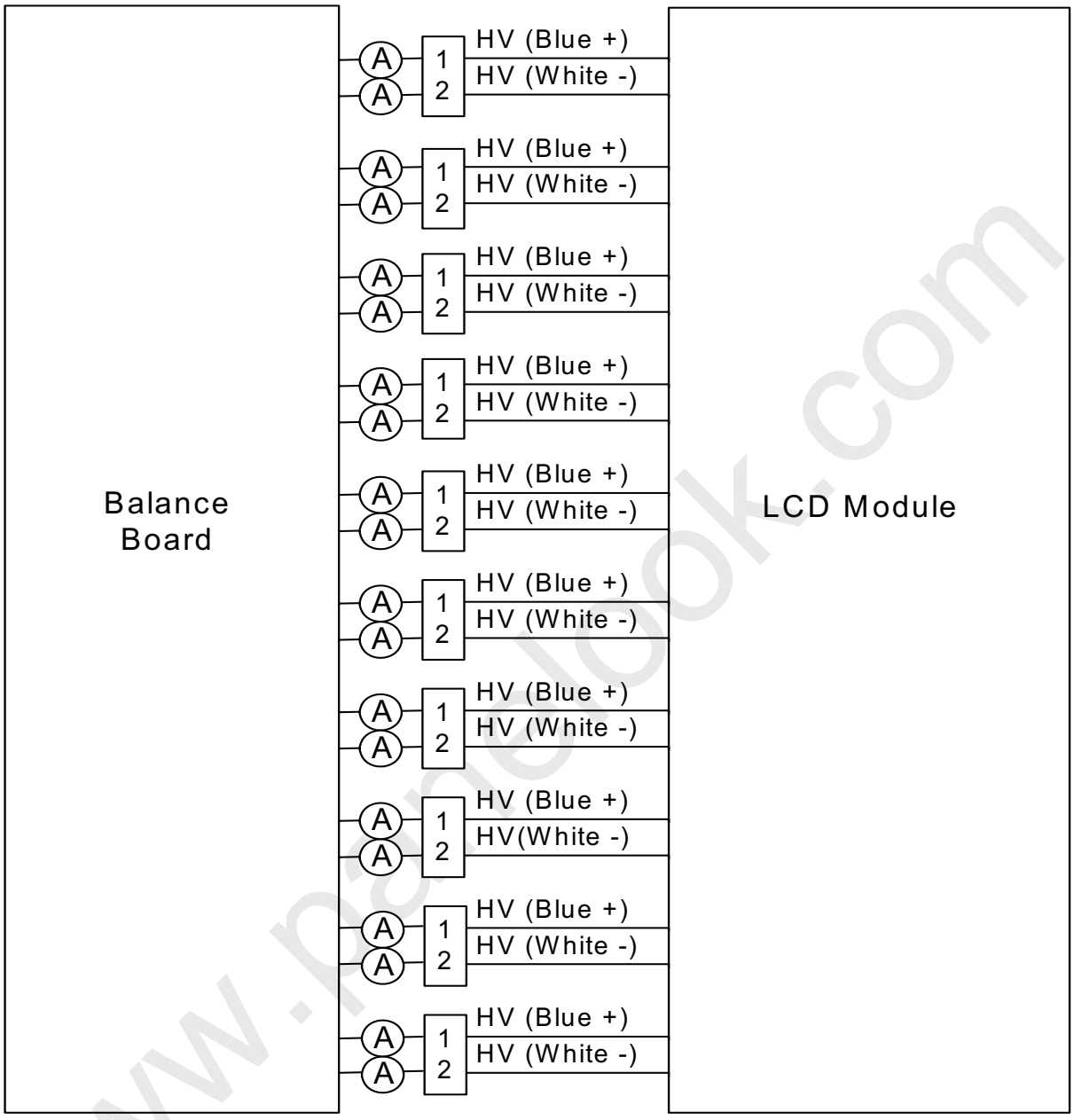
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Input High Voltage		$V_{(HV1/HV2}$	-	1200	-	V	(2)
Input Current		$I_{BL(HV)}$		TBD		mArms	No Dimming
Oscillating Frequency		F_W	54.0	55.5	57.0	kHz	
Individual Lamp Current		I_L	8.2	8.5	8.8	mA	H.V
Lamp Detection	High (LD)	LD	11.5		12	V	Normal Operation
	Low (LD)	LD			1.5	V	Lamp Connector Open
Dimming frequency		F_B	120	160	180	Hz	
Minimum Duty Ratio		D_{MIN}	-	20	-	%	

Note (1) Lamp current is measured by utilizing high frequency current meters as shown below:

Note (2) Input High Voltage Hv based on spec. +-7% tolerance.

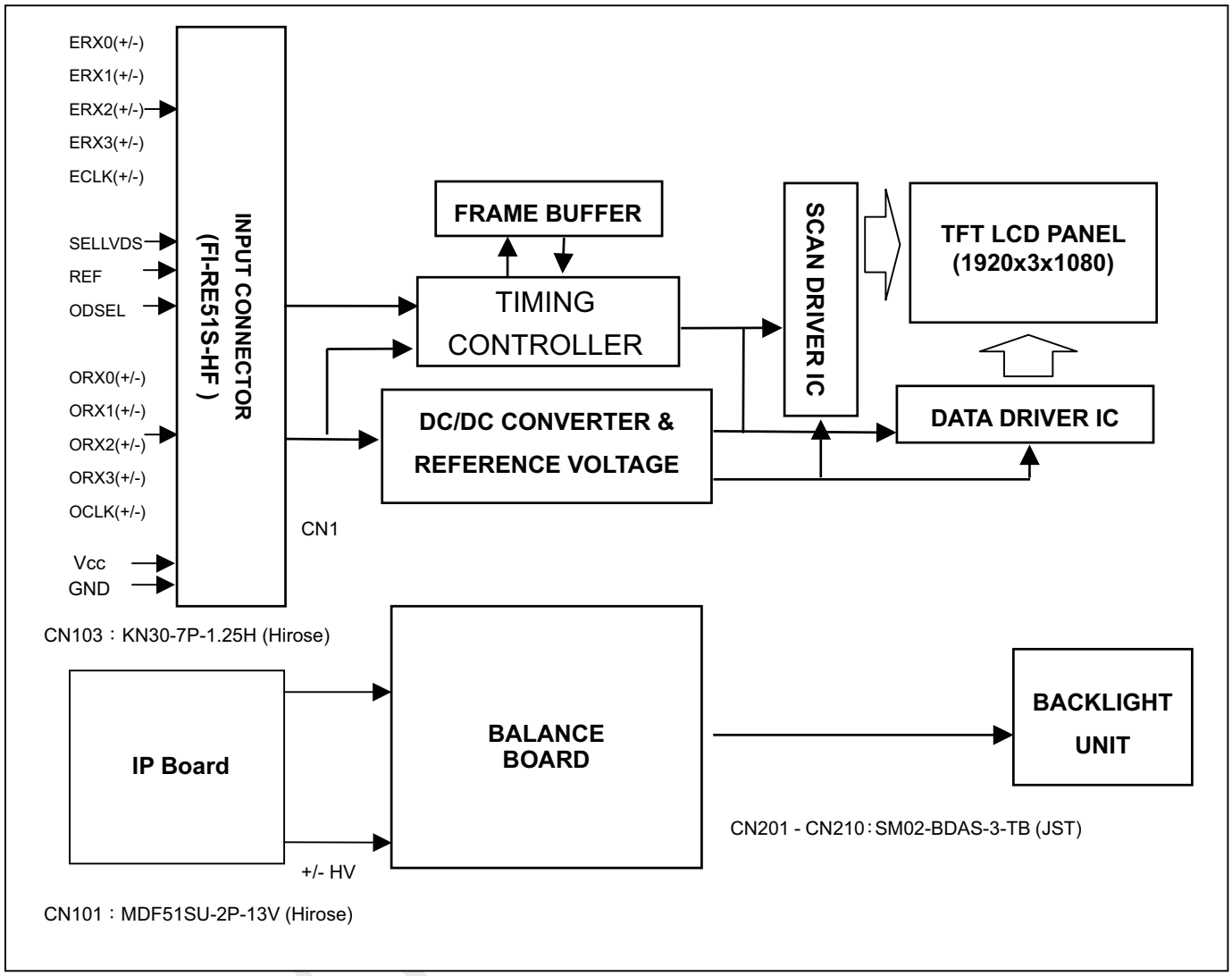
Note (3) Asymmetric ratio must be from 90% to 110% ($0.9<Ip/ I_{rms@T/2X\sqrt{2}}<1.1$)





4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



5. INTERFACE PIN CONNECTION

5.1 TFT LCD MODULE

CNF1 Connector Pin Assignment

Pin	Name	Description	Note
1	VCC	+12V power supply	
2	VCC	+12V power supply	
3	VCC	+12V power supply	
4	VCC	+12V power supply	
5	VCC	+12V power supply	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	ORX0-	Odd pixel, Negative LVDS differential data input. Channel 0	
11	ORX0+	Odd pixel, Positive LVDS differential data input. Channel 0	
12	ORX1-	Odd pixel, Negative LVDS differential data input. Channel 1	
13	ORX1+	Odd pixel, Positive LVDS differential data input. Channel 1	
14	ORX2-	Odd pixel, Negative LVDS differential data input. Channel 2	
15	ORX2+	Odd pixel, Positive LVDS differential data input. Channel 2	
16	GND	Ground	
17	OCLK-	Odd pixel, Negative LVDS differential clock input	
18	OCLK+	Odd pixel, Positive LVDS differential clock input.	
19	GND	Ground	
20	ORX3-	Odd pixel, Negative LVDS differential data input. Channel 3	
21	ORX3+	Odd pixel, Positive LVDS differential data input. Channel 3	
22	N.C.	No Connection	(1)
23	N.C.	No Connection	
24	GND	Ground	
25	ERX0-	Even pixel Negative LVDS differential data input. Channel 0	
26	ERX0+	Even pixel Positive LVDS differential data input. Channel 0	
27	ERX1-	Even pixel Negative LVDS differential data input. Channel 1	
28	ERX1+	Even pixel Positive LVDS differential data input. Channel 1	
29	ERX2-	Even pixel Negative LVDS differential data input. Channel 2	
30	ERX2+	Even pixel Positive LVDS differential data input. Channel 2	
31	GND	Ground	
32	ECLK-	Even pixel Negative LVDS differential clock input.	
33	ECLK+	Even pixel Positive LVDS differential clock input.	

34	GND	Ground	
35	ERX3-	Even pixel Negative LVDS differential data input. Channel 3	
36	ERX3+	Even pixel Positive LVDS differential data input. Channel 3	
37	N.C.	No Connection	(1)
38	N.C.	No Connection	
39	GND	Ground	
40	ODSEL	Overdrive Lookup Table Selection	(3)
41	N.C.	No Connection	(1)
42	N.C.	No Connection	(1)
43	N.C.	No Connection	(1)
44	N.C.	No Connection	(1)
45	SELLVDS	LVDS Data Format Selection	(2)
46	N.C.	No Connection	(1)
47	N.C.	No Connection	
48	N.C.	No Connection	
49	N.C.	No Connection	(1)
50	N.C.	No Connection	
51	N.C.	No Connection	

Note (1) Reserved for internal use. Please leave it open.

Note (2) Low : JEIDA LVDS Format (default), High : VESA Format.

Note (3) Overdrive lookup table selection. The overdrive lookup table should be selected in accordance to the frame rate to optimize image quality.

ODSEL	Note
L	Lookup table was optimized for 60 Hz frame rate.
H	Lookup table was optimized for 50 Hz frame rate.

Note (4) Low =Open or Connect to GND, High = Connect to +3.3V

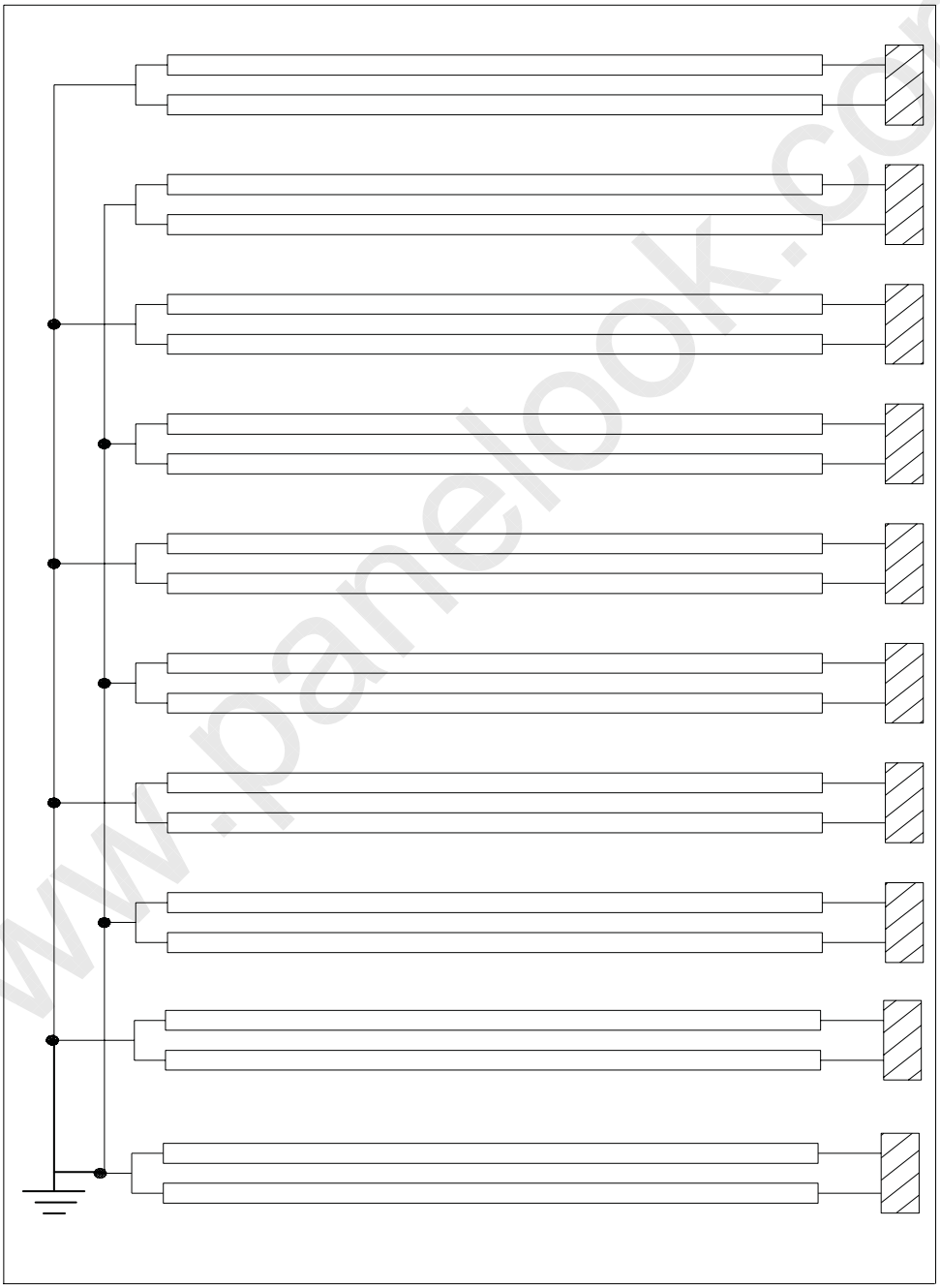
5.2 BACKLIGHT UNIT

The pin configuration for the housing and leader wire is shown in the table below.

CN201-CN210 (Housing): BDAMR-02VAS-3 (JST)

Pin No.	Symbol	Description	Wire Color
1	HV	High Voltage	Blue
2	HV	High Voltage	White

Note (1) The backlight interface housing for high voltage side is a model BDAMR-02VAS-3 (JST), manufactured by JST. The mating header on inverter part number is SM02-BDAS-3-TB (JST).



5.3 BALANCE BOARD UNIT

CN101-CN102 (Header): MDF51SU-2P-13V (Hirose)

Pin No.	Symbol	Description
1	HV-	CCFL high voltage
2	HV+	CCFL high voltage

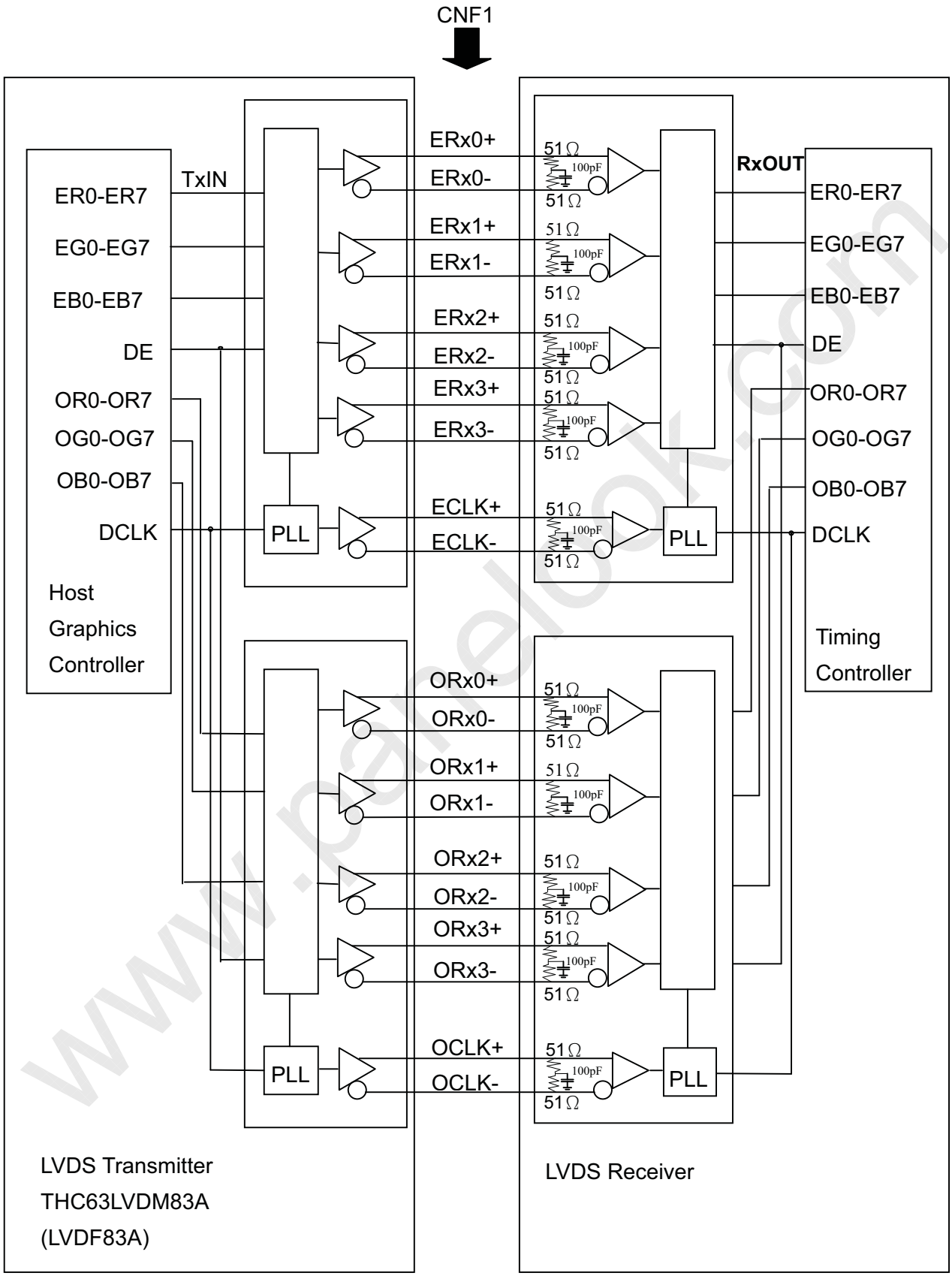
CN201-CN210 (Header): SM02-BADAS-3-TB(JST)

Pin No.	Symbol	Description
1	HV+	CCFL high voltage
2	HV-	CCFL high voltage

CN103 (Header): KN30-7P-1.25H (Hirose)

Pin No.	Symbol	Description
1	VCC	Power Supply for Protection Circuit
2	FB	Lamp Current Detected Voltage
3	GND	Signal Ground
4	NC	Signal Ground
5	LD	CCFL Connector Open & Non-lighting signal

5.4 BLOCK DIAGRAM OF INTERFACE



ER0~ER7 : Even pixel R data
EG0~EG7 : Even pixel G data
EB0~EB7 : Even pixel B data
OR0~OR7: Odd pixel R data
OG0~OG7: Odd pixel G data
OB0~OB7 : Odd pixel B data
DE : Data enable signal
DCLK : Data clock signal

Note (1) The system must have the transmitter to drive the module.

Note (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

Note (3) Two pixel data send into the module for every clock cycle. The first pixel of the frame is even pixel and the second pixel is odd pixel.

5.5 LVDS INTERFACE

	SIGNAL		TRANSMITTER THC63LVDM83A		INTERFACE CONNECTOR		RECEIVER THC63LVDF84A		TFT CONTROL INPUT	
	SELLVDS=H	SELLVDS= L or OPEN	PIN	INPUT	Host	TFT-LCD	PIN	OUTPUT	SELLVDS=H	SELLVDS= L or OPEN
	R0	R2	51	TxIN0			27	Rx OUT0	R0	R2
	R1	R3	52	TxIN1			29	Rx OUT1	R1	R3
	R2	R4	54	TxIN2	TA OUT0+	Rx 0+	30	Rx OUT2	R2	R4
	R3	R5	55	TxIN3			32	Rx OUT3	R3	R5
	R4	R6	56	TxIN4			33	Rx OUT4	R4	R6
	R5	R7	3	TxIN6	TA OUT0-	Rx 0-	35	Rx OUT6	R5	R7
	G0	G2	4	TxIN7			37	Rx OUT7	G0	G2
	G1	G3	6	TxIN8			38	Rx OUT8	G1	G3
	G2	G4	7	TxIN9			39	Rx OUT9	G2	G4
	G3	G5	11	TxIN12	TA OUT1+	Rx 1+	43	Rx OUT12	G3	G5
	G4	G6	12	TxIN13			45	Rx OUT13	G4	G6
	G5	G7	14	TxIN14			46	Rx OUT14	G5	G7
	B0	B2	15	TxIN15	TA OUT1-	Rx 1-	47	Rx OUT15	B0	B2
	B1	B3	19	TxIN18			51	Rx OUT18	B1	B3
	B2	B4	20	TxIN19			53	Rx OUT19	B2	B4
24	B3	B5	22	TxIN20			54	Rx OUT20	B3	B5
bit	B4	B6	23	TxIN21	TA OUT2+	Rx 2+	55	Rx OUT21	B4	B6
	B5	B7	24	TxIN22			1	Rx OUT22	B5	B7
	DE	DE	30	TxIN26			6	Rx OUT26	DE	DE
	R6	R0	50	TxIN27	TA OUT2-	Rx 2-	7	Rx OUT27	R6	R0
	R7	R1	2	TxIN5			34	Rx OUT5	R7	R1
	G6	G0	8	TxIN10			41	Rx OUT10	G6	G0
	G7	G1	10	TxIN11			42	Rx OUT11	G7	G1
	B6	B0	16	TxIN16	TA OUT3+	Rx 3+	49	Rx OUT16	B6	B0
	B7	B1	18	TxIN17			50	Rx OUT17	B7	B1
	RSVD 1	RSVD 1	25	TxIN23			2	Rx OUT23	NC	NC
	RSVD 2	RSVD 2	27	TxIN24	TA OUT3-	Rx 3-	3	Rx OUT24	NC	NC
	RSVD 3	RSVD 3	28	TxIN25			5	Rx OUT25	NC	NC
	DCLK		31	TxCLK IN	TxCLK OUT+ TxCLK OUT-	RxCLK IN+ RxCLK IN-	26	RxCLK OUT	DCLK	

R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE: Data enable signal

Notes(1) RSVD(reserved)pins on the transmitter shall be “H” or(“L” or OPEN)

5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

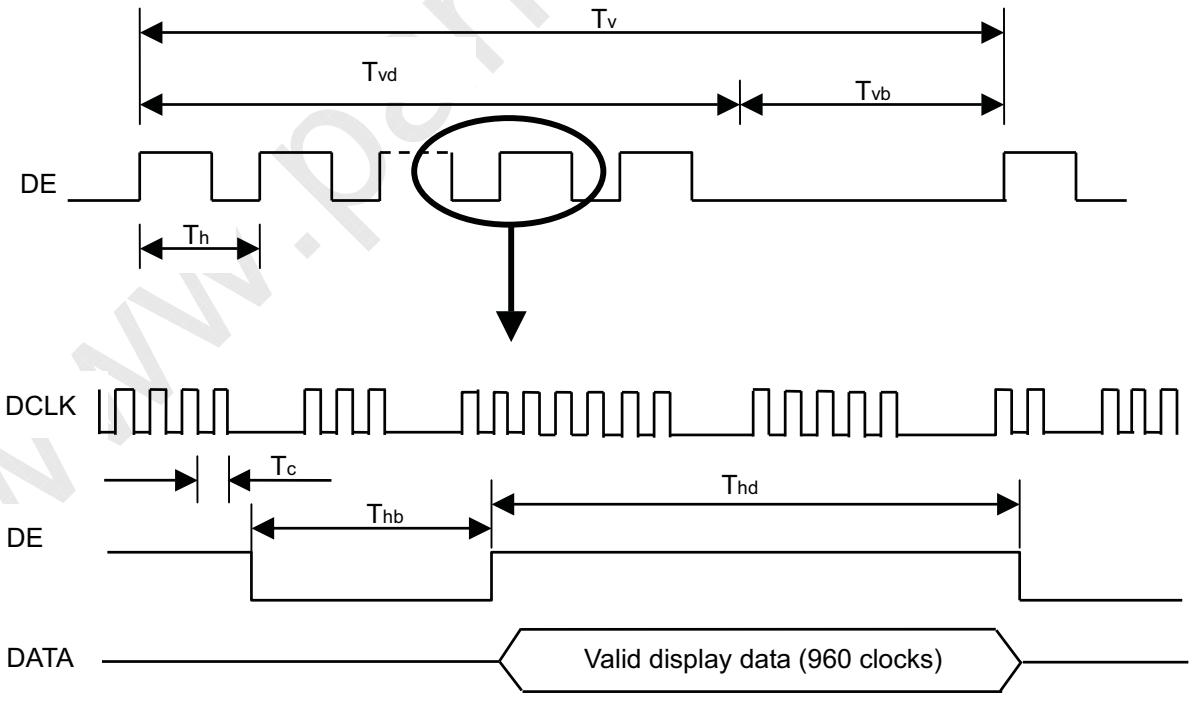
The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	1/Tc	60	74	80	MHz	
	Input cycle to cycle jitter	Trcl	-	-	200	ps	
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	
	Hold Time	Tlvhd	600	-	-	ps	
Vertical Active Display Term	Frame Rate	Fr5	47	50	53	Hz	(1)
		Fr6	57	60	63	Hz	(2)
	Total	Tv	1115	1125	1135	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	-
	Blank	Tvb	35	45	55	Th	-
Horizontal Active Display Term	Total	Th	1050	1100	1150	Tc	Th=Thd+Thb
	Display	Thd	960	960	960	Tc	-
	Blank	Thb	90	140	190	Tc	-

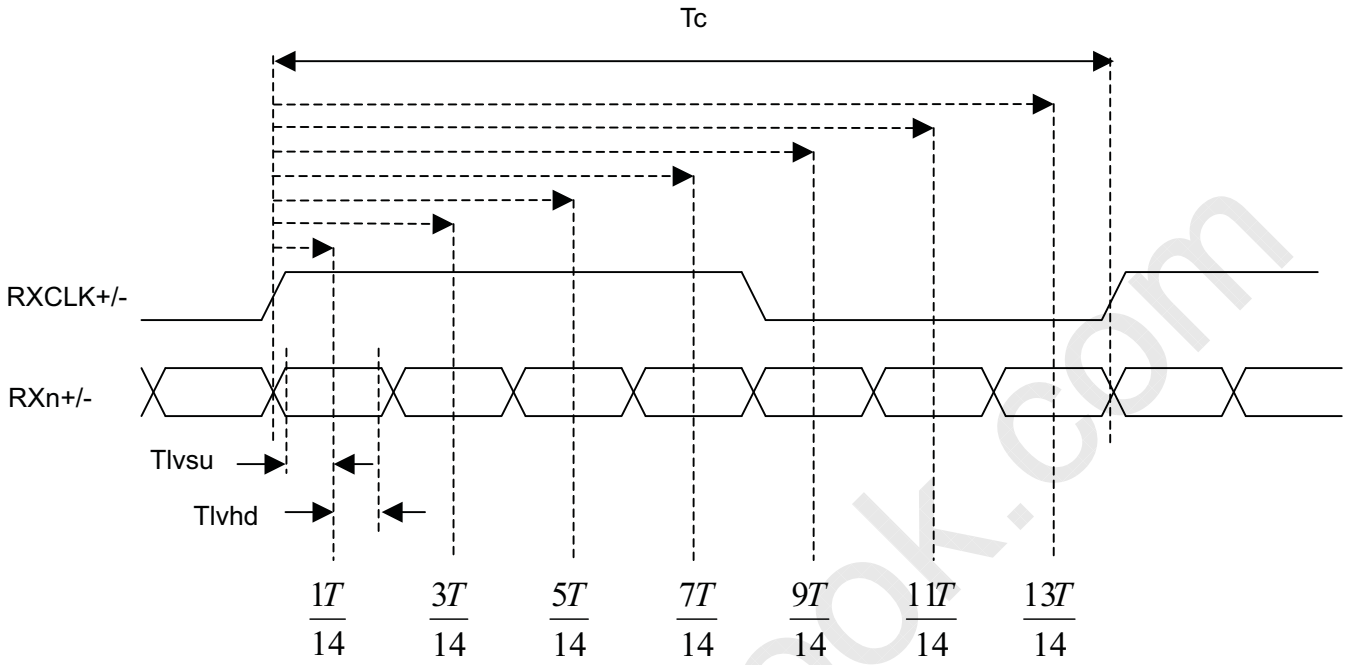
Note (1) (ODSEL) = (H). Please refer to 5.1 for detail information.

(2) (ODSEL) = (L). Please refer to 5.1 for detail information.

INPUT SIGNAL TIMING DIAGRAM

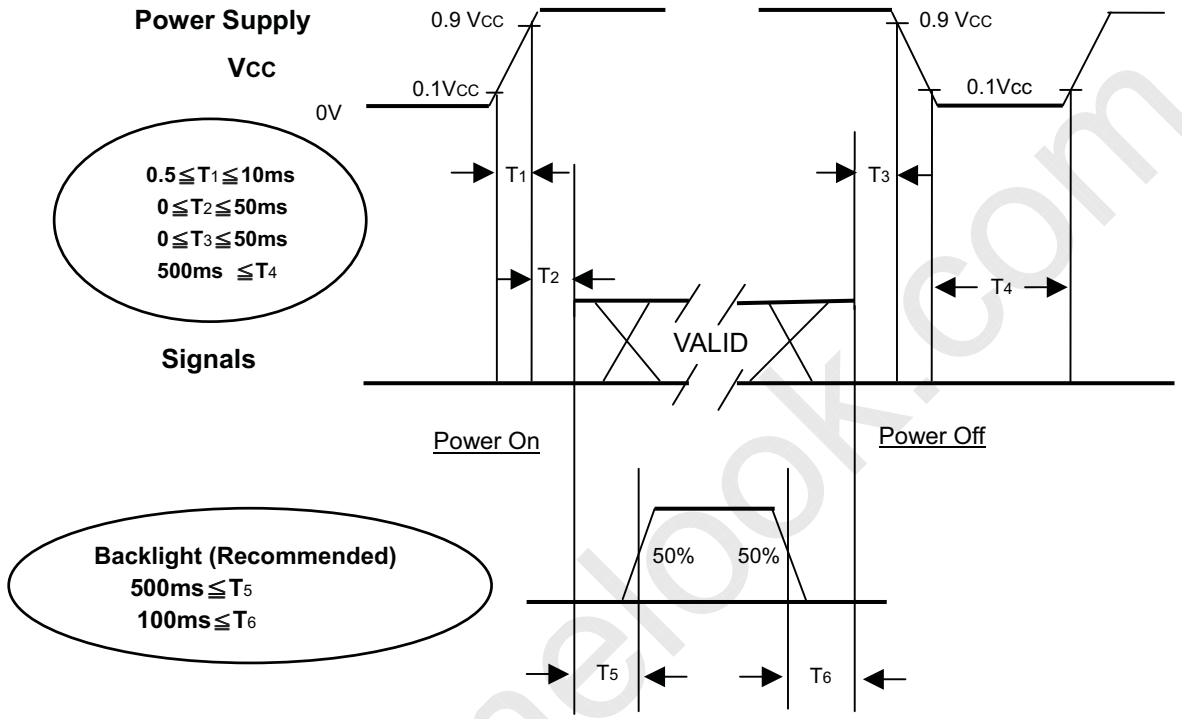


LVDS RECEIVER INTERFACE TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	12	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current(HV)	I_L	8.0 ± 0.5	mA
Oscillating Frequency (Inverter)	F_W	44±3	KHz
Frame rate		60	Hz

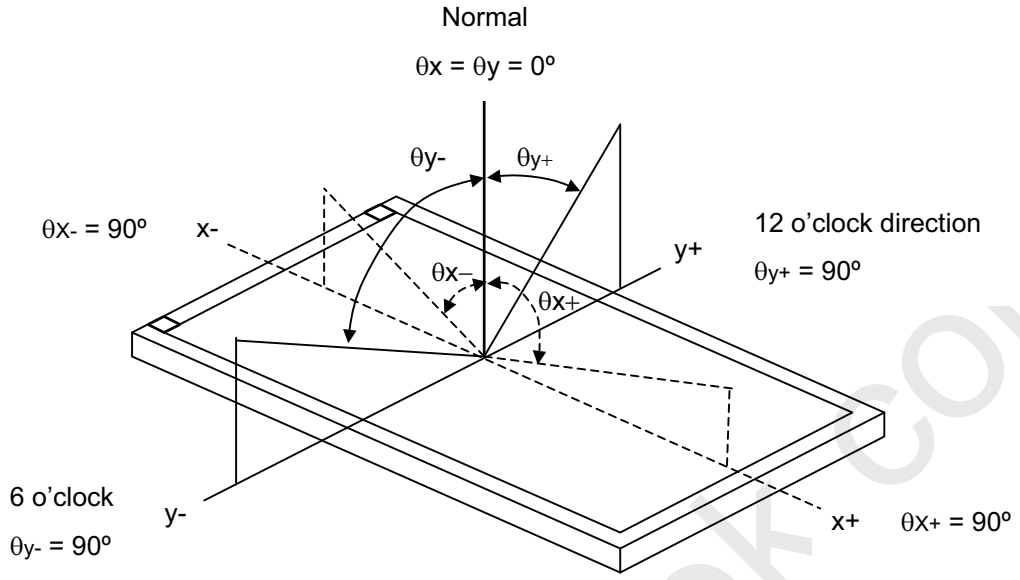
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing angle at Normal direction	TBD	(2000)	-	-	(2)
Response Time		Gray to gray average		-	(6.5)		ms	(3)
Center Luminance of White		L_C		TBD	(550)	-	cd/	(4)
White Variation		δW		-	-	1.3	-	(7)
Cross Talk		CT		-	-	4.0	%	(5)
Color Chromaticity	Red	Rx		Typ. – 0.03	(0.658)	Typ. + 0.03	-	(6)
		Ry			(0.328)		-	
	Green	Gx			(0.183)		-	
		Gy			(0.682)		-	
	Blue	Bx			(0.151)		-	
		By			(0.064)		-	
	White	Wx			0.280		-	
		Wy			0.280		-	
	Color Gamut	CG			(92)		%	NTSC
Viewing Angle	Horizontal	θ_x+	CR≥20		88	-	Deg.	(1)
		θ_x-			88	-		
	Vertical	θ_Y+			88	-		
		θ_Y-			88	-		

Note (1) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by EZ-Contrast 160R (Eldim)



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

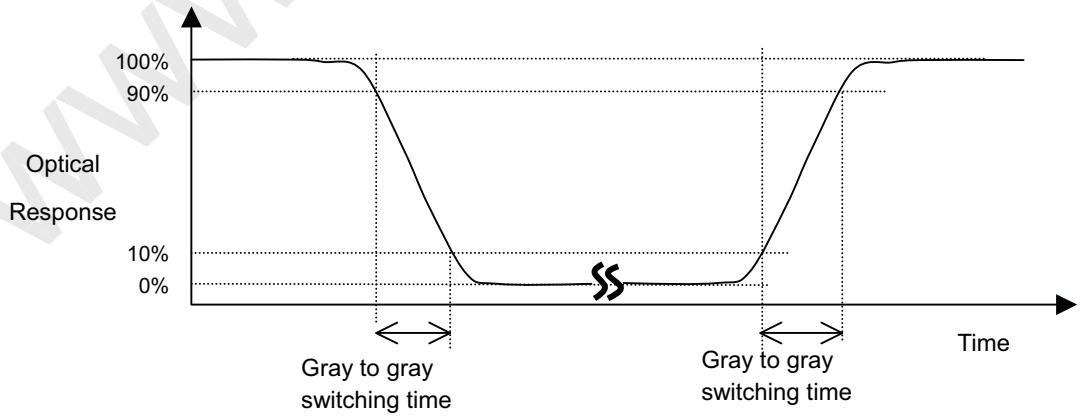
Contrast Ratio (CR) = L255 / L0

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (7).

Note (3) Definition of Gray to Gray Switching Time :



The driving signal means the signal of gray level 0, 63, 127, 191, 255.

Gray to gray average time means the average switching time of gray level 0 ,63,127,191,255 to each other .

Note (4) Definition of Luminance of White (L_C, L_{AVE}):

Measure the luminance of gray level 255 at center point and 5 points

$L_C = L(5)$

$L_{AVE} = [L(1)+ L(2)+ L(3)+ L(4)+ L(5)] / 5$

where L (x) is corresponding to the luminance of the point X at the figure in Note (7).

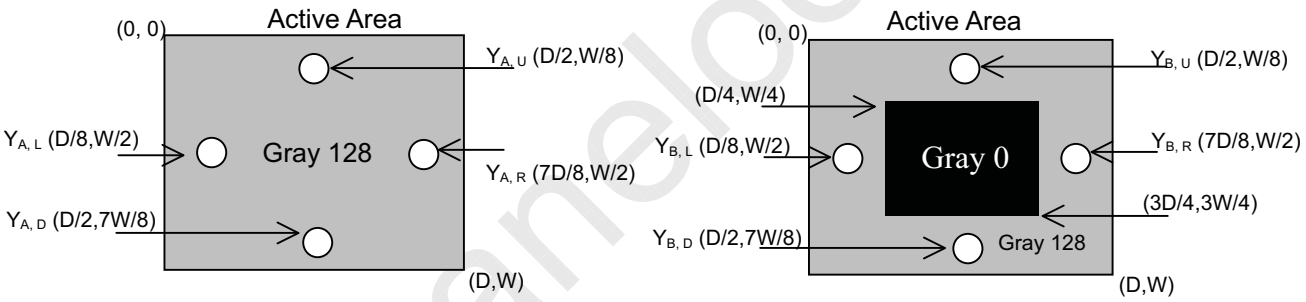
Note (5) Definition of Cross Talk (CT):

$CT = | Y_B – Y_A | / Y_A \times 100\ (\%)$

Where:

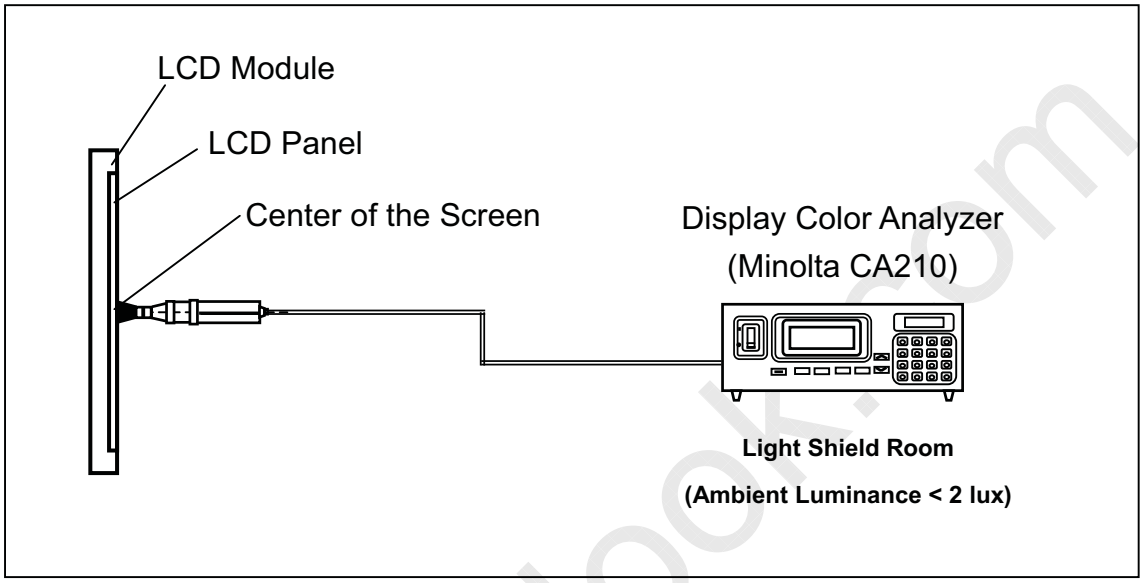
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



Note (6) Measurement Setup:

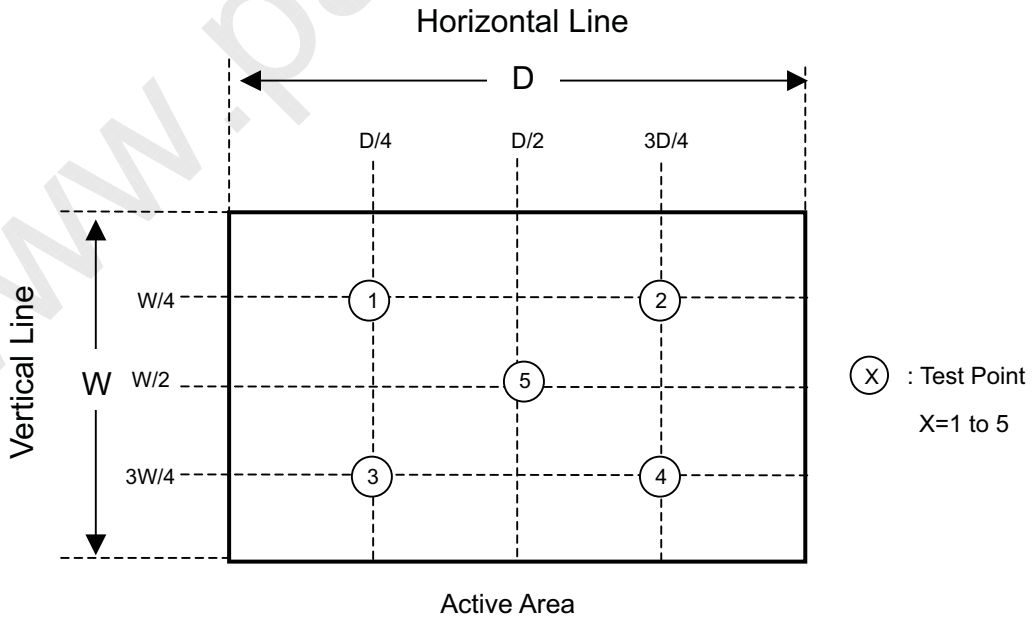
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 1 hour in a windless room.



Note (7) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and backlight.

(4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

(5) Do not plug in or pull out the I/F connector while the module is in operation.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) Moisture can easily penetrate into LCD module and may cause the damage during operation.

(9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.

(10) When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

8.2 SAFETY PRECAUTIONS

(1) The startup voltage of a backlight is over 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the backlight unit.

(2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(3) After the module's end of life, it is not harmful in case of normal operation and storage.

8.3 SAFETY STANDARDS

The LCD module should be certified with safety regulations as follows:

(1) UL60950-1 or updated standard.

(2) IEC60950-1 or updated standard.

(3) UL60065 or updated standard.

(4) IEC60065 or updated standard.

9. MECHANICAL CHARACTERISTICS