



- ☐ Tentative Specification
☐ Preliminary Specification
☒ Approval Specification

MODEL NO.: V320HK2**SUFFIX: PE1****32" FHD_120Hz Open Cell****Source board + Control board + FFC Cable****Customer:****APPROVED BY****SIGNATURE**

Name / Title _____

Note

Please return 1 copy for your confirmation with your signature and comments.

Refer to "V320HK2-PE1" Incoming Inspection Spec

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**CONTENTS**

REVISION HISTORY.....	4
1. GENERAL DESCRIPTION.....	5
1.1 OVERVIEW	5
1.2 FEATURES.....	5
1.3 MECHANICAL SPECIFICATIONS	5
2. ABSOLUTE MAXIMUM RATINGS	6
2.1 ABSOLUTE RATINGS OF ENVIRONMENT.....	6
2.2 PACKAGE STORAGE.....	7
2.3 ELECTRICAL ABSOLUTE RATINGS	7
2.3.1 TFT LCD MODULE	7
3. ELECTRICAL CHARACTERISTICS	8
3.1 TFT LCD MODULE	8
4. BLOCK DIAGRAM OF INTERFACE	11
4.1 TFT LCD MODULE	11
5. INPUT TERMINAL PIN ASSIGNMENT	12
5.1 TFT LCD Module Input.....	12
5.2 LVDS INTERFACE	15
5.3 COLOR DATA INPUT ASSIGNMENT	16
5.5 FLICKER (Vcom) ADJUSTMENT	17
6. INTERFACE TIMING.....	18
6.1 INPUT SIGNAL TIMING SPECIFICATIONS	18
6.2 POWER ON/OFF SEQUENCE.....	21
7. OPTICAL CHARACTERISTICS	22
7.1 TEST CONDITIONS.....	22
7.2 OPTICAL SPECIFICATIONS	23
8. PRECAUTIONS.....	26
8.1 ASSEMBLY AND HANDLING PRECAUTIONS	26



8.2 SAFETY PRECAUTIONS	27
9. DEFINITION OF LABELS.....	28
9.1 OPEN CELL LABEL	28
10. PACKAGING	29
10.1 PACKING SPECIFICATIONS	
10.2 PACKING METHOD	
11. MECHANICAL CHARACTERISTIC.....	31

**REVISION HISTORY**

Version	Date	Page(New)	Section	Description
Ver. 2.0	Oct. 30, 2011	All	All	Approval specification was first issued.

**1. GENERAL DESCRIPTION****1.1 OVERVIEW**

V320HK2-PE1 is a 31.5" TFT Liquid Crystal Display product with driver ICs and 2ch-LVDS interface. This product supports 1920 x 1080 Full HDTV format and can display 1.07G (8-bit+Hi-FRC)colors. The backlight unit is not built in.

1.2 FEATURES

CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [in]	31.51
Pixels [lines]	1920 x 1080
Active Area [mm]	698.4 (H) x 392.85 (V) (31.51" diagonal)
Sub-Pixel Pitch [mm]	0.12125 (H) x 0.36375 (V)
Pixel Arrangement	RGB vertical stripe
Weight [g]	871
Physical Size [mm]	716.1(H)X410.0 (V) × 1.4(D) Typ.
Display Mode	Transmissive mode / Normally black
Contrast Ratio	5000:1 Typ. (Typical value measure at CMI's module)
Glass thickness (Array / CF) [mm]	0.5 / 0.5
Viewing Angle (CR>20)	+88/-88(H), +88/-88(V) Typ. (CR≥20) (Typical value measure at CMI's module)
Color Chromaticity	R = (0.660, 0.320) G = (0.259, 0.585) B = (0.135, 0.097) W= (0.292, 0.343) Standard light source "C"
Cell Transparency [%]	4.3%Typ.. (Typical value measured at CMO's module)
Polarizer Surface Treatment	HTY Pol. Haze <3.5%

1.3 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Weight		871		g	-
I/F connector mounting position	The mounting inclination of the connector makes the screen center within $\pm 0.5\text{mm}$ as the horizontal.				(2)

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Connector mounting position

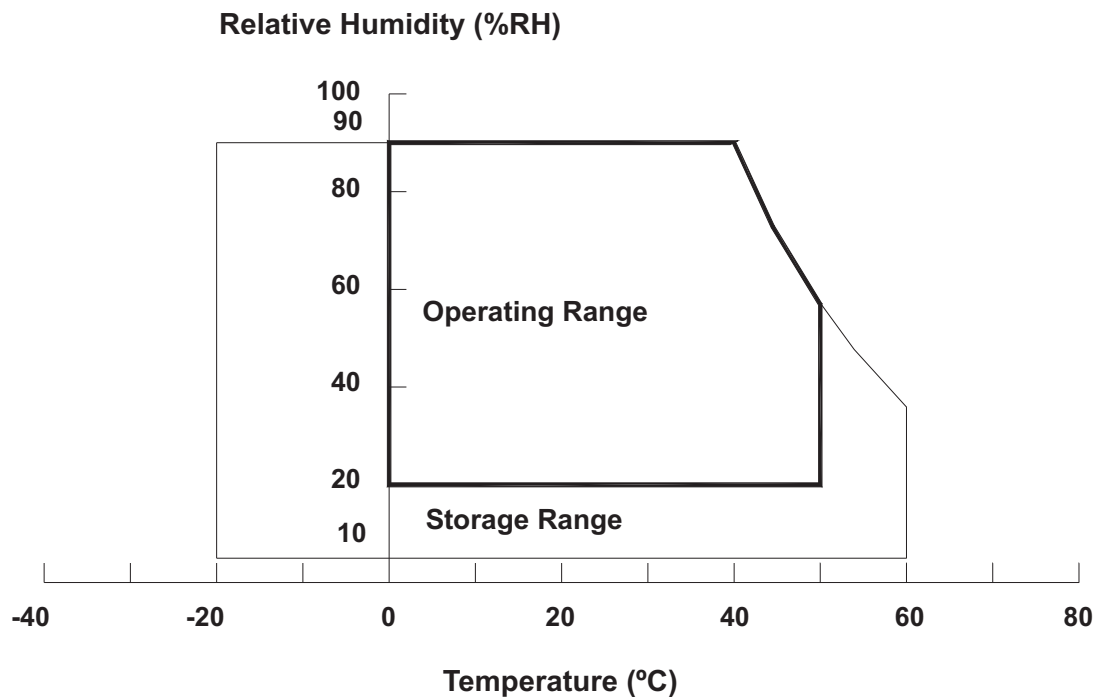
2. ABSOLUTE MAXIMUM RATINGS**2.1 ABSOLUTE RATINGS OF ENVIRONMENT**

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T _{ST}	-20	+60	°C	(1)
Operating Ambient Temperature	T _{OP}	0	+50	°C	(1), (2)

Note (1) Temperature and relative humidity range is shown in the figure below.

- (a) 90 %RH Max. ($T_a \leq 40\text{ }^{\circ}\text{C}$).
- (b) Wet-bulb temperature should be 39 °C Max. ($T_a > 40\text{ }^{\circ}\text{C}$).
- (c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.



**2.2 PACKAGE STORAGE**

Storage Condition : With shipping package.

Storage temperature range : 25±5 °C

Storage humidity range : 50±10%RH

Shelf life : a month

2.3 ELECTRICAL ABSOLUTE RATINGS**2.3.1 TFT LCD MODULE**

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	13.5	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

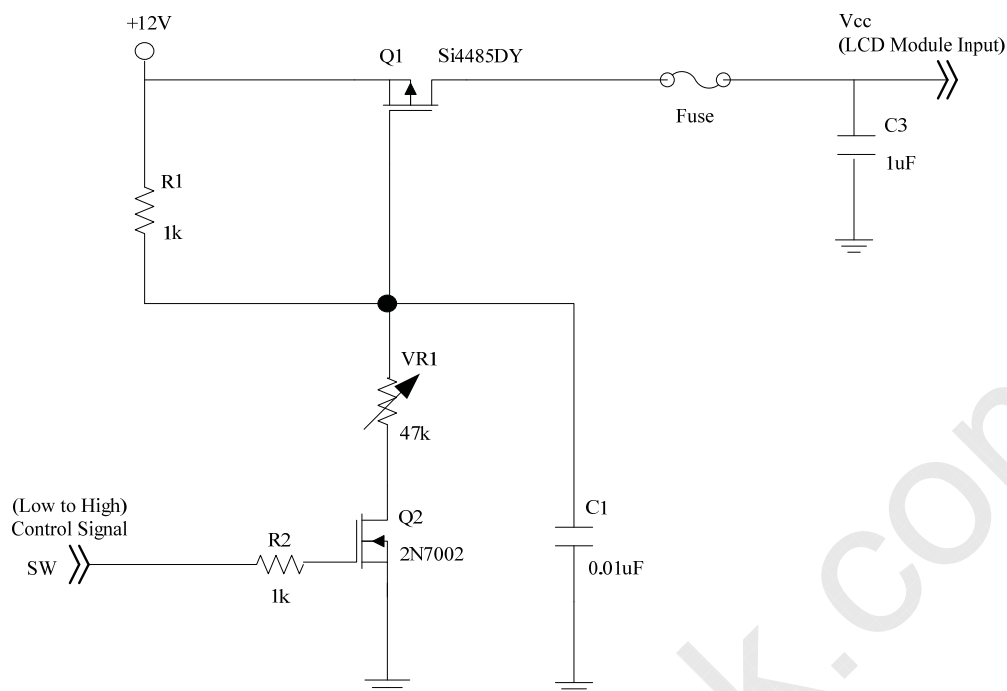
3. ELECTRICAL CHARACTERISTICS**3.1 TFT LCD MODULE**

(Ta = 25 ± 2 °C)

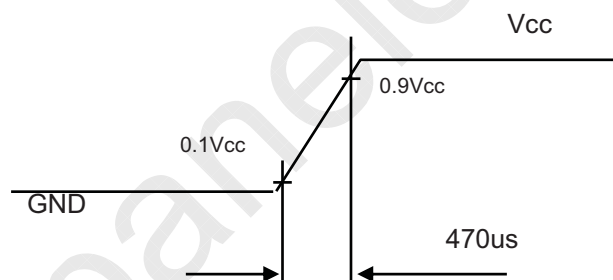
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V _{CC}	10.8	12	13.2	V	(1)
Rush Current		I _{RUSH}	—	—	4.45	A	(2)
Power Supply Current	White Pattern	—	—	1.06	—	A	(3)
	Horizontal Stripe	—	—	1.51	1.79	A	
	Black Pattern	—	—	1.07	—	A	
LVDS interface	Differential Input High Threshold Voltage	V _{LVTH}	+100	—	—	mV	(4)
	Differential Input Low Threshold Voltage	V _{LVTL}	—	—	-100	mV	
	Common Input Voltage	V _{CM}	1.0	1.2	1.4	V	
	Differential input voltage	V _{ID}	200	—	600	mV	
	Terminating Resistor	R _T	—	100	—	ohm	
CMOS interface	Input High Threshold Voltage	V _{IH}	2.7	—	3.3	V	
	Input Low Threshold Voltage	V _{IL}	0	—	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:

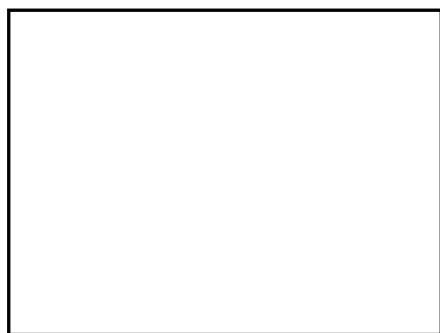


Vcc rising time is 470us



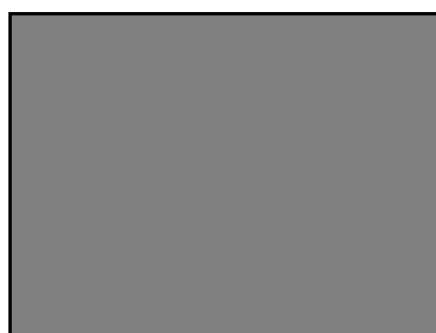
Note (3) The specified power supply current is under the conditions at $V_{cc} = 12\text{ V}$, $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$, $f_v = 60\text{ Hz}$, whereas a power dissipation check pattern below is displayed.

a. White Pattern

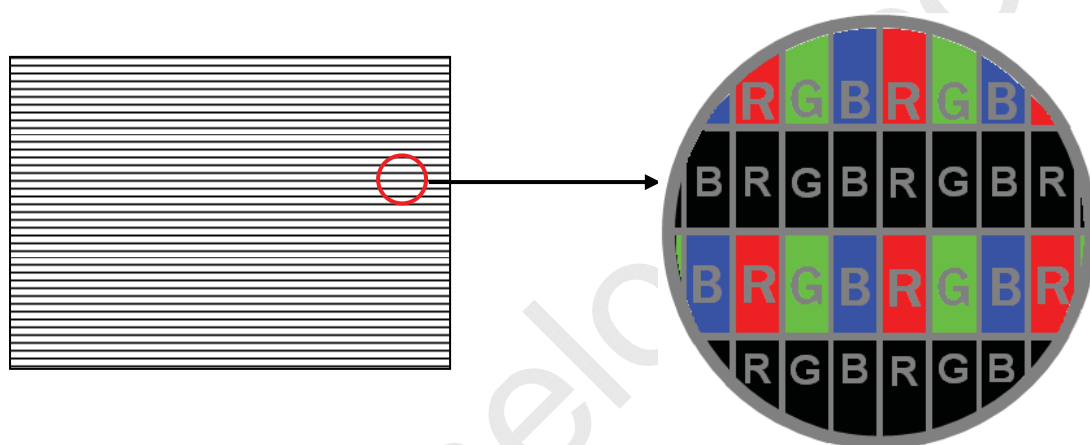


Active Area

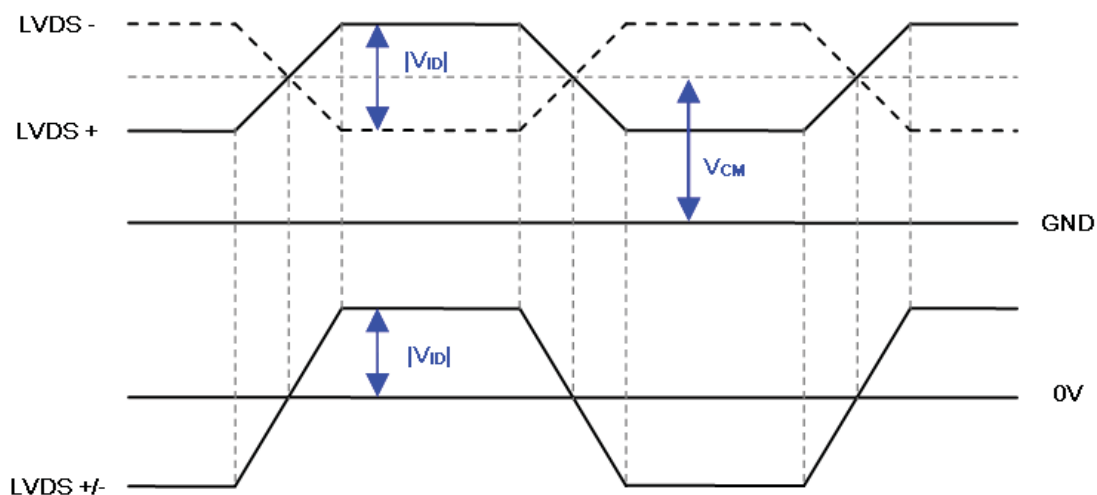
b. Black Pattern



Active Area

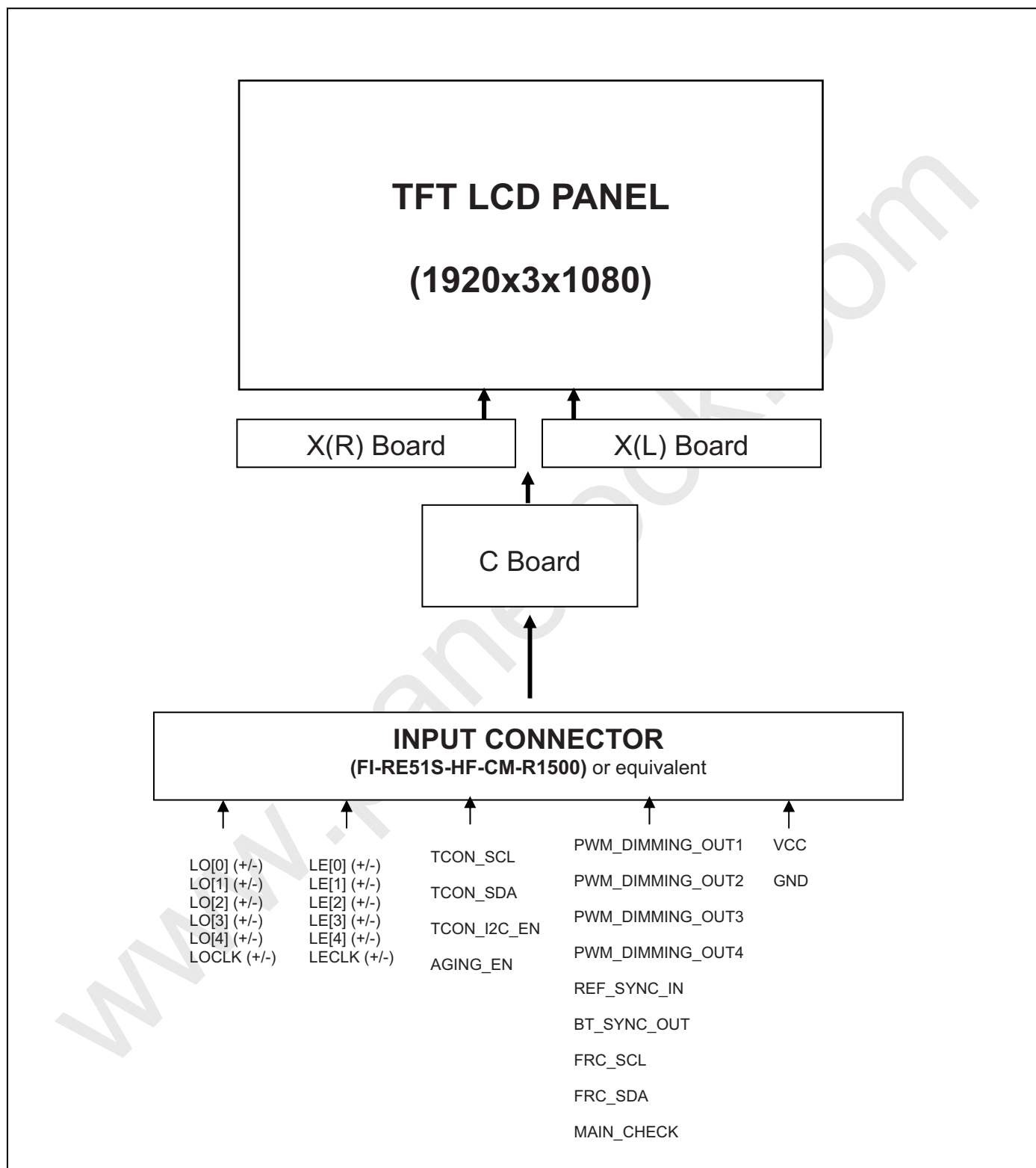


Note (4) The LVDS input characteristics are as follows:



4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



**5. INPUT TERMINAL PIN ASSIGNMENT****5.1 TFT LCD Module Input**

CN311 Connector Pin Assignment (FI-RE51S-HF-CM-R1500, JAE Taiwan(台灣航空電子) or equivalent)

Pin	Name	Description	Note
1	VCC	+12V power supply	
2	VCC	+12V power supply	
3	VCC	+12V power supply	
4	VCC	+12V power supply	
5	VCC	+12V power supply	
6	PWM_DIMMIN G_OUT4	PWM4 output for scanning control	
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	LO[0]-	Odd pixel Negative LVDS differential data input. Channel 0	(1)
11	LO[0]+	Odd pixel Positive LVDS differential data input. Channel 0	
12	LO[1]-	Odd pixel Negative LVDS differential data input. Channel 1	
13	LO[1]+	Odd pixel Positive LVDS differential data input. Channel 1	
14	LO[2]-	Odd pixel Negative LVDS differential data input. Channel 2	
15	LO[2]+	Odd pixel Positive LVDS differential data input. Channel 2	
16	GND	Ground	
17	LOCLK-	Odd pixel Negative LVDS differential clock input.	(1)
18	LOCLK+	Odd pixel Positive LVDS differential clock input.	
19	GND	Ground	
20	LO[3]-	Odd pixel Negative LVDS differential data input. Channel 3	(1)
21	LO[3]+	Odd pixel Positive LVDS differential data input. Channel 3	
22	LO[4]-	Odd pixel Negative LVDS differential data input. Channel 4	
23	LO[4]+	Odd pixel Positive LVDS differential data input. Channel 4	
24	GND	Ground	
25	LE[0]-	Even pixel Negative LVDS differential data input. Channel 0	(1)
26	LE[0]+	Even pixel Positive LVDS differential data input. Channel 0	
27	LE[1]-	Even pixel Negative LVDS differential data input. Channel 1	
28	LE[1]+	Even pixel Positive LVDS differential data input. Channel 1	

29	LE[2]-	Even pixel Negative LVDS differential data input. Channel 2	(1)
30	LE[2]+	Even pixel Positive LVDS differential data input. Channel 2	
31	GND	Ground	
32	LECLK-	Even pixel Negative LVDS differential clock input.	(1)
33	LECLK+	Even pixel Positive LVDS differential clock input.	
34	GND	Ground	
35	LE[3]-	Even pixel Negative LVDS differential data input. Channel 3	(1)
36	LE[3]+	Even pixel Positive LVDS differential data input. Channel 3	
37	LE[4]-	Even pixel Negative LVDS differential data input. Channel 4	
38	LE[4]+	Even pixel Positive LVDS differential data input. Channel 4	
39	GND	Ground	
40	TCON_SCL	I2C Bus of TCON	
41	REF_SYNC_I N	Shop Mode Sync	
42	BT_SYNC_OUT	BT Sync	
43	TCON_I2C_EN	Bus Switch Enable	(2)
44	TCON_SDA	I2C Bus of TCON	
45	PWM_DIMMING_OUT2	PWM2 output for scanning control	
46	PWM_DIMMING_OUT3	PWM3 output for scanning control	
47	FRC_SCL	I2C Bus of FRC	
48	PWM_DIMMING_OUT1	PWM1 output for scanning control	
49	FRC_SDA	I2C Bus of FRC	
50	MAIN_CHECK	TCON Board Stand Alone Mode	
51	AGING_EN.	TCON Aging Enable	(3)

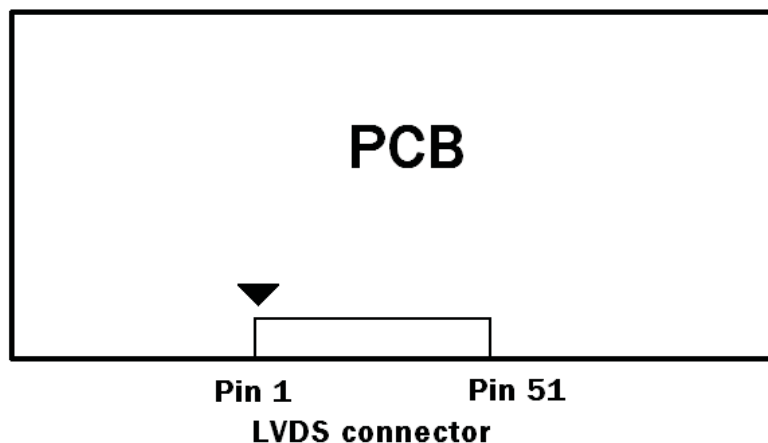
Note (1) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and second pixel is even pixel.

Note (2) High=connect to +3.3V : Enable bus switch ; Low= connect to GND or Open : Disable bus switch for I2C bus isolation.

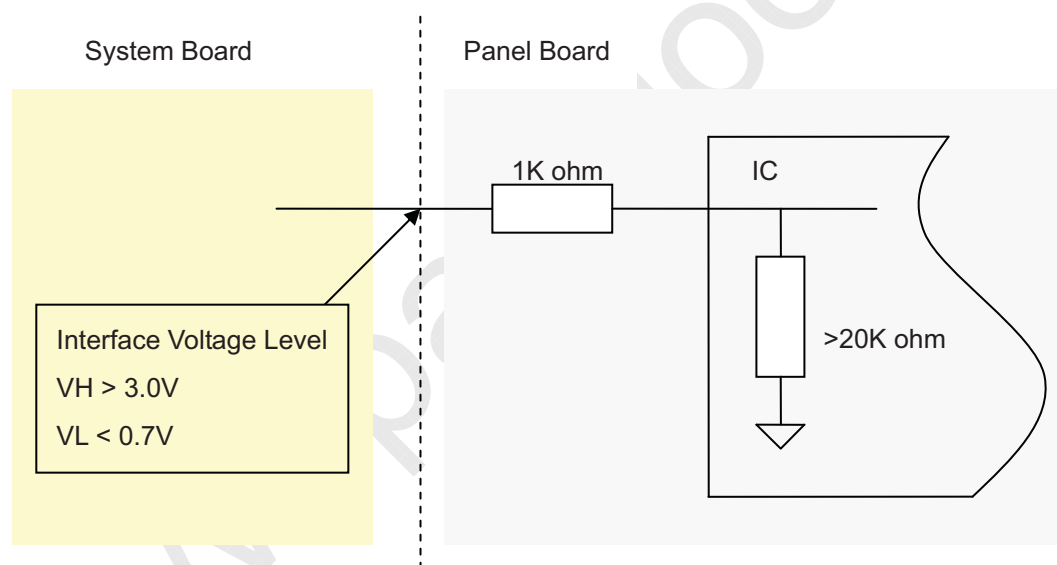
Note (3) High=connect to +3.3V : Enable TCON aging mode ; Low= connect to GND or Open : Disable TCON

aging mode.

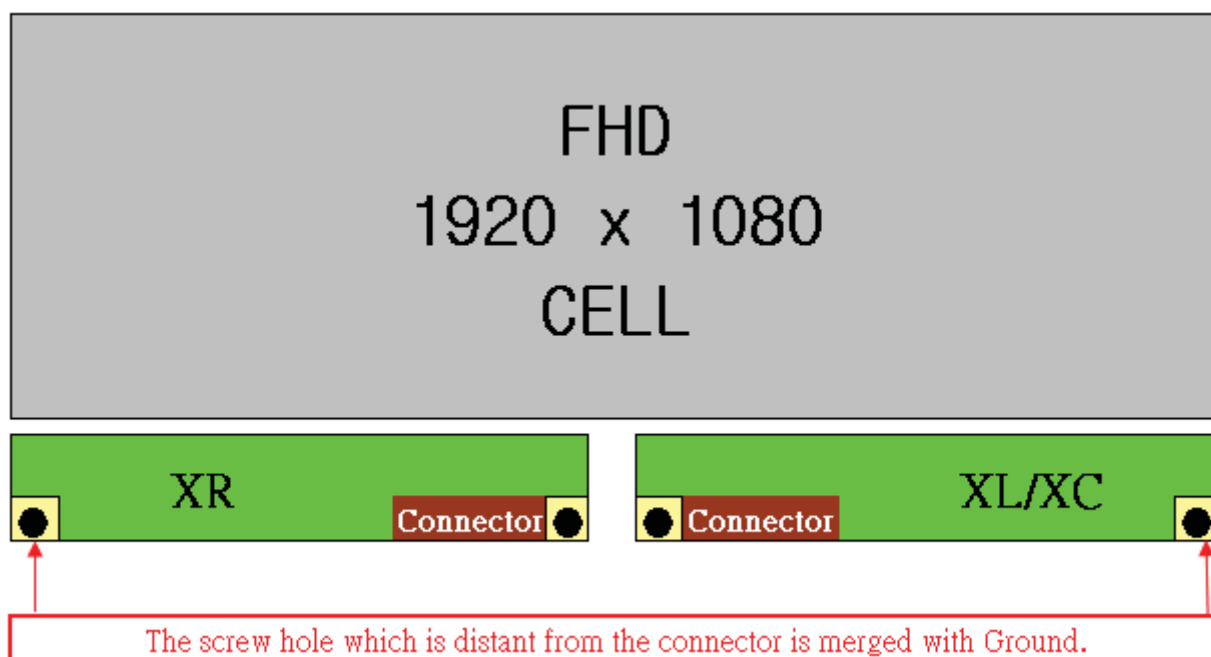
Note (4) LVDS connector pin order defined as follows



Note (5) Interface optional pin has internal scheme as following diagram. Customer should keep the interface voltage level requirement as below.

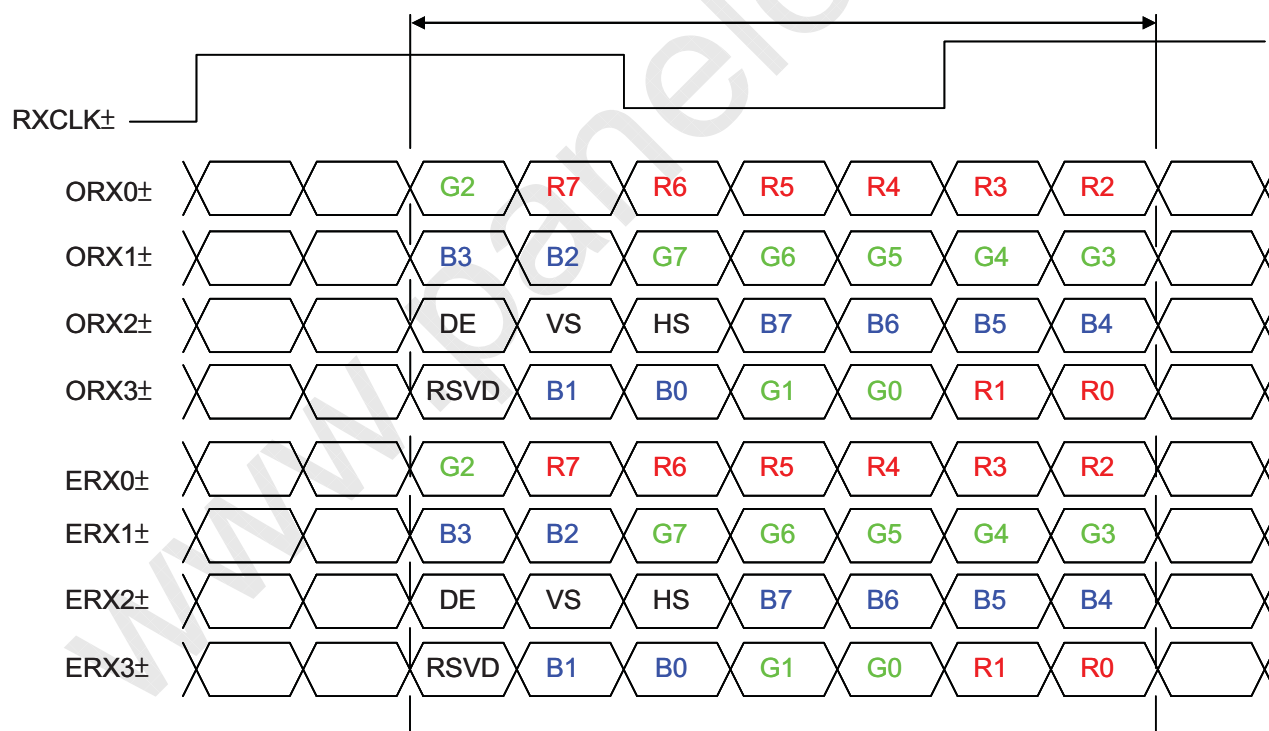


Note (6) The screw hole which is distant from the connector is marged with Ground.



5.2 LVDS INTERFACE

The TCON board should be input JEIDA format LVDS signal.



R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B9: Pixel B Data (7; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

Note(1): RSVD (Reserved) pins on the transmitter shall be “H” or “L”.

5.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color.

The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																															
		Red										Green										Blue											
R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0				
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	Red	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0			
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1			
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1			
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1			
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0			
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1			
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	Red (1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	Red (2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	:																																
	:																																
	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0			
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0			
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:			
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:			
	Green (1021)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0		
	Green (1022)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0		
	Green (1023)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0		
Gray Scale	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1			
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0			

Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Blue	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

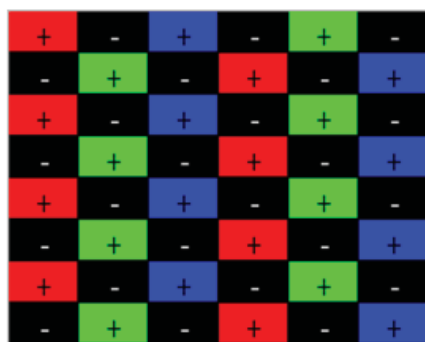
Note (1) 0: Low Level Voltage, 1: High Level Voltage

5.5 FLICKER (Vcom) ADJUSTMENT

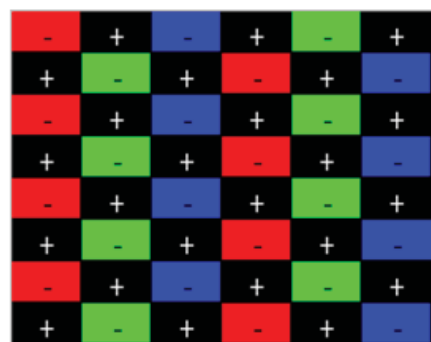
(1) Adjustment Pattern:

Sub pixel on/off Pattern was shown as below. If customer need below pattern, please directly contact with Account FAE. (bright sub-pixel : G128 ; dark sub-pixel : G0)

Frame N



Frame N+1_←



(2) Adjustment method: (Digital V-com)

Programmable memory IC is used for Digital V-com adjustment in this model. CMI provide Auto Vcom tools to adjust Digital V-com. The detail connection and setting instruction, please directly contact with Account FAE or refer CMI Auto V-com adjustment OI. Below items is suggested to be ready before Digital V-com adjustment in customer LCM line.

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

(Ta = 25 ± 2 °C)

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	73	74.25	75.5	MHz	
	Input cycle to cycle jitter	T_{rcl}	—	—	200	ps	(3)
	Spread spectrum modulation range	F_{clkin_mod}	$F_{clkin}-2\%$	—	$F_{clkin}+2\%$	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}			200	KHz	
LVDS Receiver Data	Receiver Skew Margin	T_{RSKM}	-400	—	400	ps	(5)
Vertical Active Display Term	Frame Rate	F_{r5}	—	50	—	Hz	
		F_{r6}	—	60	—	Hz	
	Total	T_v	1115	1125	1135	Th	$T_v=T_{vd}+T_{vb}$
	Display	T_{vd}	1080	1080	1080	Th	—
	Blank	T_{vb}	35	45	55	Th	—
Horizontal Active Display Term	Total	T_h	1080	1100	1120	Tc	$T_h=T_{hd}+T_{hb}$
	Display	T_{hd}	960	960	960	Tc	—
	Blank	T_{hb}	120	140	160	Tc	—

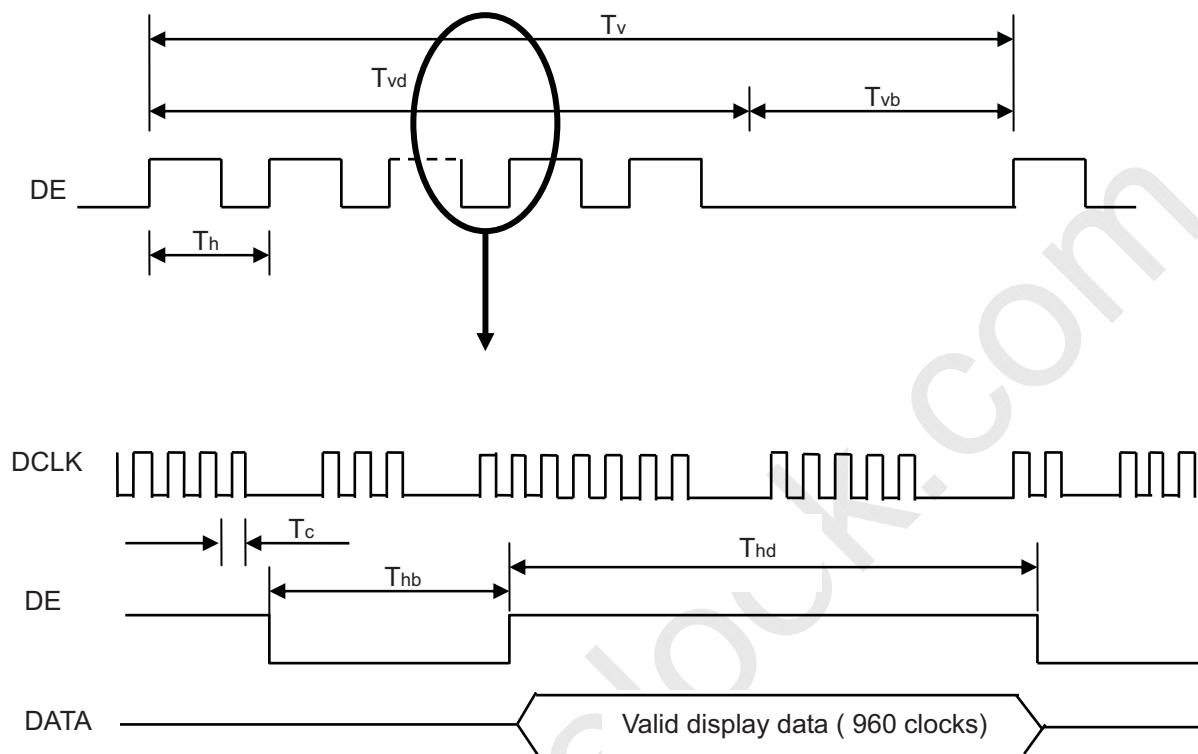
Note (1) Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

Note (2) Please make sure the range of pixel clock has follow the below equation:

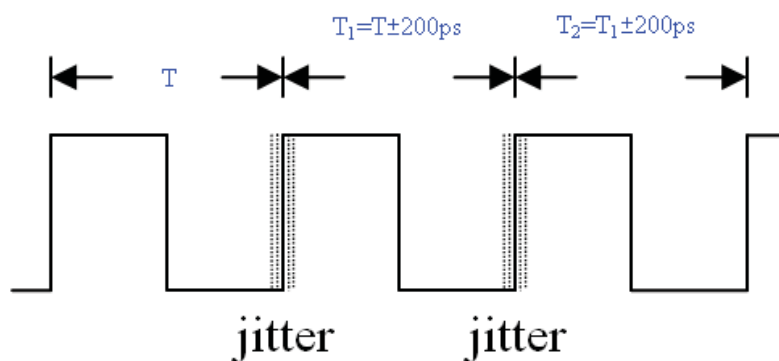
$$F_{clkin(max)} \geq F_{r6} \times T_v \times T_h$$

$$F_{r5} \times T_v \times T_h \geq F_{clkin(min)}$$

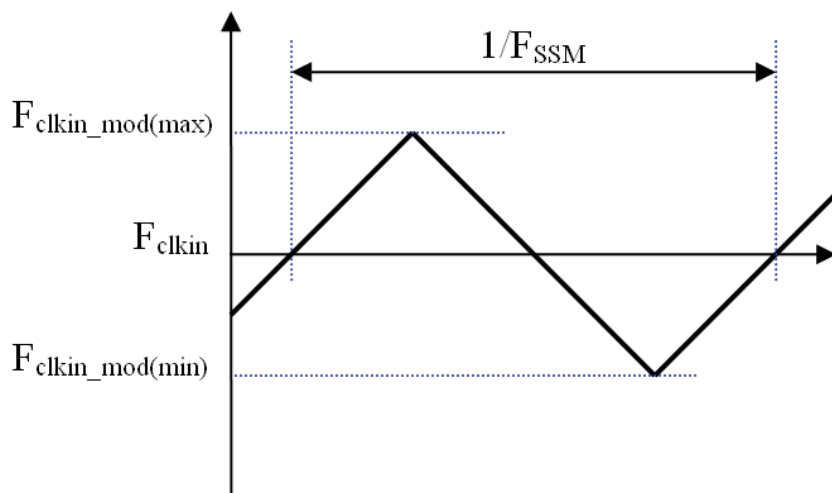
INPUT SIGNAL TIMING DIAGRAM



Note (3) The input clock cycle-to-cycle jitter is defined as below figures. $Trcl = |T_1 - T_1|$

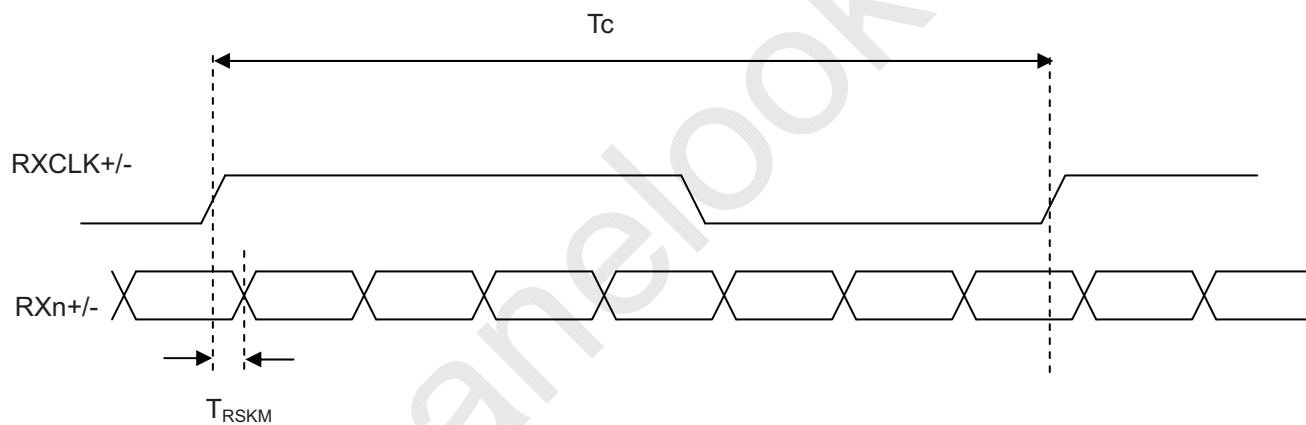


Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) LVDS receiver skew margin is defined and shown as below.

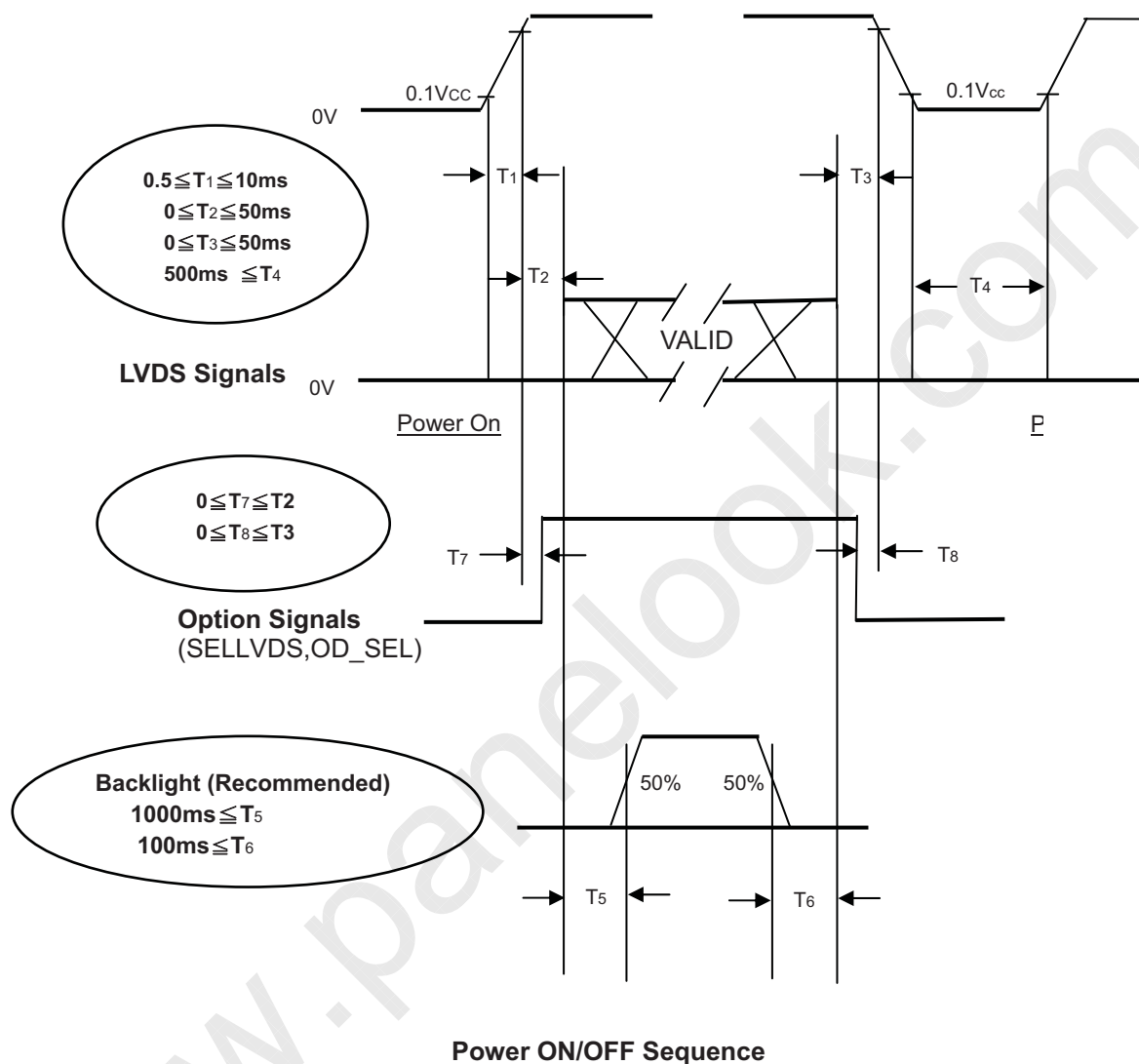
LVDS RECEIVER INTERFACE TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE

($T_a = 25 \pm 2^\circ\text{C}$)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Note (1) The supply voltage of the external system for the module input should follow the definition of V_{cc} .

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of V_{cc} is in off level, please keep the level of input signals on the low or high impedance. If $T_2 < 0$, that maybe cause electrical overstress failure.

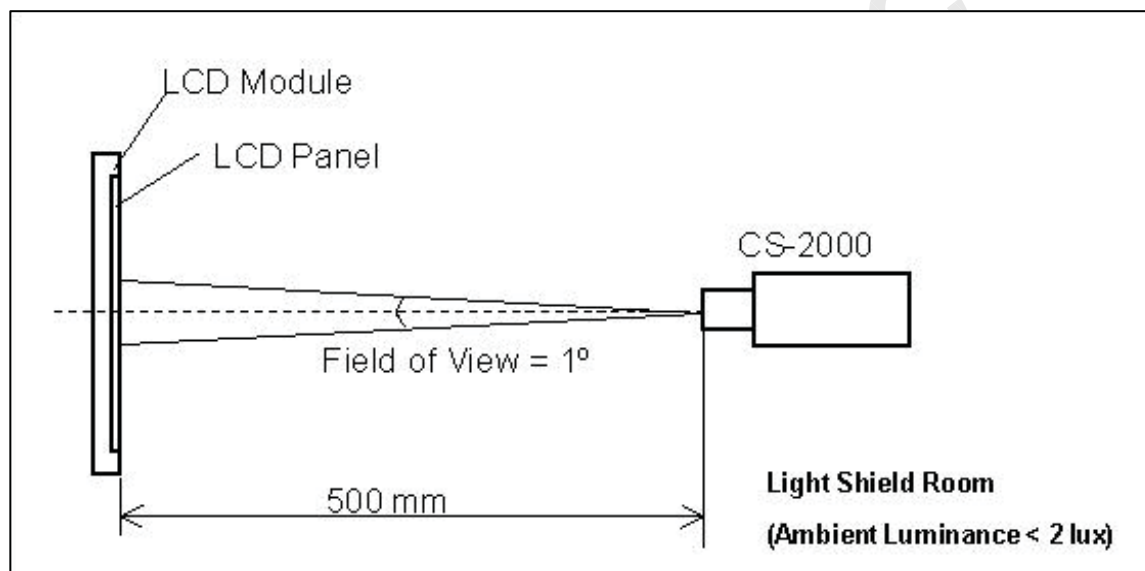
Note (4) T_4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS**7.1 TEST CONDITIONS**

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V _{CC}	12.0	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	I _L	7.5 ± 0.5	mA
Oscillating Frequency (Inverter)	F _w	40 ± 3	KHz
Vertical Frame Rate	Fr	120	Hz

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring in a windless room.



7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown as below. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity	Red	Rcx	$\theta_x=0^\circ, \theta_Y=0^\circ$ Viewing Angle at Normal Direction Standard light source “C”	-	0.660	-	-	(0),(1)
		Rcy			0.320		-	
	Green	Gcx			0.259		-	
		Gcy			0.585		-	
	Blue	Bcx			0.135		-	
		Bcy			0.097		-	
	White	Wcx			0.292		-	
		Wcy			0.343		-	
Center Transmittance		T%	$\theta_x=0^\circ, \theta_Y=0^\circ$	-	4.3	-	%	(1),(6)
Contrast Ratio		CR	with CMI module	3500	5000	-	-	(1),(3)
Response Time (VA)		Gray to gray	$\theta_x=0^\circ, \theta_Y=0^\circ$ with CMI Module@120Hz	-	6.5	12		(1),(4)
White Variation		δW	$\theta_x=0^\circ, \theta_Y=0^\circ$ with CMI module	-	-	1.3	-	(1),(5)
Viewing Angle	Horizontal	θ_x+	$CR\geq 20$ (VA) with CMI module		88		Deg.	(1),(2)
		θ_x-			88			
	Vertical	θ_Y+			88			
		θ_Y-			88			

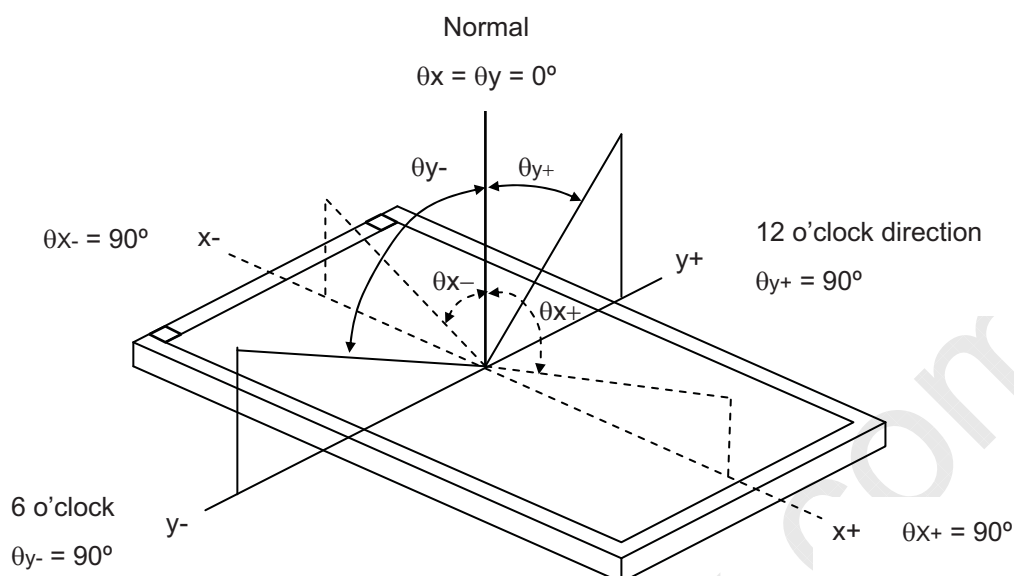
Note (0) Light source is the standard light source "C" which is defined by CIE and driving voltage are based on suitable gamma voltages. The calculating method is as following:

1. Measure Module's W,R,G,B spectrum and BLU's spectrum. Which BLU (for V315H3-L02) is supplied by CMI.
2. Calculate cell's spectrum.
3. Calculate cell's chromaticity by using the spectrum of standard light source "C".

Note (1) Light source is the BLU which supplied by CMI and driving voltage are based on suitable gamma voltages.

Note (2) Definition of Viewing Angle (θ_x, θ_y):

Viewing angles are measured by Autronic Conoscope Cono-80 (or Eldim EZ-Contrast 160R)



Note (3) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

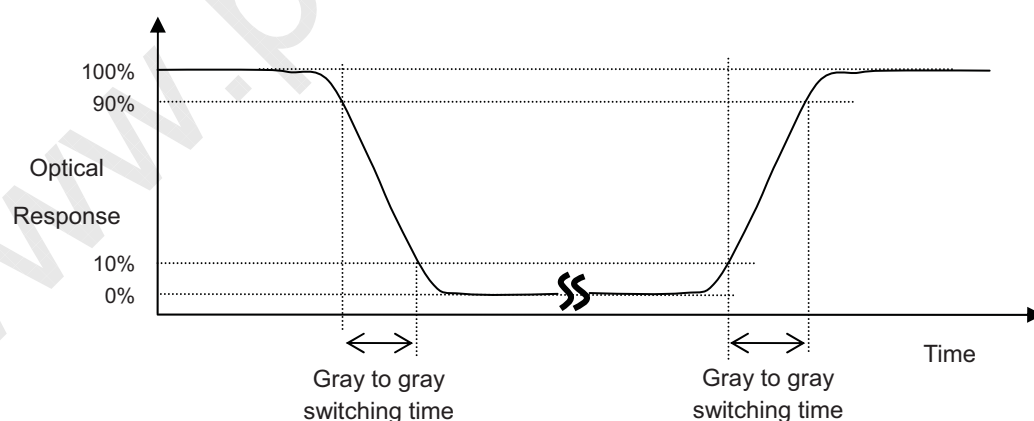
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L1023}}{\text{Surface Luminance of L0}}$$

L255: Luminance of gray level 1023

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (4) Definition of Gray-to-Gray Switching Time:



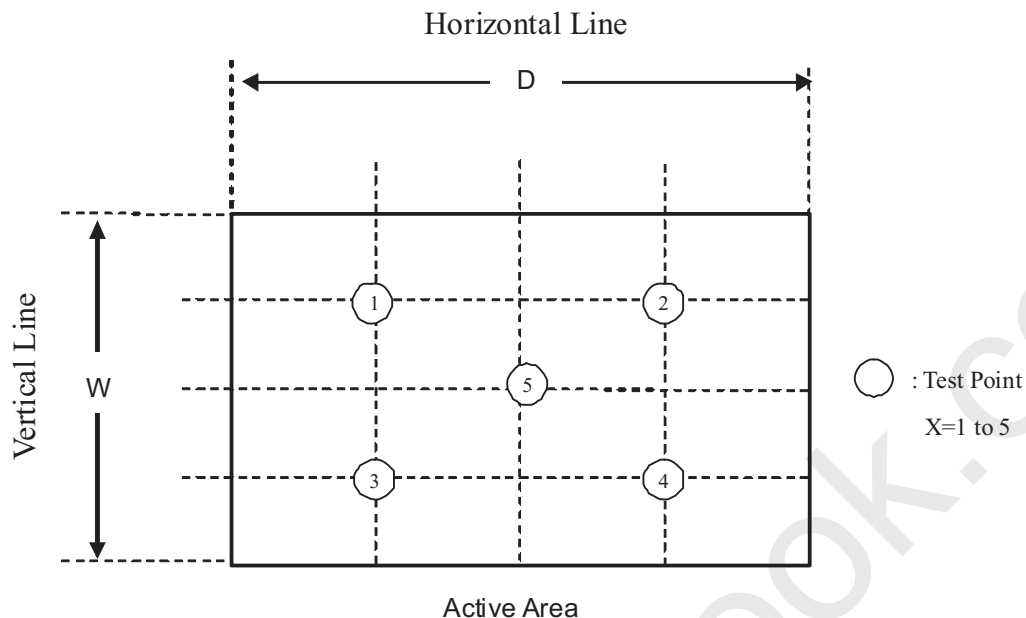
The driving signal means the signal of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023.

Gray to gray average time means the average switching time of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023 to each other.

Note (5) Definition of White Variation (δW):

Measure the luminance of gray level 1023 at 5 points

$$\delta W = \text{Maximum [L (1), L (2), L (3), L (4), L (5)]} / \text{Minimum [L (1), L (2), L (3), L (4), L (5)]}$$



Note (6) Definition of Transmittance (T%) :

Measure the luminance of gray level 1023 at center point of LCD module.

$$\text{Transmittance (T\%)} = \frac{\text{Luminance of LCD module}}{\text{Luminance of backligh unit}} \times 100\% \text{ PRECAUTIONS}$$

8. PRECAUTIONS**8.1 ASSEMBLY AND HANDLING PRECAUTIONS**

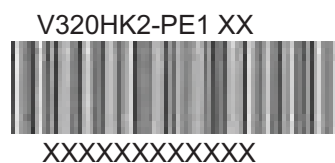
- [1] Do not apply rough force such as bending or twisting to the module during assembly.
- [2] It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- [3] Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.
- [4] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.
- [5] The distance between COF edge and rib of BLU must bigger than 5mm. This can prevent the damage of COF when assemble the module.
- [6] Do not design sharp-pointed structure / parting line / tooling gate on the COF position of plastic parts, because the burr will scrape the COF.
- [7] If COF would bended to assemble in the module. Do not put the IC location on the bending corner of COF.
- [8] The gap between COF IC and any structure of BLU must bigger than 2mm. This can prevent the damage of COF IC
- [9] Bezel opening must have no burr. Burr will scrape the panel surface.
- [10] Bezel of module and bezel of set can not press or touch the panel surface. It will make light leakage or scrape.
- [11] When module used FFC / FPC, but no FFC / FPC to be attached in the open cell. Customer can refer the FFC / FPC drawing and buy it by self.
- [12] The gap between Panel and any structure of Bezel must bigger than 2mm. This can prevent the damage of Panel.
- [13] Do not plug in or pull out the I/F connector while the module is in operation.
- [14] Do not disassemble the module.
- [15] Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- [16] Moisture can easily penetrate into LCD module and may cause the damage during operation.
- [17] When storing modules as spares for a long time, the following precaution is necessary.
 - [17.1] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35°C at normal humidity without condensation.
 - [17.2] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.
- [18] When ambient temperature is lower than 10°C, the display quality might be reduced.

**8.2 SAFETY PRECAUTIONS**

- [1] The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.
- [2] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- [3] After the module's end of life, it is not harmful in case of normal operation and storage.

9. DEFINITION OF LABELS**9.1 OPEN CELL LABEL**

The barcode nameplate is pasted on each open cell as illustration for CMI internal control.

**9.2 CARTON LABEL**

The barcode nameplate is pasted on each box as illustration, and its definitions are as following explanation.

PO.NO.	_____	
Part ID.	_____	Quantities <u>10</u>
Model Name	V320HK2-PE1	
Carton ID.	_____	

- (a) ModelName:V320HK2-PE1
- (b) Carton ID: CMI internal control
- (c) Quantities: 10

10. PACKAGING

10.1 PACKING SPECIFICATIONS

- (1) 10 LCD TV Panels / 1 Box
- (2) Box dimensions : 810 (L) X 555 (W) X92 (H)mm
- (3) Weight : approximately 16Kg (10 panels per box)
- (4) 260 LCD TV Panels / 1 Group

10.2 PACKING METHOD

Figures 10-1 and 10-2 are the packing method

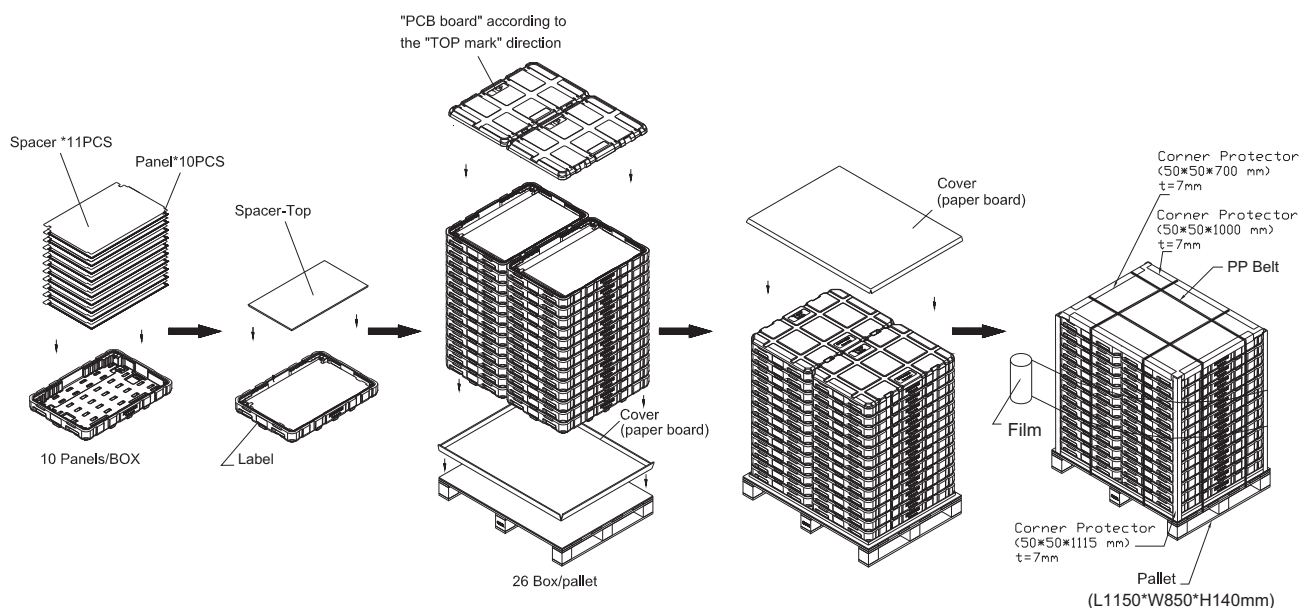
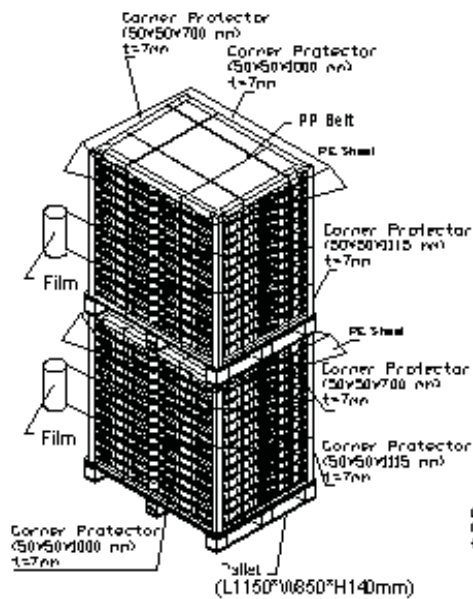


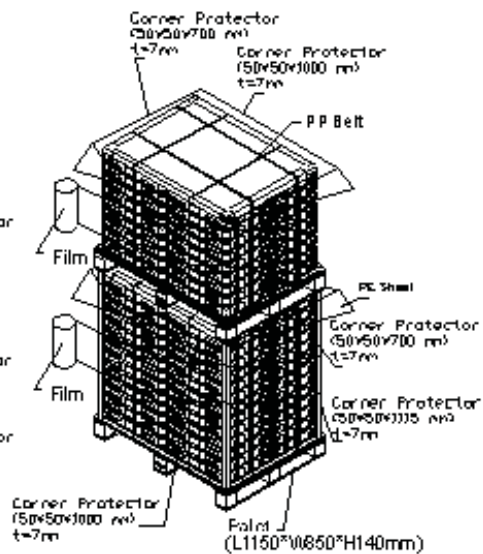
Figure.10-1 packing method

Sea / Land Transportation
(40ft HQ Container)



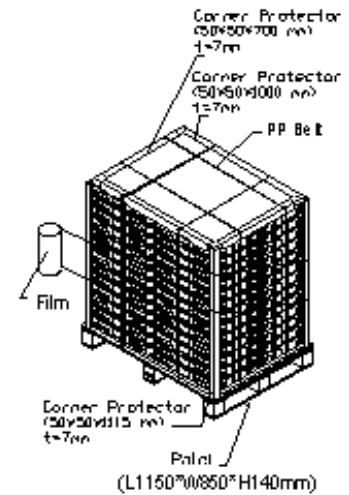
26 Box / Pallet + 26 Box / Pallet

Sea / Land Transportation



26 Box / Pallet + 18 Box / Pallet

Air Transportation



26 Box / Pallet

11. MECHANICAL CHARACTERISTIC

