



TFT LCD Approval Specification

MODEL NO.: V260H1 – P03

Customer: _____

Approved by: _____

Note:

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**REVISION HISTORY**

Version	Date	Page (New)	Section	Description
Ver 2.0	Feb. 11,'10	All	All	Approval Specification was first issued.
Ver 2.1	Jul. 23,'10	25~27	8	Add T2 LCM label information.
		31	11	Modify the drawing of mechanical.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V260H1- P03 is a 26-inch TFT LCD cell with driver ICs and 2ch-LVDS interface. This module supports 1920 x 1080 Full HDTV format and can display 16.7M colors (8-bit/color). The backlight unit is not built in

1.2 CHARACTERISTICS

CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [in]	26.0
Pixels [lines]	1920 x 1080
Active Area [mm]	576 x 324
Sub -Pixel Pitch [mm]	0.100 (H) × 0.300(V)
Pixel Arrangement	RGB vertical stripe
Weight [g]	TYP. 865
Physical Size [mm]	592(W) x 339.8(H) x 1.83(D) Typ.
Display Mode	TN, Normally White
Contrast Ratio	800:1 Typ. (Typical value measured at CMI's module)
Glass thickness (Array/CF) [mm]	0.7 / 0.7
Viewing Angle (CR>10)	+80/-80(H), +80/-70(V) Typ. (Typical value measured at CMI's module)
Color Chromaticity	R= 0.654, 0.329 G= 0.275, 0.600 B= 0.147, 0.106 W= 0.320, 0.365 *Please refer to "color chromaticity" on p.21
Cell Transparency [%]	6.1% Typ. (Typical value measured at CMI's module)
Polarizer (CF side)	Anti-Glare coating, 587.4(W) x 335.2(H). Hardness: 3H
Polarizer (TFT side)	587.4(W) x 335.2(H)

1.3 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Weight		865		g	
I/F connector mounting position	The mounting inclination of the connector makes the screen center within $\pm 0.5\text{mm}$ as the horizontal.				(1)

Note (1) Connector mounting position



2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT (BASED ON CMI MODULE V260H1-L03)

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T _{ST}	-20	+60	°C	(1)
Operating Ambient Temperature	T _{OP}	0	+50	°C	(1), (2)

Note (1) Temperature and relative humidity range is shown in the figure below.

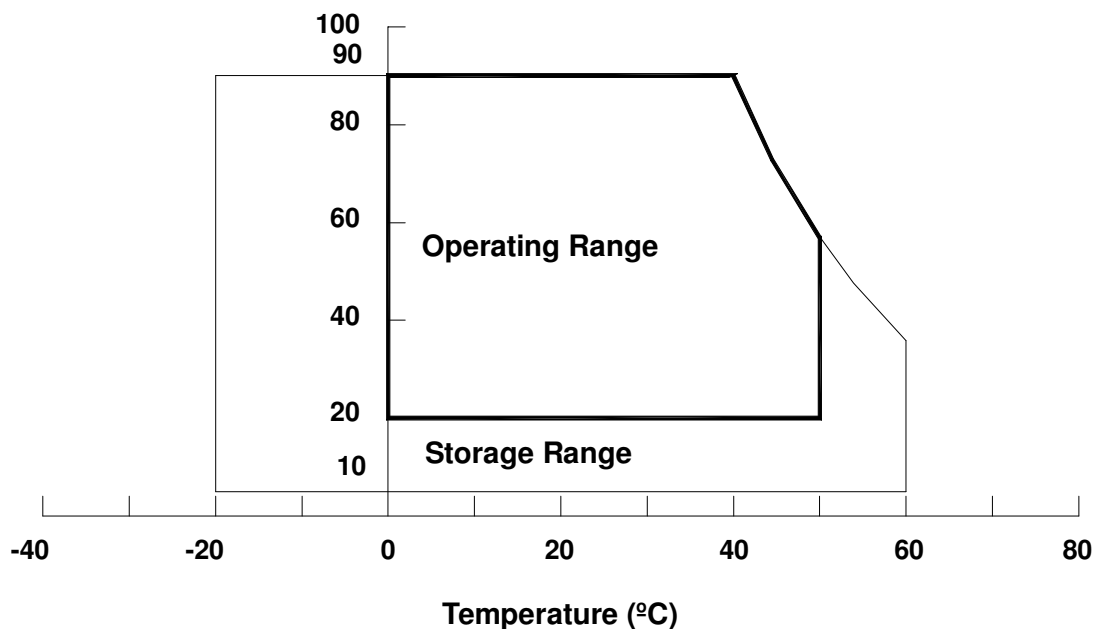
(a) 90 %RH Max. ($T_a \leq 40\text{ }^{\circ}\text{C}$).

(b) Wet-bulb temperature should be 39 °C Max. ($T_a > 40\text{ }^{\circ}\text{C}$).

(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.

Relative Humidity (%RH)



**2.2 ABSOLUTE RATINGS OF ENVIRONMENT (OPEN CELL)**

Storage Condition : With shipping package.

Storage temperature range : 25 ± 5 °CStorage humidity range : $50\pm10\%$ RH

Shelf life : a month

2.3 ELECTRICAL ABSOLUTE RATINGS**2.3.1 ELECTRICAL ABSOLUTE RATINGS (OPEN CELL)**

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V _{CC}	-0.3	13.5	V	(1)
Input Signal Voltage	V _{IN}	-0.3	3.6	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

3. ELECTRICAL CHARACTERISTICS

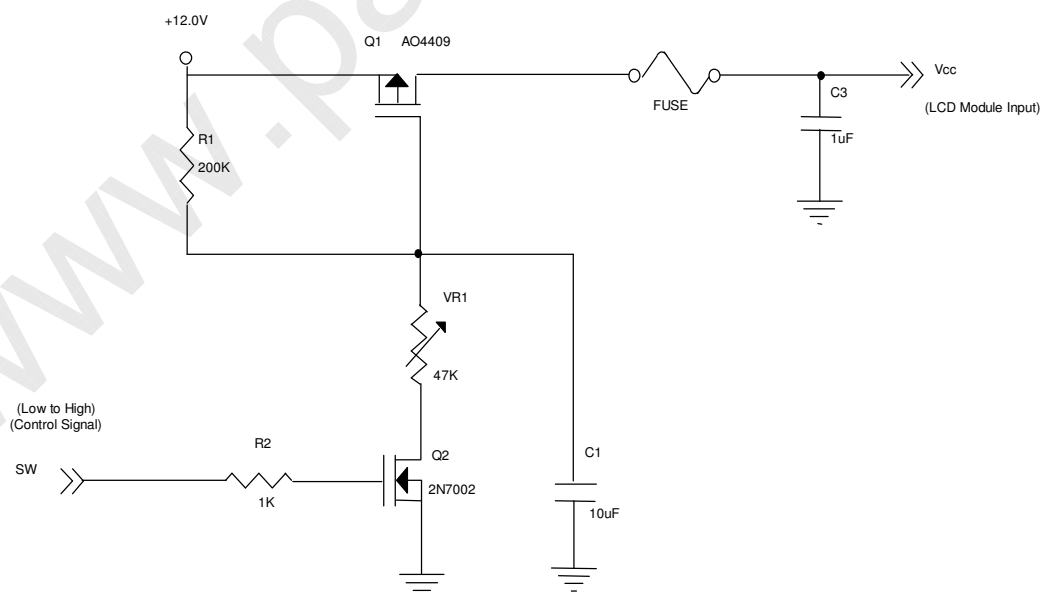
3.1 TFT LCD MODULE

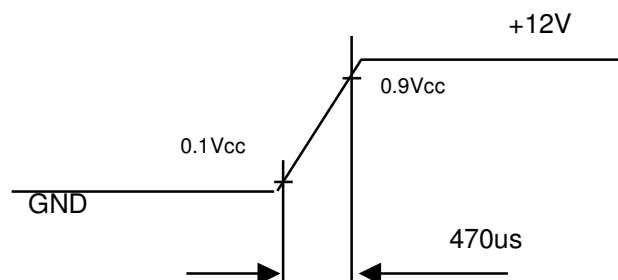
Ta = 25 ± 2 °C

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V _{CC}	10.8	12	13.2	V	(1)
Rush Current		I _{RUSH}	—	—	3.0	A	(2)
Power Supply Current	White Pattern	—	—	0.29	—	A	(3)
	Horizontal Stripe	—	—	0.45	—	A	
	Black Pattern	—	—	0.46	0.55	A	
LVDS interface	Differential Input High Threshold Voltage	V _{LVTH}	+100	—	—	mV	(4)
	Differential Input Low Threshold Voltage	V _{LVTL}	—	—	-100	mV	
	Common Input Voltage	V _{CM}	1.0	1.2	1.4	V	
	Differential input voltage	V _{ID}	200	—	600	mV	
	Terminating Resistor	R _T	—	100	—	ohm	
CMOS interface	Input High Threshold Voltage	V _{IH}	2.7	—	3.3	V	
	Input Low Threshold Voltage	V _{IL}	0	—	0.7	V	

Note (1) The module should be always operated within above ranges.

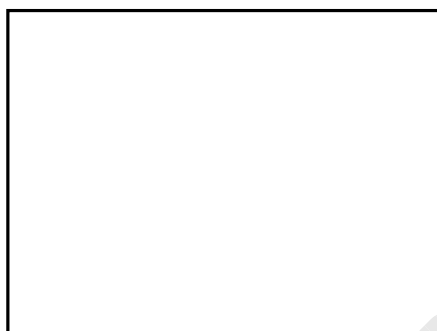
Note (2) Measurement Conditions:



Vcc rising time is 470us

Note (3) The specified power supply current is under the conditions at $V_{cc} = 12\text{ V}$, $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$, $f_v = 60\text{ Hz}$, whereas a power dissipation check pattern below is displayed.

a. White Pattern



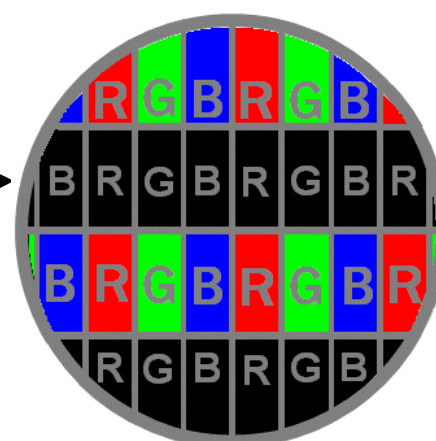
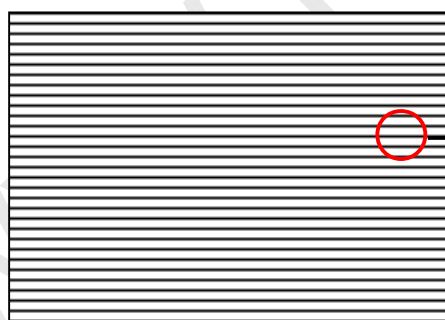
Active Area

b. Black Pattern

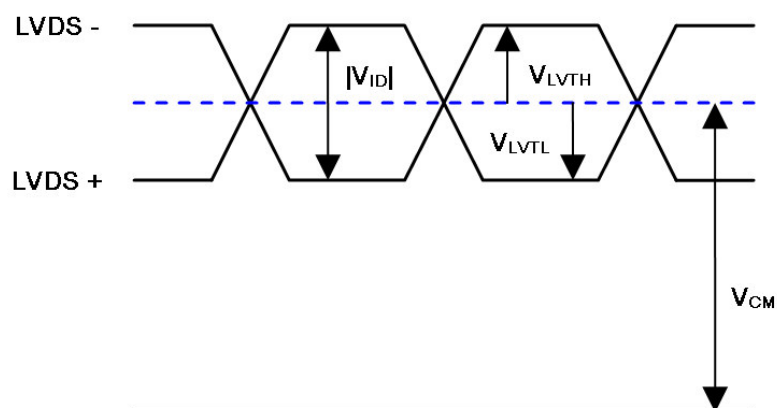


Active Area

c. Horizontal Pattern

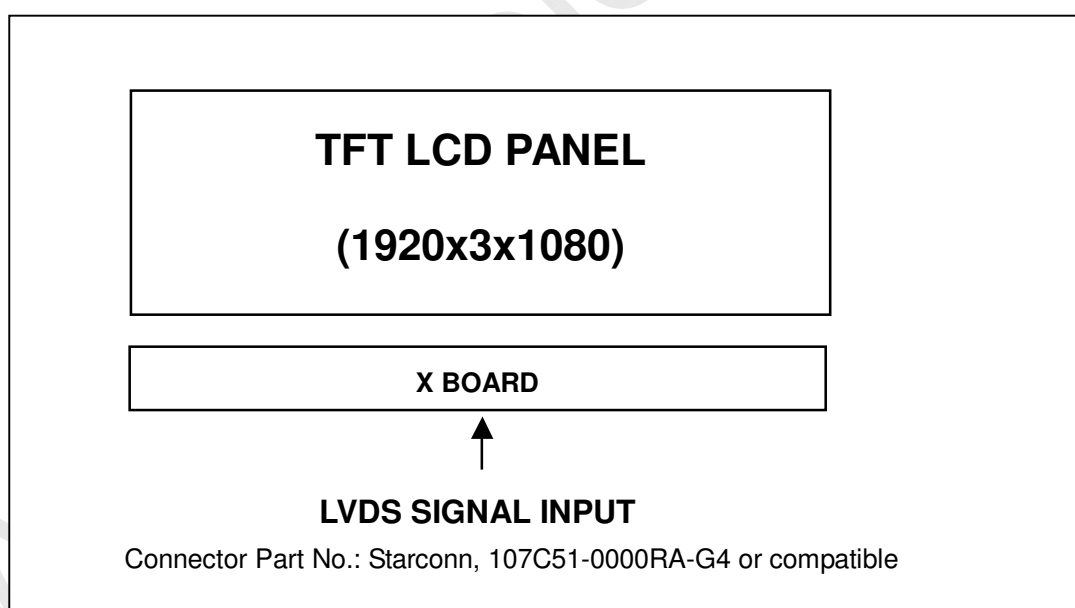


Note (4) The LVDS input characteristics are as follows:



4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



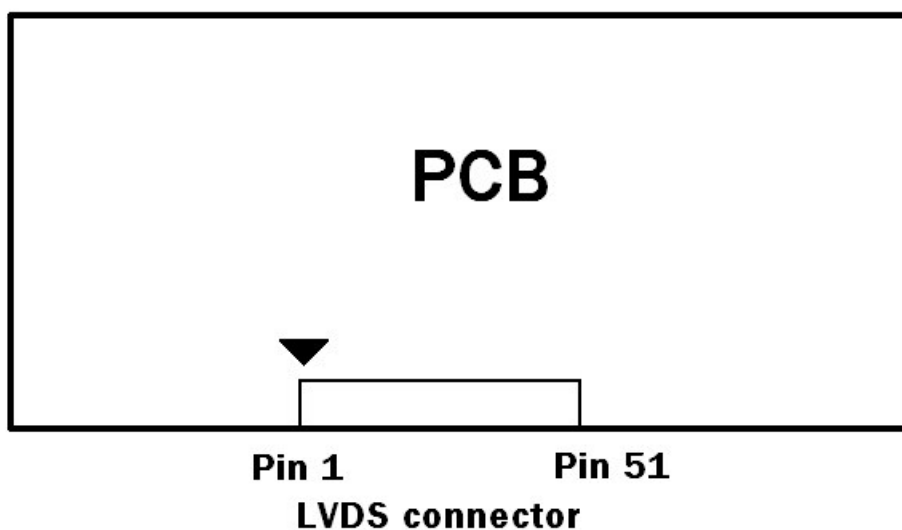
**5. INPUT TERMINAL PIN ASSIGNMENT****5.1 TFT LCD MODULE****CNF1 Connector Pin Assignment**

Pin	Name	Description	Note
1	VCC	+12V power supply	
2	VCC	+12V power supply	
3	VCC	+12V power supply	
4	VCC	+12V power supply	
5	VCC	+12V power supply	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	ORX0-	Odd pixel Negative LVDS differential data input. Channel 0	(1)
11	ORX0+	Odd pixel Positive LVDS differential data input. Channel 0	
12	ORX1-	Odd pixel Negative LVDS differential data input. Channel 1	
13	ORX1+	Odd pixel Positive LVDS differential data input. Channel 1	
14	ORX2-	Odd pixel Negative LVDS differential data input. Channel 2	
15	ORX2+	Odd pixel Positive LVDS differential data input. Channel 2	
16	GND	Ground	
17	OCLK-	Odd pixel Negative LVDS differential clock input	(1)
18	OCLK+	Odd pixel Positive LVDS differential clock input.	
19	GND	Ground	
20	ORX3-	Odd pixel Negative LVDS differential data input. Channel 3	(1)
21	ORX3+	Odd pixel Positive LVDS differential data input. Channel 3	
22	N.C.	No Connection	(3)
23	N.C.	No Connection	
24	GND	Ground	
25	ERX0-	Even pixel Negative LVDS differential data input. Channel 0	(1)
26	ERX0+	Even pixel Positive LVDS differential data input. Channel 0	
27	ERX1-	Even pixel Negative LVDS differential data input. Channel 1	
28	ERX1+	Even pixel Positive LVDS differential data input. Channel 1	
29	ERX2-	Even pixel Negative LVDS differential data input. Channel 2	
30	ERX2+	Even pixel Positive LVDS differential data input. Channel 2	
31	GND	Ground	
32	ECLK-	Even pixel Negative LVDS differential clock input.	(1)
33	ECLK+	Even pixel Positive LVDS differential clock input.	

34	GND	Ground	
35	ERX3-	Even pixel Negative LVDS differential data input. Channel 3	(1)
36	ERX3+	Even pixel Positive LVDS differential data input. Channel 3	
37	N.C.	No Connection	(3)
38	N.C.	No Connection	
39	GND	Ground	
40	N.C.	No Connection	(3)
41	N.C.	No Connection	
42	N.C.	No Connection	
43	N.C.	No Connection	
44	N.C.	No Connection	
45	SELLVDS	High(3.3V) or open for VESA, Low (GND) for JEIDA	(4)(5)
46	N.C.	No Connection	(3)
47	N.C.	No Connection	
48	N.C.	No Connection	
49	N.C.	No Connection	
50	N.C.	No Connection	
51	N.C.	No Connection	

Note (1) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel

Note (2) LVDS connector pin order defined as follows

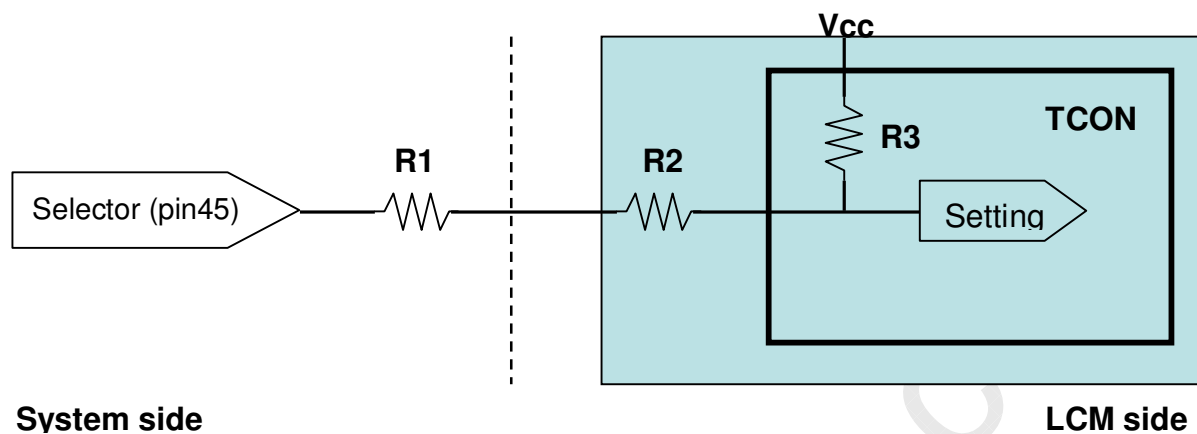


Note (3) Reserved for internal use. Please leave it open.

Note (4) Low: JEIDA LVDS Format (Connect to GND), High or open: VESA Format. (Connect to +3.3V)

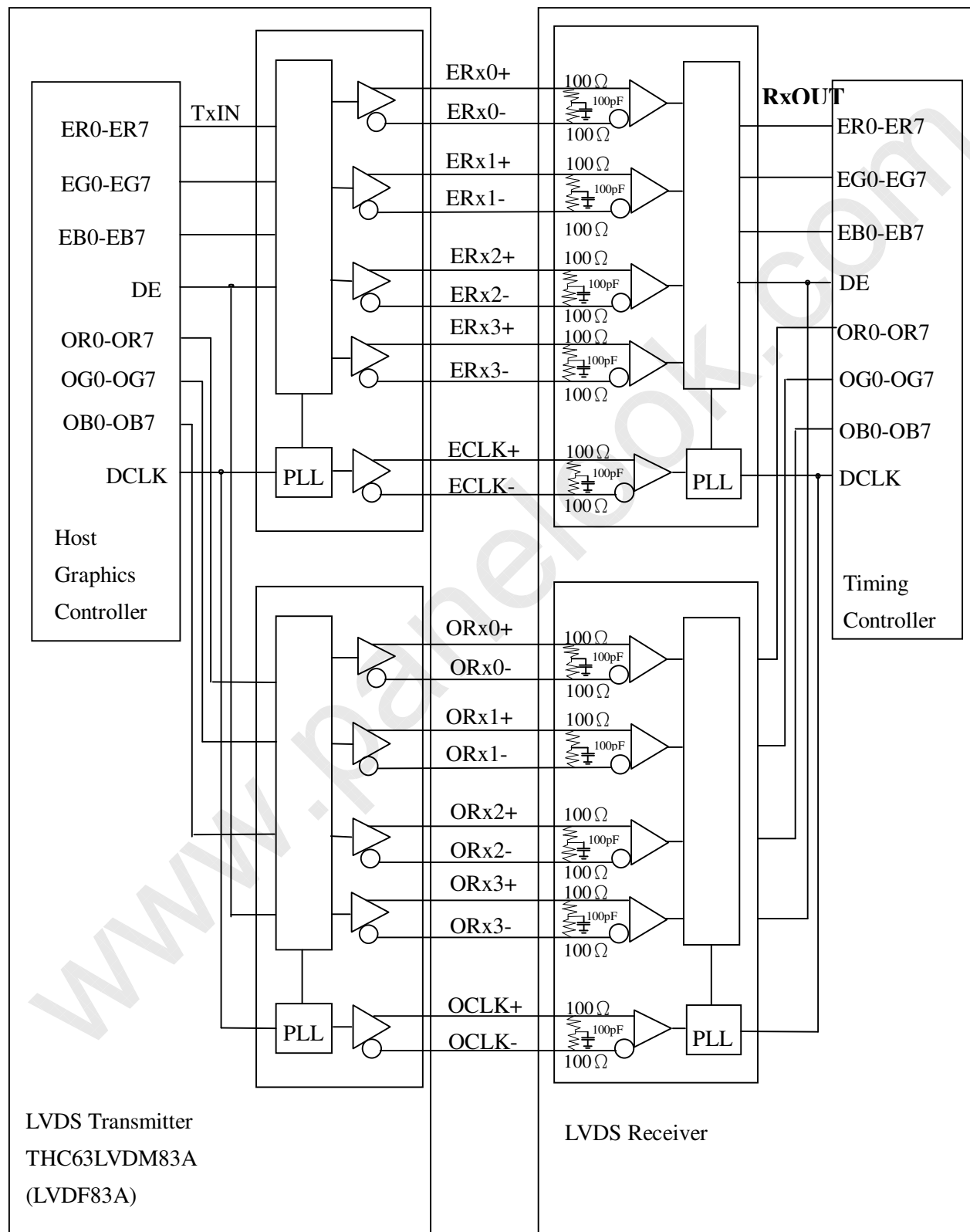
Note (5) LVDS signal pin connected to the LCM side has the following diagram.

R1 in the system side should be less than 1K Ohm. ($R1 < 1K\text{ Ohm}$)



5.2 BLOCK DIAGRAM OF INTERFACE

CNF1



ER0~ER7: Even pixel R data

EG0~EG7: Even pixel G data

EB0~EB7: Even pixel B data

OR0~OR7: Odd pixel R data

OG0~OG7: Odd pixel G data

OB0~OB7: Odd pixel B data

DE: Data enable signal

DCLK: Data clock signal

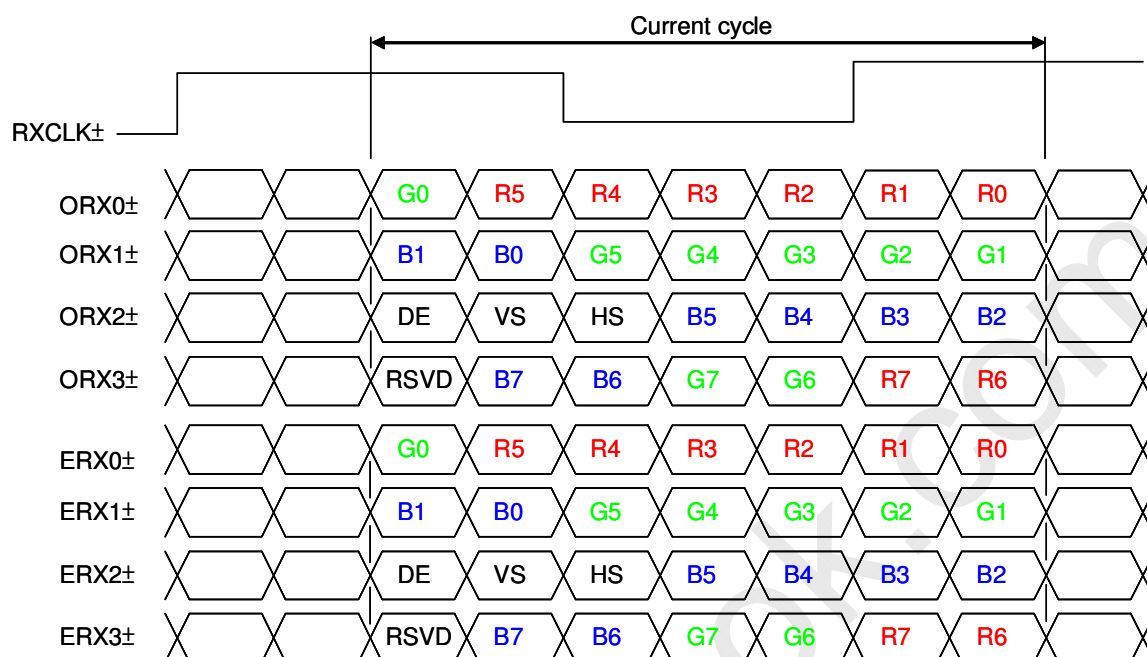
Note (1) The system must have the transmitter to drive the module.

Note (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

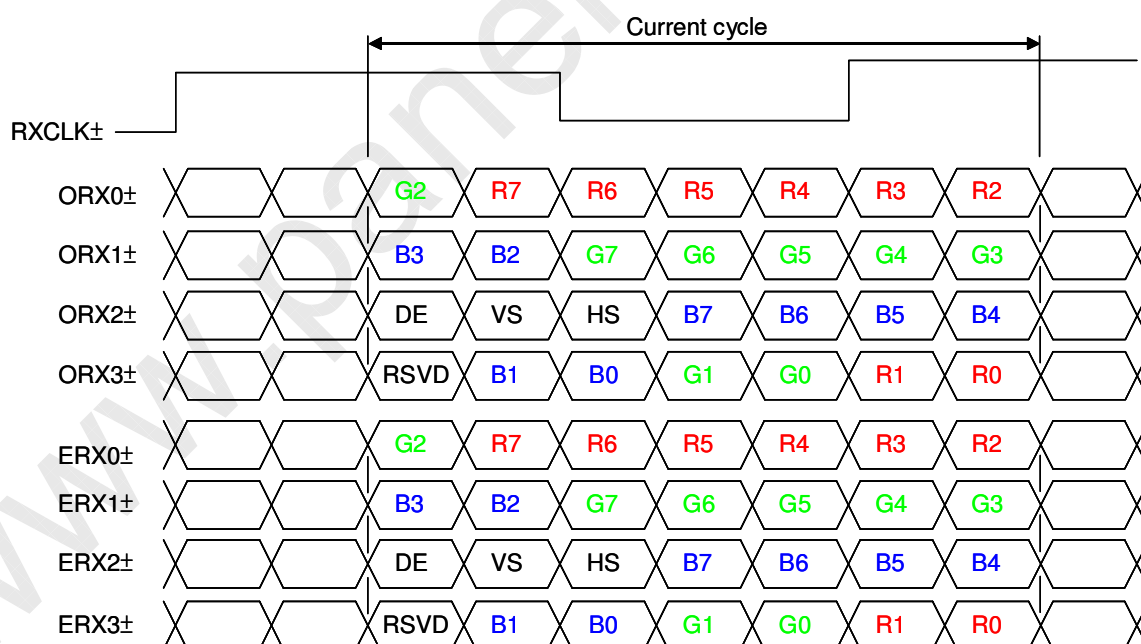
Note (3) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

5.3 LVDS INTERFACE

VESA LVDS format : (SELLVDS pin=H or open)



JEDIA LVDS format : (SELLVDS pin=L)



R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE : Data enable signal

DCCLK : Data clock signal

Notes: (1) RSVD (reserved) pins on the transmitter shall be "H" or "L".

5.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
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	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

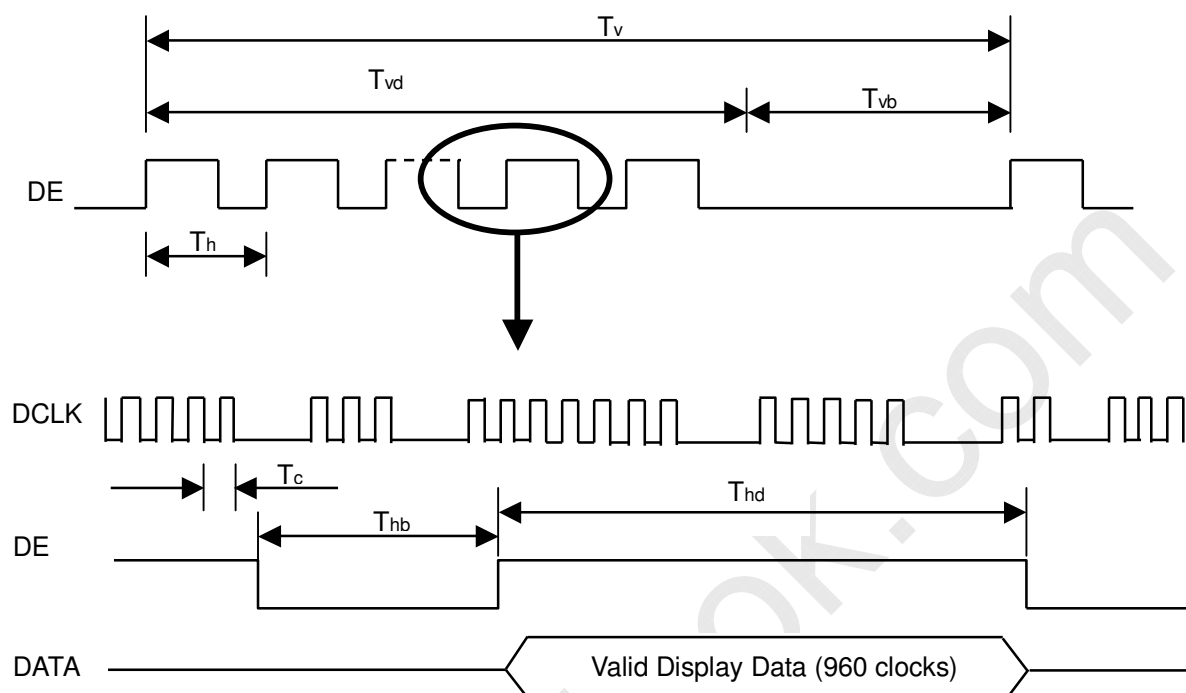
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	60	74.25	80	MHz	
	Input cycle to cycle jitter	T_{rcl}	—	—	200	ps	(3)
	Spread spectrum modulation range	$F_{\text{clkin_mod}}$	$F_{\text{clkin}}-2\%$	—	$F_{\text{clkin}}+2\%$	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}			200	KHz	
LVDS Receiver Data	Setup Time	T_{lvsu}	600	—	—	ps	(5)
	Hold Time	T_{lvhd}	600	—	—	ps	
Vertical Active Display Term	Frame Rate	F_{r5}	47	50	53	Hz	
		F_{r6}	57	60	63	Hz	
	Total	T_{v}	1115	1125	1135	Th	$T_{\text{v}}=T_{\text{vd}}+T_{\text{vb}}$
	Display	T_{vd}	1080	1080	1080	Th	—
	Blank	T_{vb}	35	45	55	Th	—
Horizontal Active Display Term	Total	T_{h}	1050	1100	1150	T_{c}	$T_{\text{h}}=T_{\text{hd}}+T_{\text{hb}}$
	Display	T_{hd}	960	960	960	T_{c}	—
	Blank	T_{hb}	90	140	190	T_{c}	—

Note (1) Please make sure the range of pixel clock has follow the below equation :

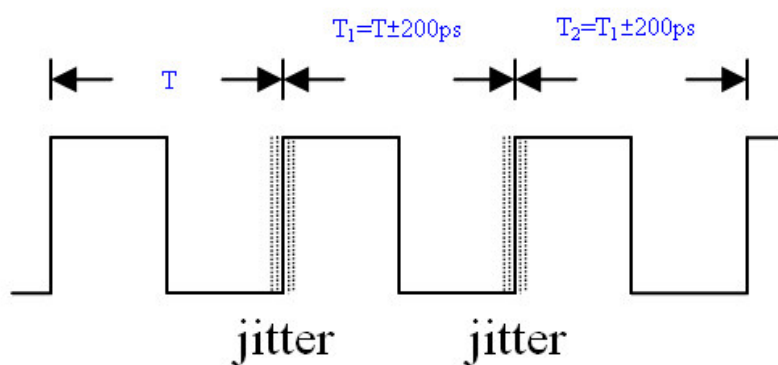
$$F_{\text{clkin}}(\text{max}) \geq F_{\text{r6}} \times T_{\text{v}} \times T_{\text{h}}$$

$$F_{\text{r5}} \times T_{\text{v}} \times T_{\text{h}} \geq F_{\text{clkin}}(\text{min})$$

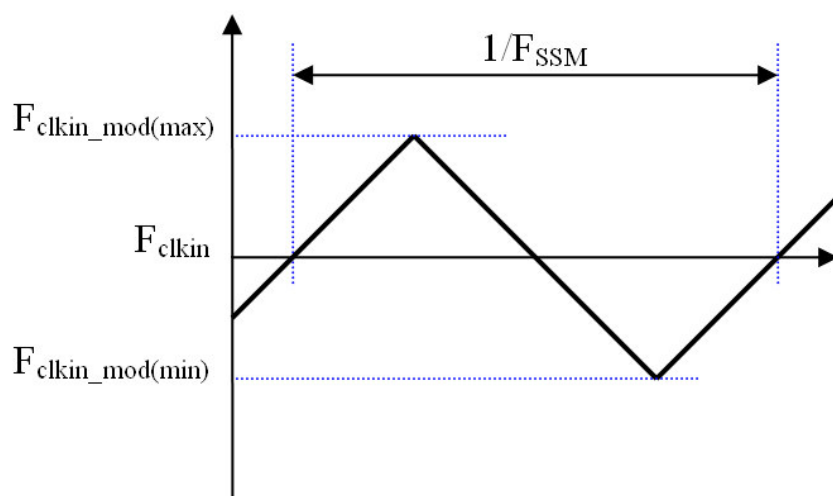
Note (2) This module is operated in DE only mode and please follow the input signal timing diagram below :

INPUT SIGNAL TIMING DIAGRAM

Note (3) The input clock cycle-to-cycle jitter is defined as below figures. $Trcl = |T_1 - T_1|$

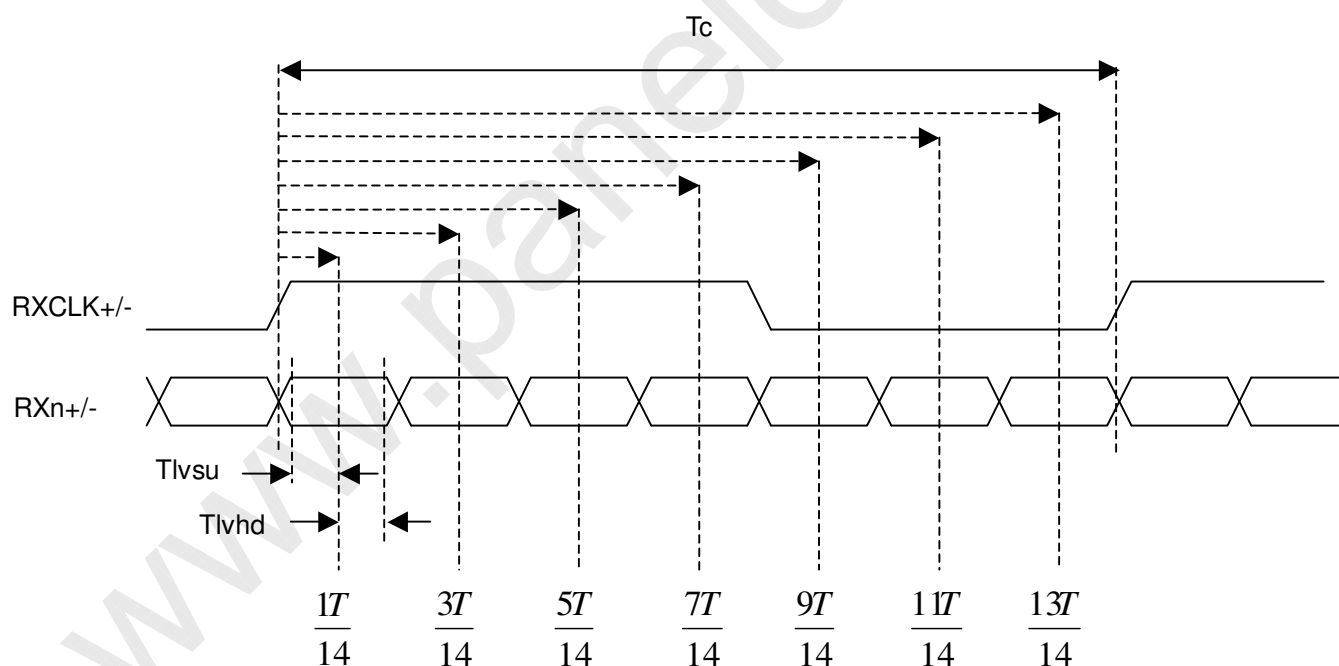


Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



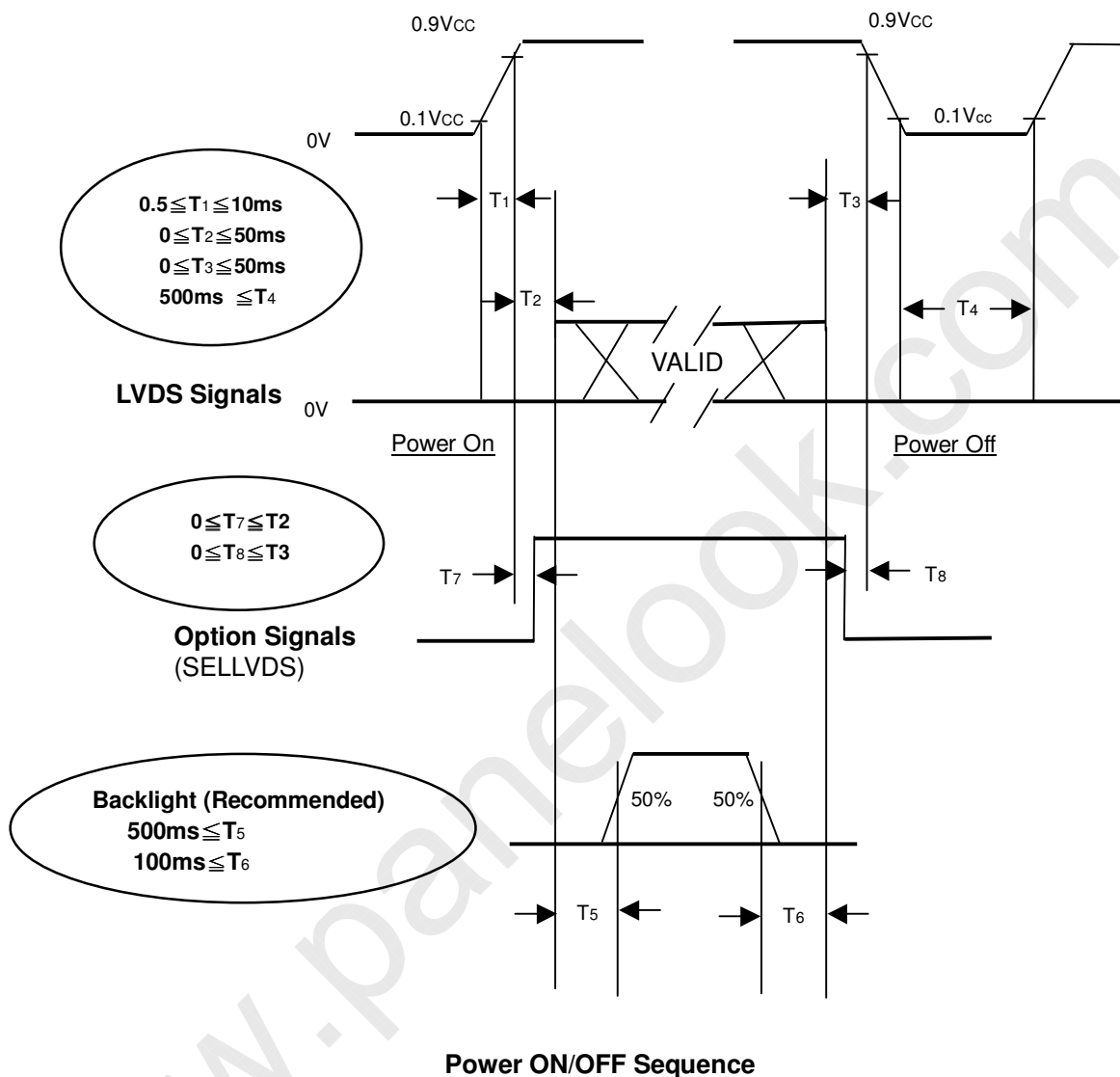
Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

LVDS RECEIVER INTERFACE TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Note (1) The supply voltage of the external system for the module input should follow the definition of V_{CC} .

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of V_{CC} is in off level, please keep the level of input signals on the low or high impedance. If $T_2 < 0$, that maybe cause electrical overstress failure.

Note (4) T_4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V _{CC}	12.0	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	I _L	7.5 ± 0.5	mA
Oscillating Frequency (Inverter)	F _w	40 ± 3	KHz
Vertical Frame Rate	Fr	60	Hz

7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown as below. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (5).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity	Red	Rcx	$\theta_x=0^\circ, \theta_Y=0^\circ$ Viewing Angle at Normal Direction Standard light source “C”	-	0.654	-	-	(0),(5)
		Rcy			0.329		-	
	Green	Gcx			0.275		-	
		Gcy			0.600		-	
	Blue	Bcx			0.147		-	
		Bcy			0.106		-	
	White	Wcx			0.320		-	
		Wcy			0.365		-	
Center Transmittance		T%	$\theta_x=0^\circ, \theta_Y=0^\circ$	-	6.1	-	%	(1),(7)
Contrast Ratio		CR	with CMI module		800	-		(1),(3)
Response Time		T _R	$\theta_x=0^\circ, \theta_Y=0^\circ$	-	1.4		ms	(1),(4)
		T _F	with CMI Module@60Hz	-	3.6		ms	
White Variation		δW	$\theta_x=0^\circ, \theta_Y=0^\circ$ with CMI module	-	-	1.3	-	(1),(6)
Viewing Angle	Horizontal	θ _{x+}	CR≥10 With CMI module		80		Deg.	(1),(2)
		θ _{x-}			80			
	Vertical	θ _{Y+}			80			
		θ _{Y-}			70			

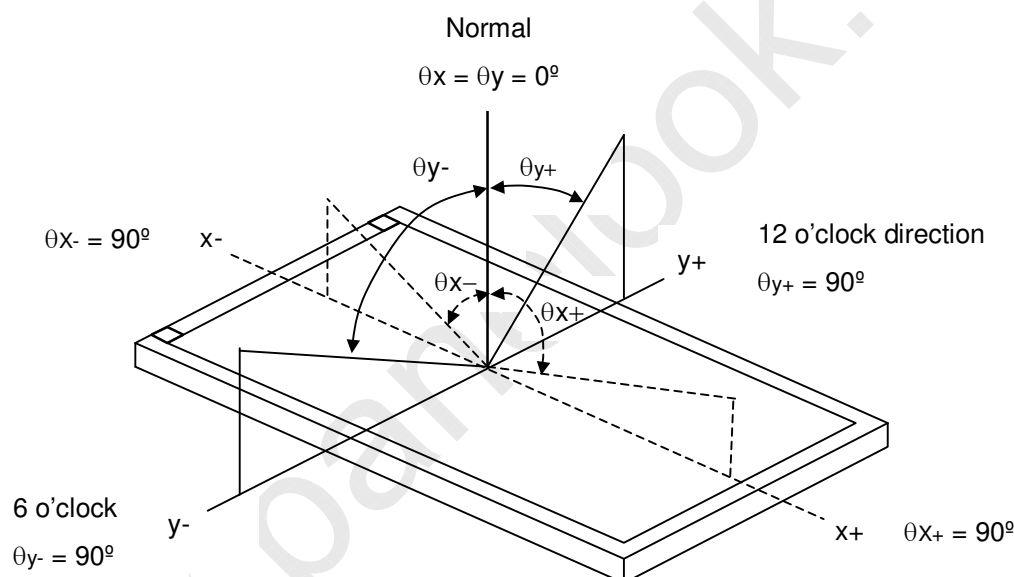
Note (0) Light source is the standard light source "C" which is defined by CIE and driving voltage are based on suitable gamma voltages. The calculating method is as following :

1. Measure Module's and BLU's spectrum. White is without signal input and R,G,B are with signal input. BLU (for V260H1-L03) is supplied by CMI.
2. Calculate cell's spectrum.
3. Calculate cell's chromaticity by using the spectrum of standard light source "C".

Note (1) Light source is the BLU which is supplied by CMI and driving voltage are based on suitable gamma voltages.

Note (2) Definition of Viewing Angle (θ_x , θ_y):

Viewing angles are measured by Autronic Conoscope Cono-80



Note (3) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

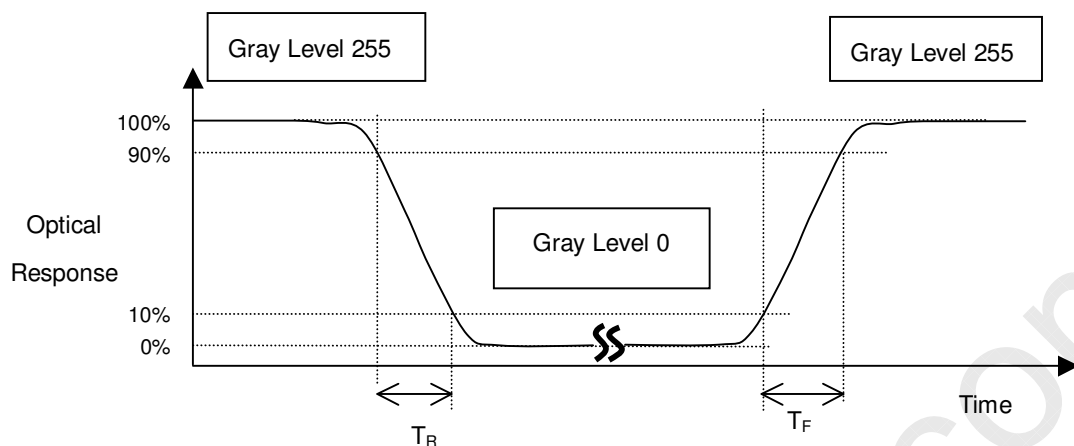
$$\text{Contrast Ratio (CR)} = L_{255} / L_0$$

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

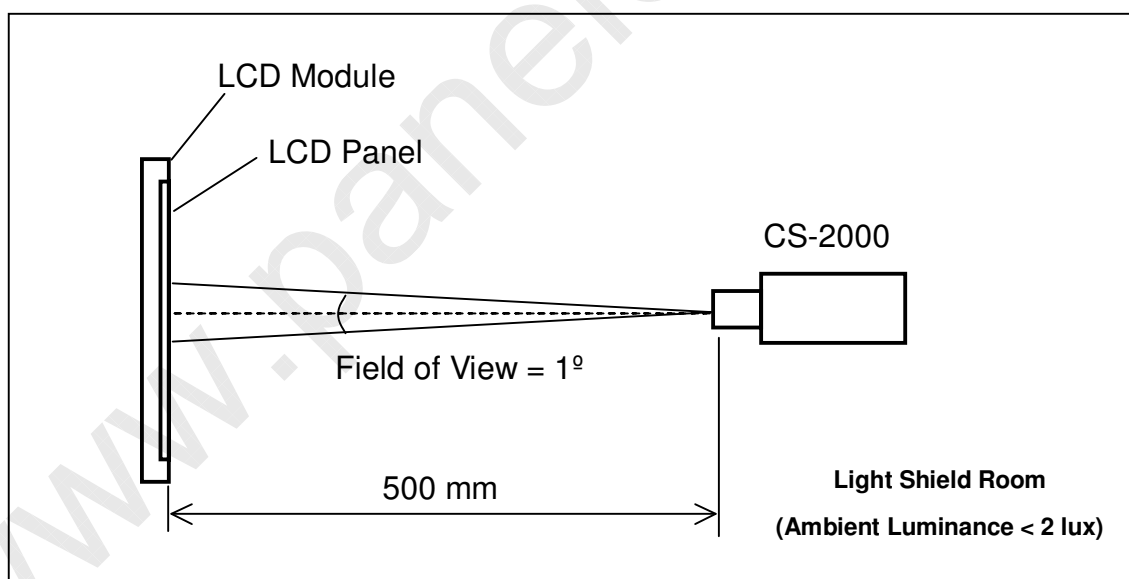
CR = CR (X), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (4) Definition of Response Time (T_R , T_F):



Note (5) Measurement Setup:

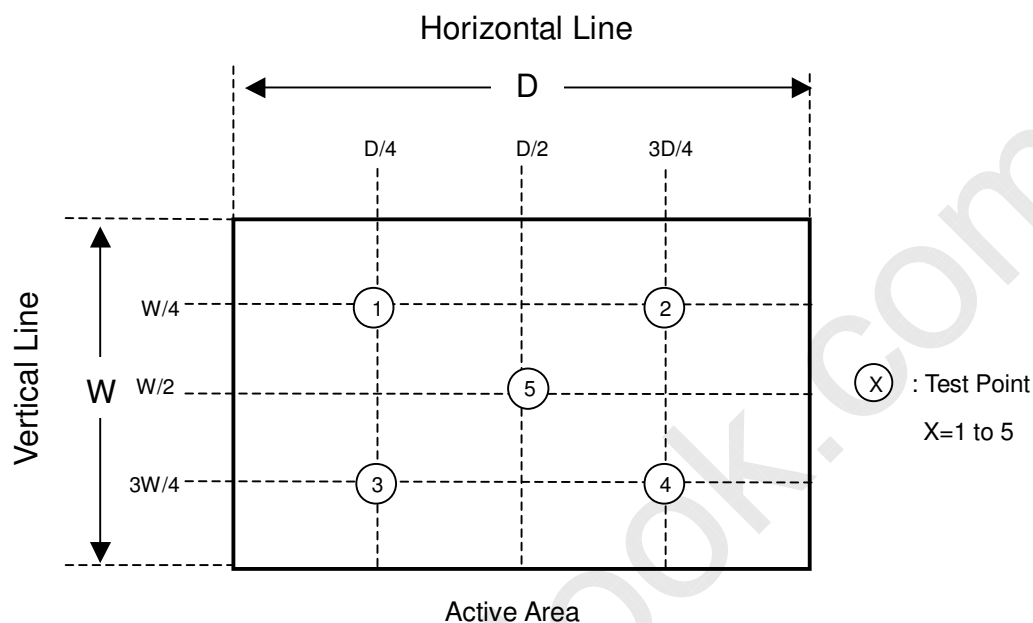
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement (CS-1000 or CA-210 calibrated by CS-2000) should be executed after lighting backlight for 1 hour in a windless room.



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

$$\delta W = \text{Maximum} [L(1), L(2), L(3), L(4), L(5)] / \text{Minimum} [L(1), L(2), L(3), L(4), L(5)]$$



Note (7) Definition of Transmittance (T%) :

Module is without signal input.

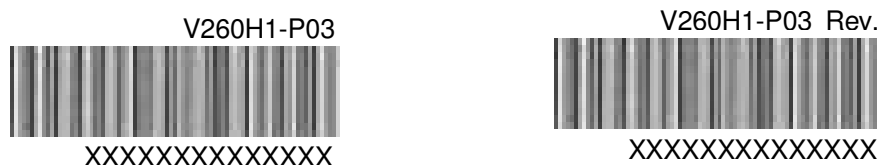
$$\text{Transmittance} = \frac{\text{Luminance of LCD module}}{\text{Luminance of backlight}} * 100\%$$

8. DEFINITION OF LABELS

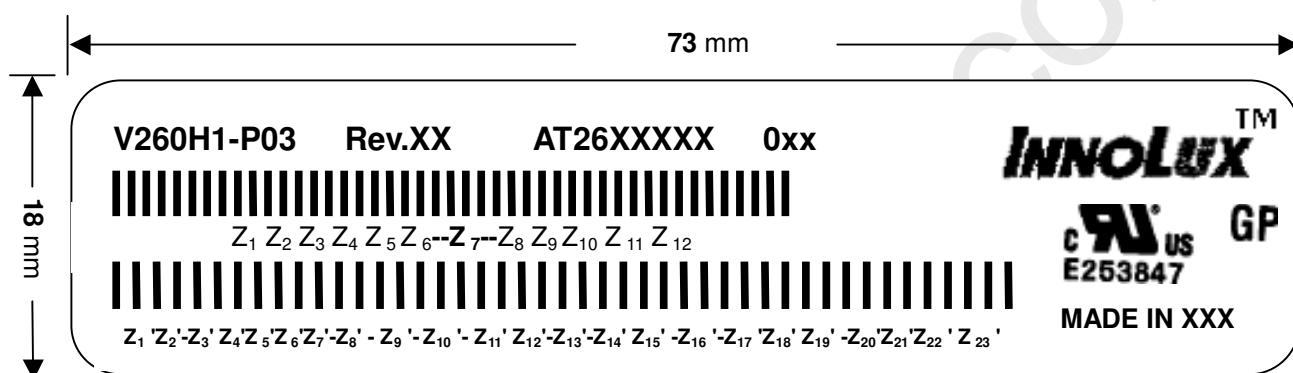
8.1 OPEN CELL LABEL

The barcode nameplate is pasted on each open cell as illustration for CMI internal control.

8.1.1 FOR TAINAN LCM, NAN-HAI LCM, NINGBO LCM's LABEL TYPE

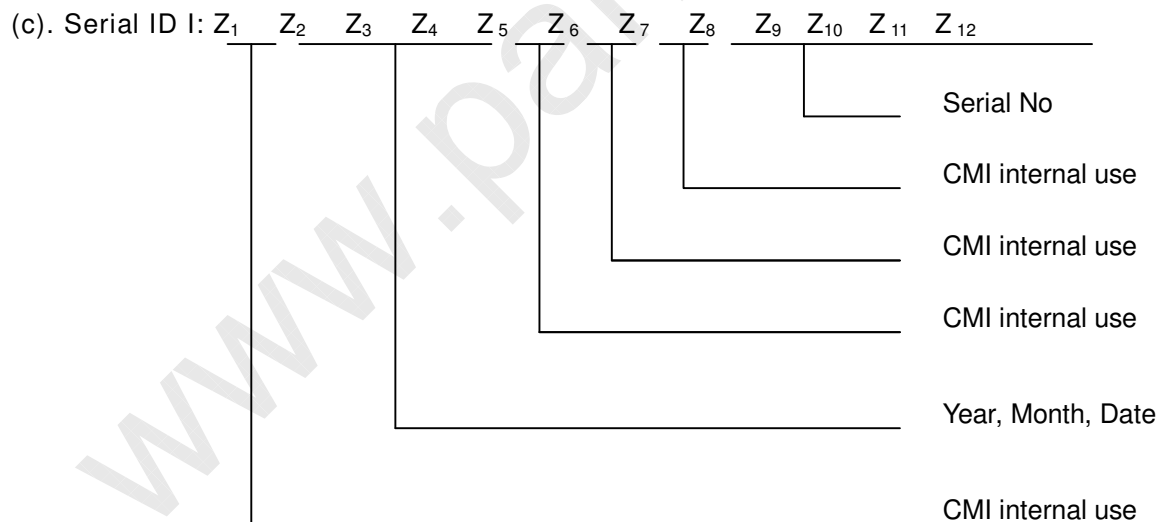


8.1.2 FOR JHUNAN T2 LCM's LABEL TYPE



(a). Model Number: V260H1-P03

(b). Rev.: XX



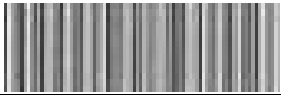
Serial ID includes the information as below:

1. Manufactured Date: Year: 0~9, for 2010~2019
2. Month: 1~9 & A~C for Jan. ~ Dec.
3. Date: 1~9 & A~Z (exclude I, O, Q, U) for 1st~31th
4. Serial No: Module manufacture sequence no

8.2 CARTON LABEL

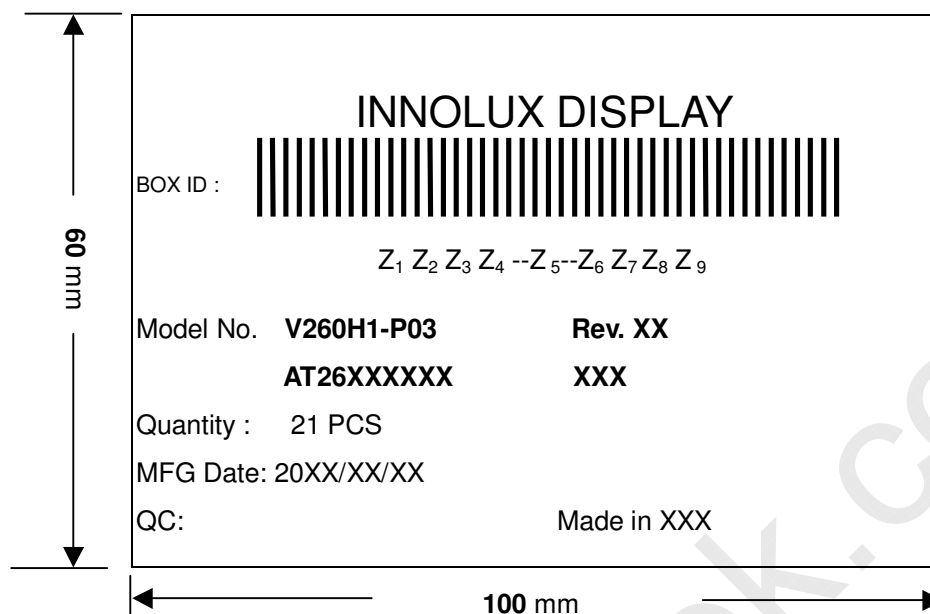
The barcode nameplate is pasted on each box as illustration, and its definitions are as following explanation

8.2.1 FOR TAINAN LCM, NAN-HAI LCM, NINGBO LCM's CARTON LABEL TYPE

P.O. NO.	_____
Parts ID.	_____
Carton ID.	
	XXXXXXXXXXXXXXXX
Quantities	21
Made in XXXXXX	

- (a) Model Name: V260H1– P03
- (b) Carton ID: CMI internal control
- (c) Quantities: 21

8.2.2 FOR JHUNAN T2 LCM's CARTON LABEL TYPE

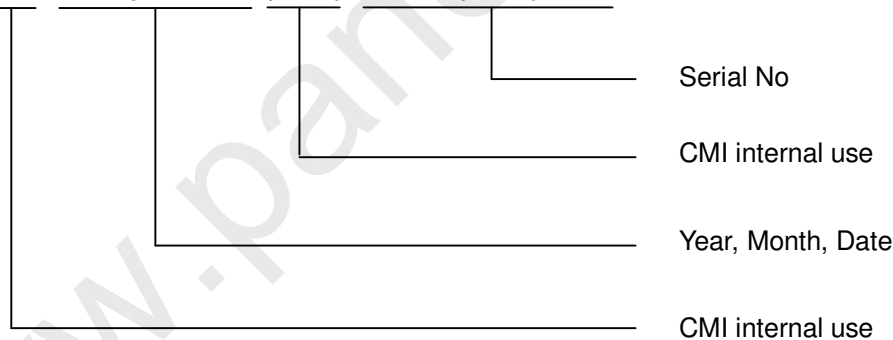


(a). Model Number: V260H1-P03

(b). Rev.: XX

(c). Packing quantity: 21 PCS

(d). Serial ID: Z₁ Z₂ Z₃ Z₄ Z₅ Z₆ Z₇ Z₈ Z₉



Serial ID includes the information as below:

(a). Manufactured Date: Year: 0~9, for 2010 ~2019

Month: 1~9 & A~C for Jan. ~ Dec.

Date: 1~9 & A~Z (exclude I, O, Q, U) for 1st~31th

(b). Serial No: Module packing sequence no.

9. PACKAGING

9.1 PACKING SPECIFICATIONS

- (1) 21PCS LCD TV Panels / 1 Box
- (2) Box dimensions : 812 (L) X 572 (W) X 277 (H)
- (3) Weight : approximately 27.5 Kg

9.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method

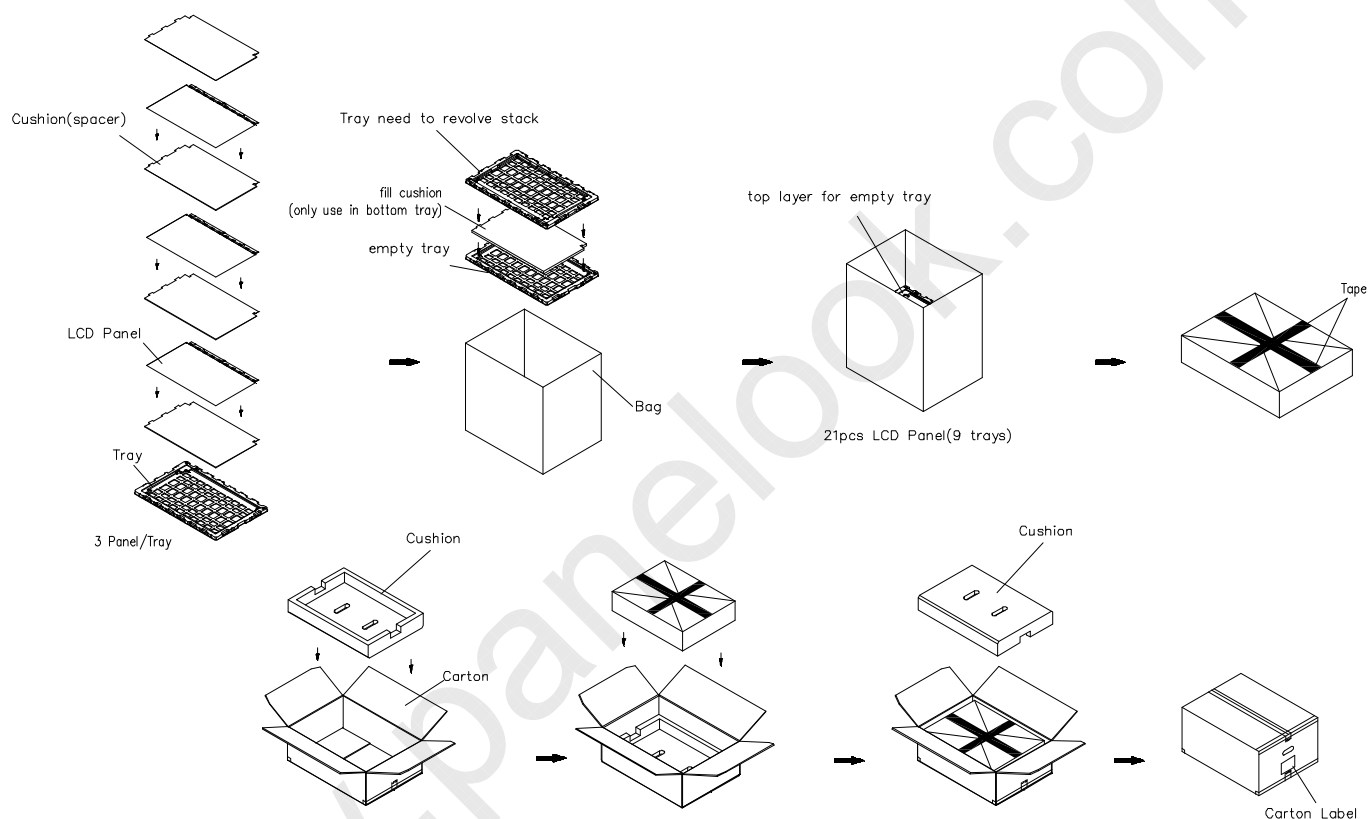
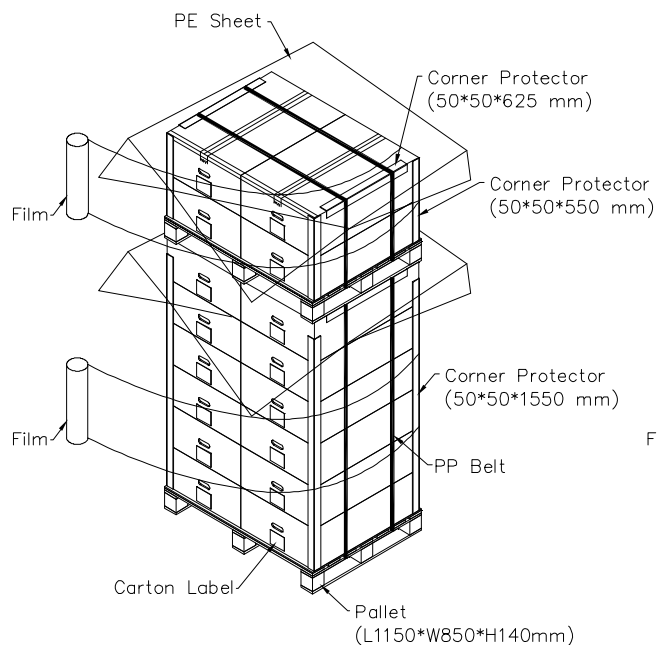


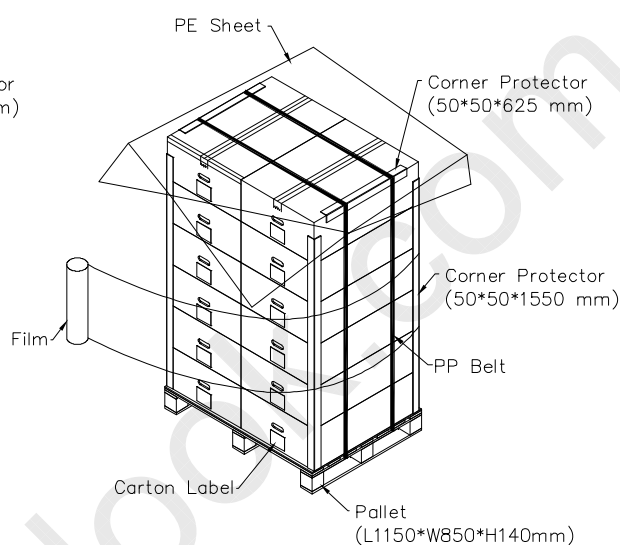
Figure. 9-1 packing method



Sea / Land Transportation
(40ft HQ Container)



Sea / Land Transportation
(40ft Container)



Air Transportation

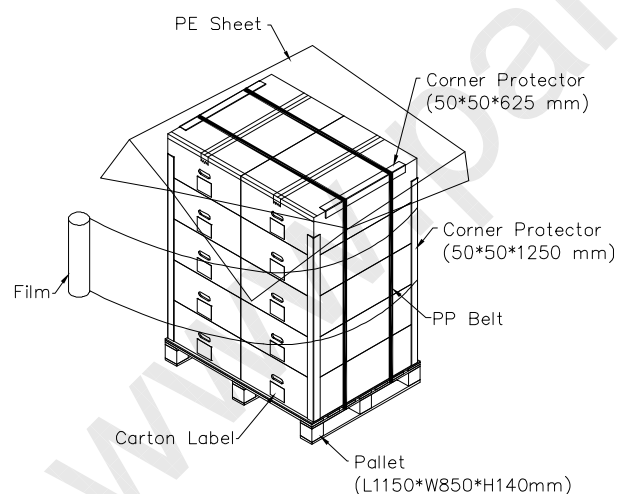


Figure. 9-2 packing method



10. PRECAUTIONS

10.1 ASSEMBLY AND HANDLING PRECAUTIONS

- (1) Do not apply rough force such as bending or twisting to the product during assembly.
- (2) To assemble backlight or install module into user's system can be only in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- (3) It's not permitted to have pressure or impulse on the module because the LCD panel will be damaged.
- (4) Always follow the correct power sequence when the product is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.
- (5) Do not pull the I/F connector in or out while the module is operating.
- (6) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- (7) It is dangerous that moisture come into or contacted the product, because moisture may damage the product when it is operating.
- (8) High temperature or humidity may reduce the performance of module. Please store this product within the specified storage conditions.
- (9) When ambient temperature is lower than 10°C may reduce the display quality. For example, the response time will become slowly.

10.2 SAFETY PRECAUTIONS

- (1) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- (2) After the product's end of life, it is not harmful in case of normal operation and storage.



Issued Date: 23, Jul. 2010

Model No.: V260H1 – P03

Approval

11. MECHANICAL CHARACTERISTICS

