



# TFT LCD Approval Specification

## MODEL NO.: V260H1 – L01

Customer: \_\_\_\_\_

Approved by: \_\_\_\_\_

Note:

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**CHI MEI**  
OPTOELECTRONICS CORP.

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Model No.: V260H1 - L01

**Approval****REVISION HISTORY**

Version	Date	Page (New)	Section	Description
Ver 2.0	Feb. 11,'10	All	All	Approval Specification was first issued.

## 1. GENERAL DESCRIPTION

### 1.1 OVERVIEW

V260H1- L01 is a TFT Liquid Crystal Display module with 4U-CCFL Backlight unit and 2ch-LVDS interface. The display diagonal is 26". This module supports 1920 x 1080 Full HDTV format and can display 16.7M colors (8-bit/color). The inverter module for backlight is built-in.

### 1.2 FEATURES

- Optimized Brightness 400nits
- Contrast Ratio 800:1
- Fast Response Time 5ms
- Color Saturation NTSC 72%
- Full HDTV (1920 x 1080 pixels) resolution, true HDTV format
- DE (Data Enable) Only Mode
- LVDS (Low Voltage Differential Signaling) Interface
- Viewing Angle: 160(H)/150(V) (CR>10) TN Technology
- Color Reproduction (Nature Color)

### 1.3 APPLICATION

- TFT LCD TVs
- Optimized Brightness, Multi-Media Displays

### 1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	576 (H) x 324 (V) (26" Diagonal)	mm	(1)
Bezel Opening Area	580.8 (H) x 328.8 (V)	mm	
Driver Element	a-si TFT Active Matrix	—	
Pixel Number	1920 x R.G.B. x 1080	pixel	
Pixel Pitch (Sub Pixel)	0.100 (H) x 0.300 (V)	mm	
Pixel Arrangement	RGB Vertical Stripe	—	
Display Colors	16.7M	color	
Display Operation Mode	Transmissive Mode / Normally White	—	
Surface Treatment	Anti-Glare Coating (Haze 25%) Hard Coating (3H)	—	

### 1.5 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	625	626	627	mm
	Vertical(V)	372	373	374	mm
	Depth(D)	31	32	33	mm
Weight	-	3727	-	g	To Rear

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

## 2. ABSOLUTE MAXIMUM RATINGS

### 2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T <sub>ST</sub>	-20	+60	°C	(1)
Operating Ambient Temperature	T <sub>OP</sub>	0	+50	°C	(1), (2)
Shock (Non-Operating)	S <sub>NOP</sub>	—	50	G	(3), (5)
Vibration (Non-Operating)	V <sub>NOP</sub>	—	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. ( $T_a \leq 40$  °C).

(b) Wet-bulb temperature should be 39 °C Max. ( $T_a > 40$  °C).

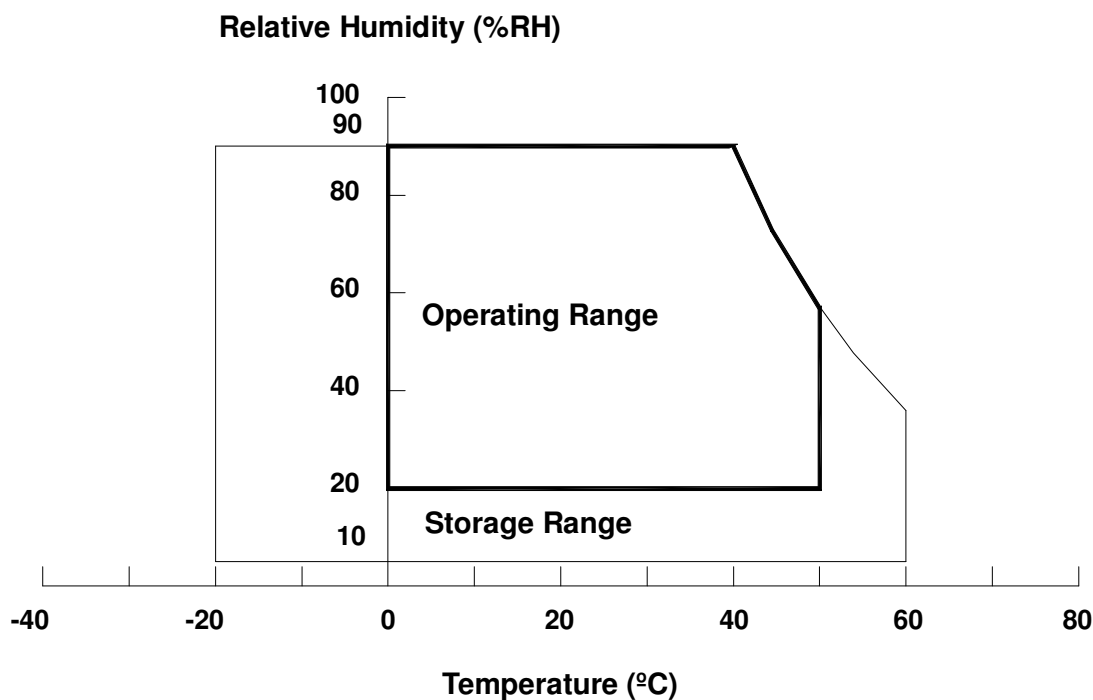
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for  $\pm X$ ,  $\pm Y$ ,  $\pm Z$ .

Note (4) 10 ~ 200 Hz, 30 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



## 2.2 ELECTRICAL ABSOLUTE RATINGS

### 2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V <sub>CC</sub>	-0.3	13.5	V	(1)
Input Signal Voltage	V <sub>IN</sub>	-0.3	3.6	V	

### 2.2.2 BACKLIGHT UNIT

Item	Symbol	Test Condition	Min.	Type	Max.	Unit	Note
Lamp Voltage	V <sub>W</sub>	Ta = 25 °C	—	—	3000	V <sub>RMS</sub>	
Power Supply Voltage	V <sub>BL</sub>	—	0	—	30	V	(1)
Control Signal Level	—	—	-0.3	—	7	V	(2), (3)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Functional operation should be restricted to the conditions described under normal operating conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals includes Backlight On/Off Control, Internal PWM Control and External PWM Control.

### 3. ELECTRICAL CHARACTERISTICS

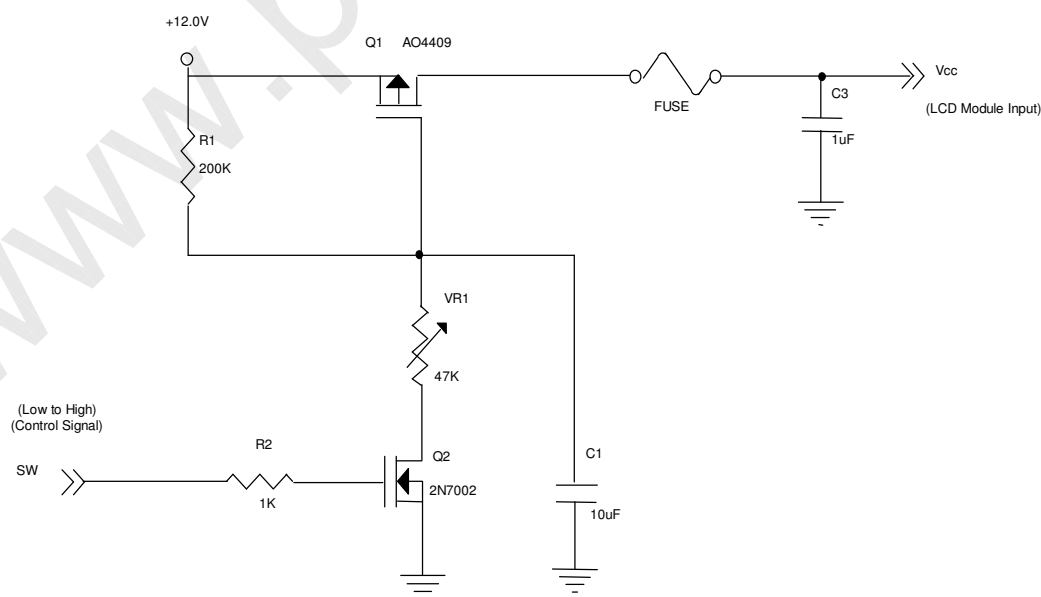
#### 3.1 TFT LCD MODULE

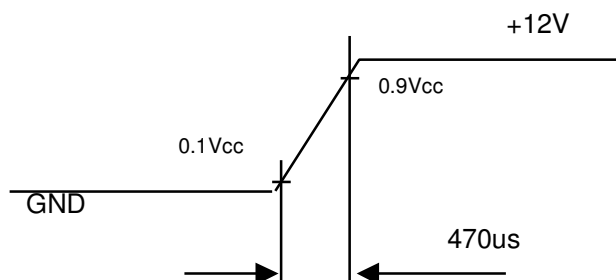
Ta = 25 ± 2 °C

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V <sub>CC</sub>	10.8	12	13.2	V	(1)
Rush Current		I <sub>RUSH</sub>	—	—	3.0	A	(2)
Power Supply Current	White Pattern	—	—	0.29	—	A	(3)
	Horizontal Stripe	—	—	0.45	—	A	
	Black Pattern	—	—	0.46	0.55	A	
LVDS interface	Differential Input High Threshold Voltage	V <sub>LVTH</sub>	+100	—	—	mV	(4)
	Differential Input Low Threshold Voltage	V <sub>LVTL</sub>	—	—	-100	mV	
	Common Input Voltage	V <sub>CM</sub>	1.0	1.2	1.4	V	
	Differential input voltage	V <sub>ID</sub>	200	—	600	mV	
	Terminating Resistor	R <sub>T</sub>	—	100	—	ohm	
CMOS interface	Input High Threshold Voltage	V <sub>IH</sub>	2.7	—	3.3	V	
	Input Low Threshold Voltage	V <sub>IL</sub>	0	—	0.7	V	

Note (1) The module should be always operated within above ranges.

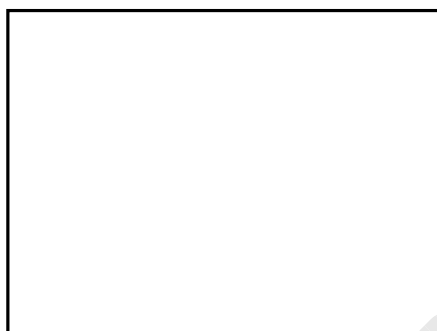
Note (2) Measurement Conditions:



**Vcc rising time is 470us**

Note (3) The specified power supply current is under the conditions at  $V_{cc} = 12\text{ V}$ ,  $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$ ,  $f_v = 60\text{ Hz}$ , whereas a power dissipation check pattern below is displayed.

a. White Pattern



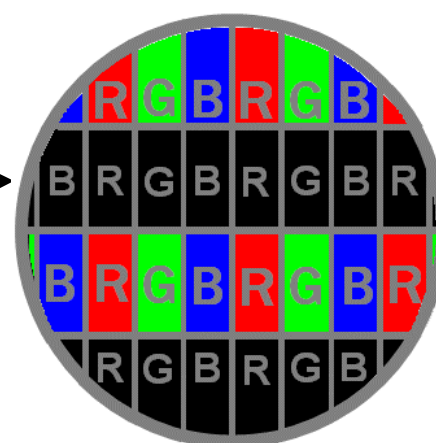
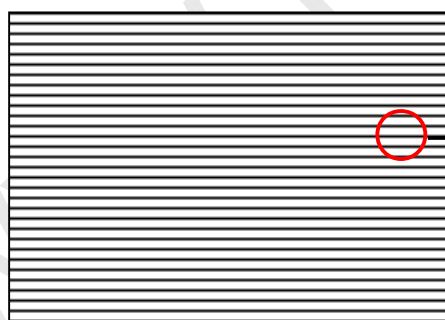
Active Area

b. Black Pattern



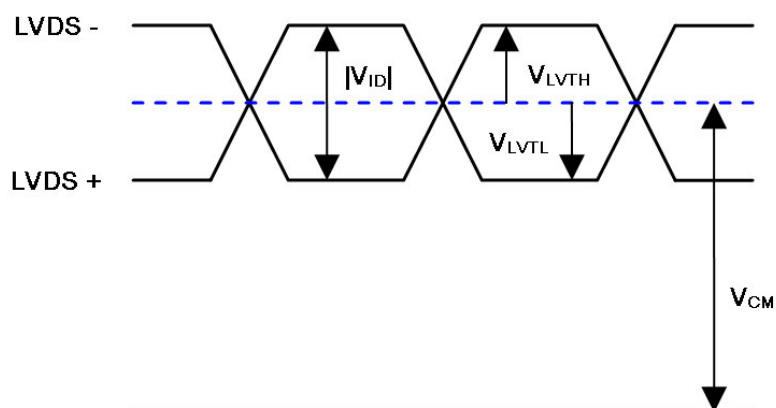
Active Area

c. Horizontal Pattern





Note (4) The LVDS input characteristics are as follows:



### 3.2 BACKLIGHT UNIT

#### 3.2.1 CCFL (Cold Cathode Fluorescent Lamp) CHARACTERISTICS (Ta = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Voltage	$V_W$	-	1410	-	$V_{RMS}$	$I_L = 7.5mA$
Lamp Current(HI-Side)	$I_L$	-	7.5	-	$mA_{RMS}$	-
Lamp Starting Voltage	$V_S$	-	-	2270	$V_{RMS}$	(1), Ta = 0 °C
		-	-	1890	$V_{RMS}$	(1), Ta = 25 °C
Operating Frequency	$F_O$	40	-	80	KHz	(2)
Lamp Life Time	$L_{BL}$	50,000	-	-	Hrs	(3)

#### 3.2.2 INVERTER CHARACTERISTICS (Ta = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Total Power Consumption	$P_{255}$	-	42	46	W	(5), (6), $I_L = 7.5mA$
Power Supply Voltage	$V_{BL}$	22.8	24	25.2	$V_{DC}$	
Power Supply Current	$I_{BL}$	-	1.75	1.92	A	Non Dimming
Input Ripple Noise	-	-	-	912	$mV_{P-P}$	$V_{BL} = 22.8V$
Oscillating Frequency	$F_W$	55	58	61	kHz	(3)
Dimming frequency	$F_B$	150	160	170	Hz	
Minimum Duty Ratio	$D_{MIN}$	10	20	-	%	(7)

Note (1) Lamp current is measured by utilizing AC current probe and its value is average by measuring master and slave board.

Note (2) The lamp starting voltage  $V_S$  should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

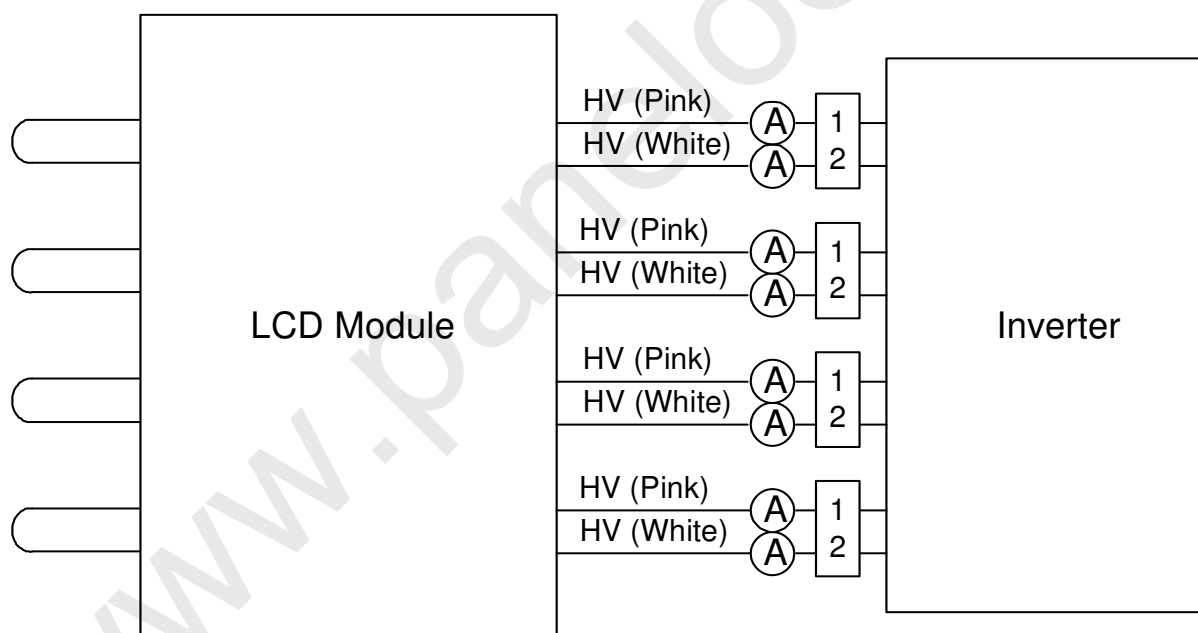
Note (3) The lamp frequency may produce interference with horizontal synchronous frequency of the display input signals, and it may result in line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) The life time of a lamp is defined as when the brightness is larger than 50% of its original value and the effective discharge length is longer than 80% of its original length (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at the center point of lamp.) as the time in which it continues to operate under the condition at  $T_a = 25 \pm 2^\circ\text{C}$  and  $I_L = 7.0 \sim 8.0\text{mA}$ .

Note (5) The power supply capacity should be higher than the total inverter power consumption  $P_{BL}$ . Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when inverter dimming.

Note (6) The measurement condition of Max. value is based on 26" backlight unit under input voltage 24V, average lamp current 7.8 mA and lighting 30 minutes later.

Note (7) 10% minimum duty ratio is only valid for electrical operation



### 3.2.3 INVERTER INTERFACE CHARACTERISTICS

Parameter		Symbol	Test Condition	Value			Unit	Note
				Min.	Typ.	Max.		
On/Off Control Voltage	ON	$V_{BLON}$	—	2.0	—	5.0	V	
	OFF		—	0	—	0.8	V	
Internal PWM Control Voltage	MAX	$V_{IPWM}$	—	3.0	3.15	3.3	V	Maximum duty ratio
	MIN			—	0	—	V	Minimum duty ratio
External PWM Control Voltage	HI	$V_{EPWM}$	—	2.0	—	5.0	V	Duty on
	LO			0	—	0.8	V	Duty off
Error Signal	Error	—	—	Open Collector			V	Abnormal
				0	—	0.8	V	Normal
VBL Rising Time	$Tr1$	—	—	30	—	—	ms	10%-90% $V_{BL}$
VBL Falling Time	$Tf1$	—	—	30	—	—	ms	
Control Signal Rising Time	$Tr$	—	—	—	—	100	ms	
Control Signal Falling Time	$Tf$	—	—	—	—	100	ms	
PWM Signal Rising Time	$T_{PWMR}$	—	—	—	—	50	us	
PWM Signal Falling Time	$T_{PWMF}$	—	—	—	—	50	us	
Input impedance	$R_{IN}$	—	—	1	—	—	MΩ	
PWM Delay Time	$T_{PWM}$	—	—	100	—	—	ms	
BLON Delay Time	$T_{on}$	—	—	300	—	—	ms	
	$T_{on1}$	—	—	300	—	—	ms	
BLON Off Time	$T_{off}$	—	—	300	—	—	ms	

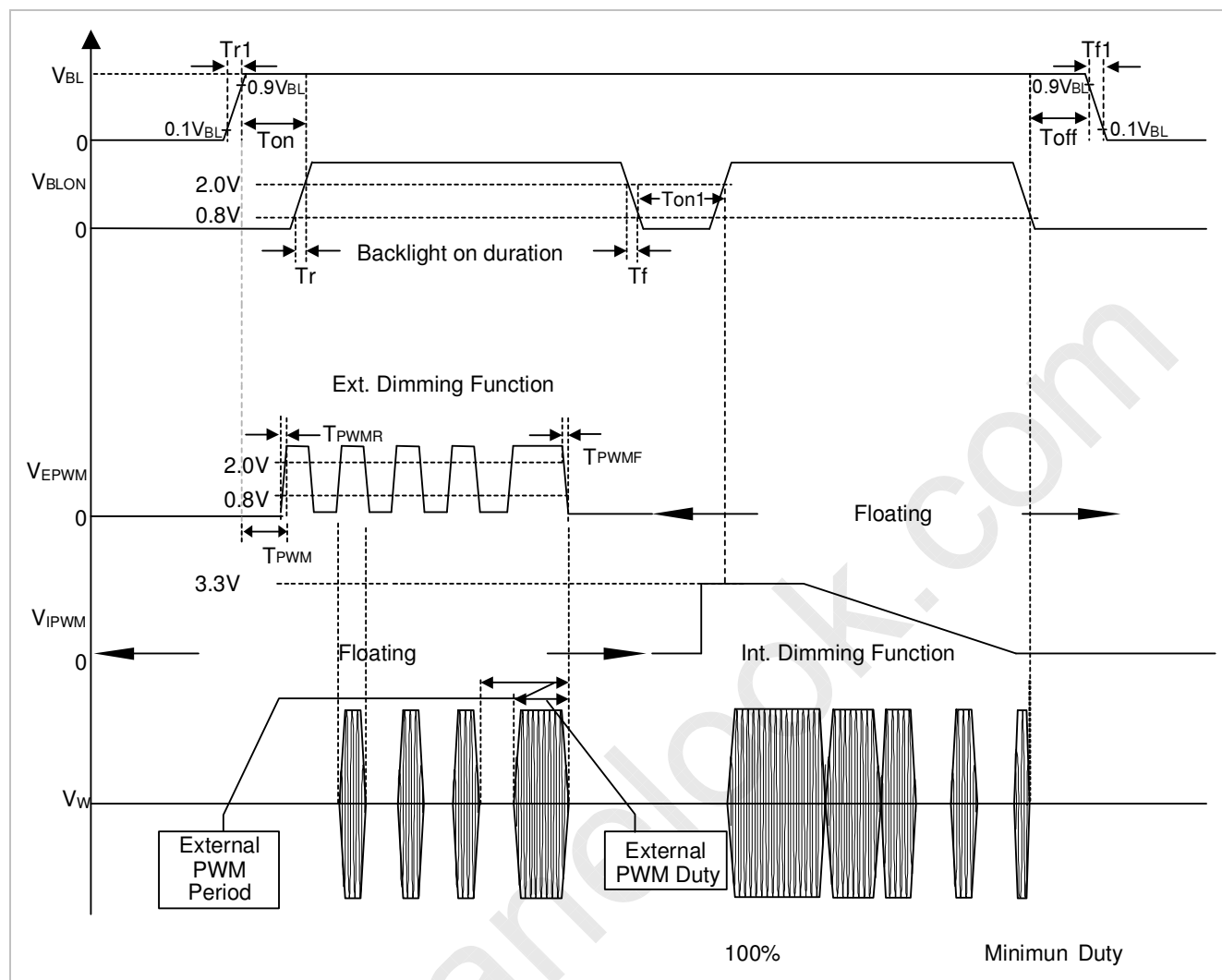
Note (1) The Dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the internal/external PWM signal during backlight turn on period.

Note (2) The power sequence and control signal timing are shown in the following figure. For a certain reason, the inverter has a possibility to be damaged with wrong power sequence and control signal timing.

Note (3) While system is turned ON or OFF, the power sequences must follow as below descriptions:

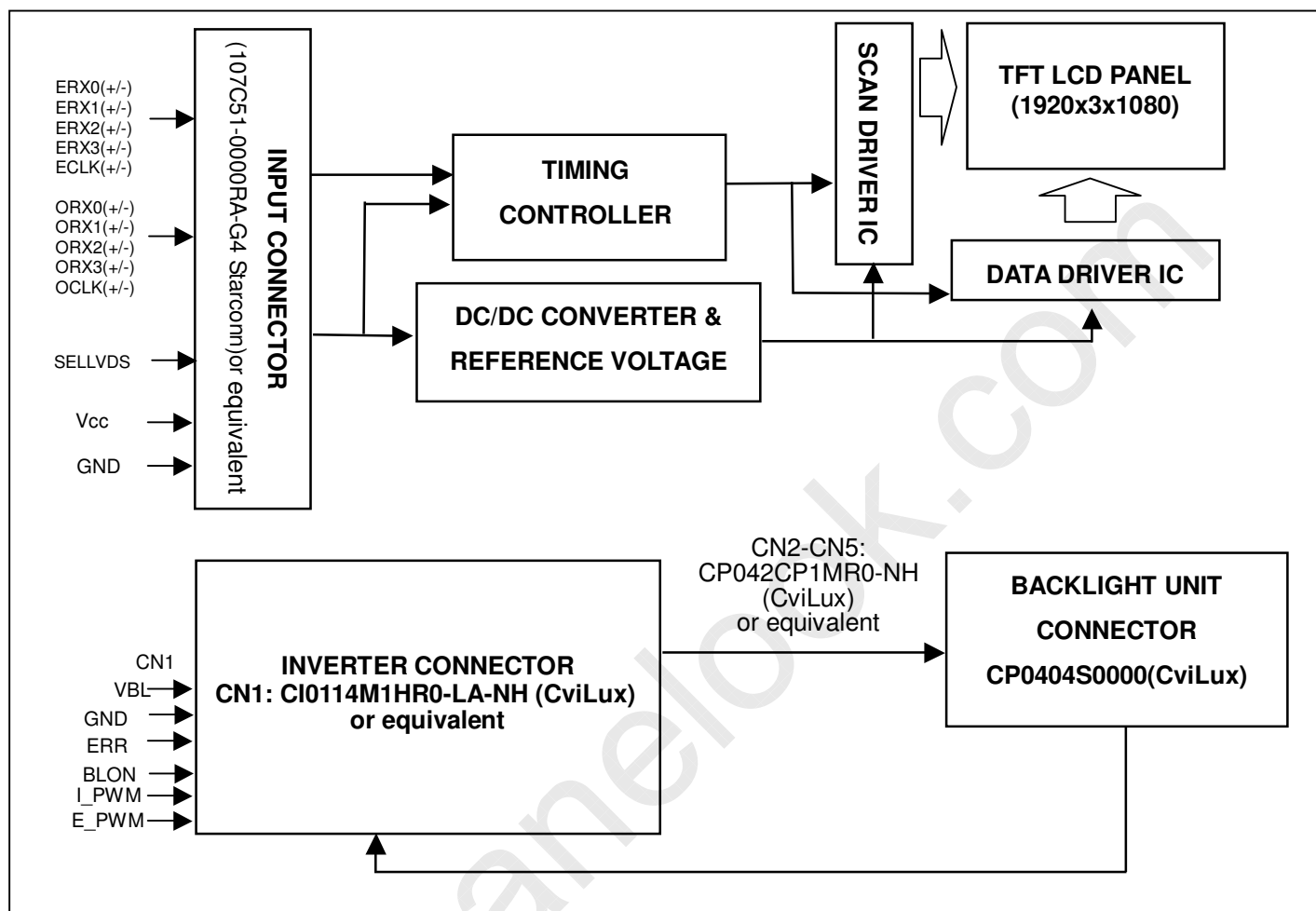
Turn ON sequence: VBL → PWM signal → BLON

Turn OFF sequence: BLOFF → PWM signal → VBL



## 4. BLOCK DIAGRAM

### 4.1 TFT LCD MODULE



## 5. INTERFACE PIN CONNECTION

### 5.1 TFT LCD MODULE

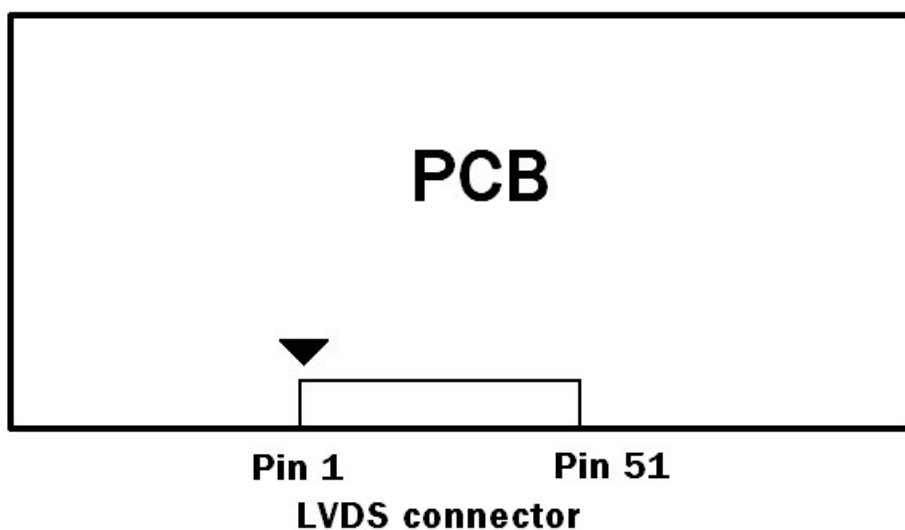
#### CNF1 Connector Pin Assignment

Pin	Name	Description	Note
1	VCC	+12V power supply	
2	VCC	+12V power supply	
3	VCC	+12V power supply	
4	VCC	+12V power supply	
5	VCC	+12V power supply	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	ORX0-	Odd pixel Negative LVDS differential data input. Channel 0	(1)
11	ORX0+	Odd pixel Positive LVDS differential data input. Channel 0	
12	ORX1-	Odd pixel Negative LVDS differential data input. Channel 1	
13	ORX1+	Odd pixel Positive LVDS differential data input. Channel 1	
14	ORX2-	Odd pixel Negative LVDS differential data input. Channel 2	
15	ORX2+	Odd pixel Positive LVDS differential data input. Channel 2	
16	GND	Ground	
17	OCLK-	Odd pixel Negative LVDS differential clock input	(1)
18	OCLK+	Odd pixel Positive LVDS differential clock input.	
19	GND	Ground	
20	ORX3-	Odd pixel Negative LVDS differential data input. Channel 3	(1)
21	ORX3+	Odd pixel Positive LVDS differential data input. Channel 3	
22	N.C.	No Connection	(3)
23	N.C.	No Connection	
24	GND	Ground	
25	ERX0-	Even pixel Negative LVDS differential data input. Channel 0	(1)
26	ERX0+	Even pixel Positive LVDS differential data input. Channel 0	
27	ERX1-	Even pixel Negative LVDS differential data input. Channel 1	
28	ERX1+	Even pixel Positive LVDS differential data input. Channel 1	
29	ERX2-	Even pixel Negative LVDS differential data input. Channel 2	
30	ERX2+	Even pixel Positive LVDS differential data input. Channel 2	
31	GND	Ground	
32	ECLK-	Even pixel Negative LVDS differential clock input.	(1)
33	ECLK+	Even pixel Positive LVDS differential clock input.	

34	GND	Ground	
35	ERX3-	Even pixel Negative LVDS differential data input. Channel 3	(1)
36	ERX3+	Even pixel Positive LVDS differential data input. Channel 3	
37	N.C.	No Connection	(3)
38	N.C.	No Connection	
39	GND	Ground	
40	N.C.	No Connection	(3)
41	N.C.	No Connection	
42	N.C.	No Connection	
43	N.C.	No Connection	
44	N.C.	No Connection	
45	SELLVDS	High(3.3V) or open for VESA, Low (GND) for JEIDA	(4)(5)
46	N.C.	No Connection	(3)
47	N.C.	No Connection	
48	N.C.	No Connection	
49	N.C.	No Connection	
50	N.C.	No Connection	
51	N.C.	No Connection	

Note (1) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel

Note (2) LVDS connector pin order defined as follows

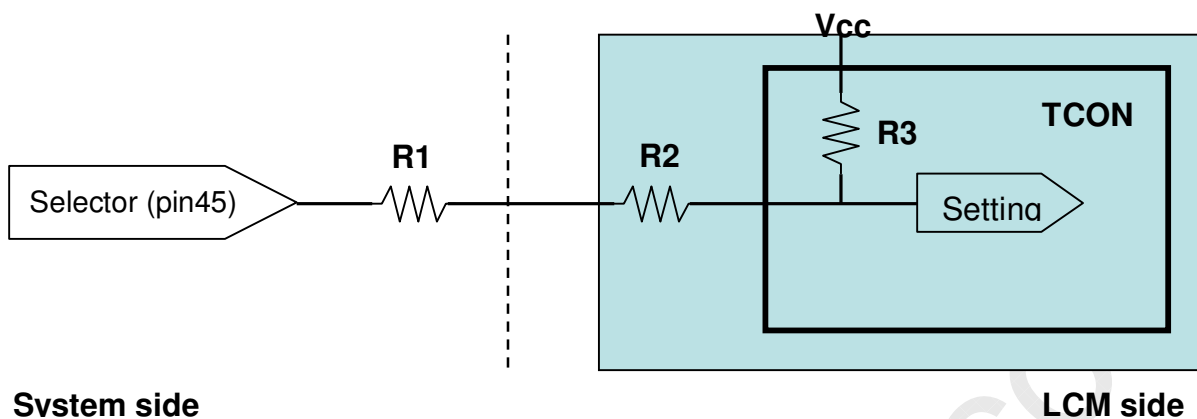


Note (3) Reserved for internal use. Please leave it open.

Note (4) Low: JEIDA LVDS Format (Connect to GND), High or open: VESA Format. (Connect to +3.3V)

Note (5) LVDS signal pin connected to the LCM side has the following diagram.

R1 in the system side should be less than 1K Ohm. ( $R1 < 1K \text{ Ohm}$ )



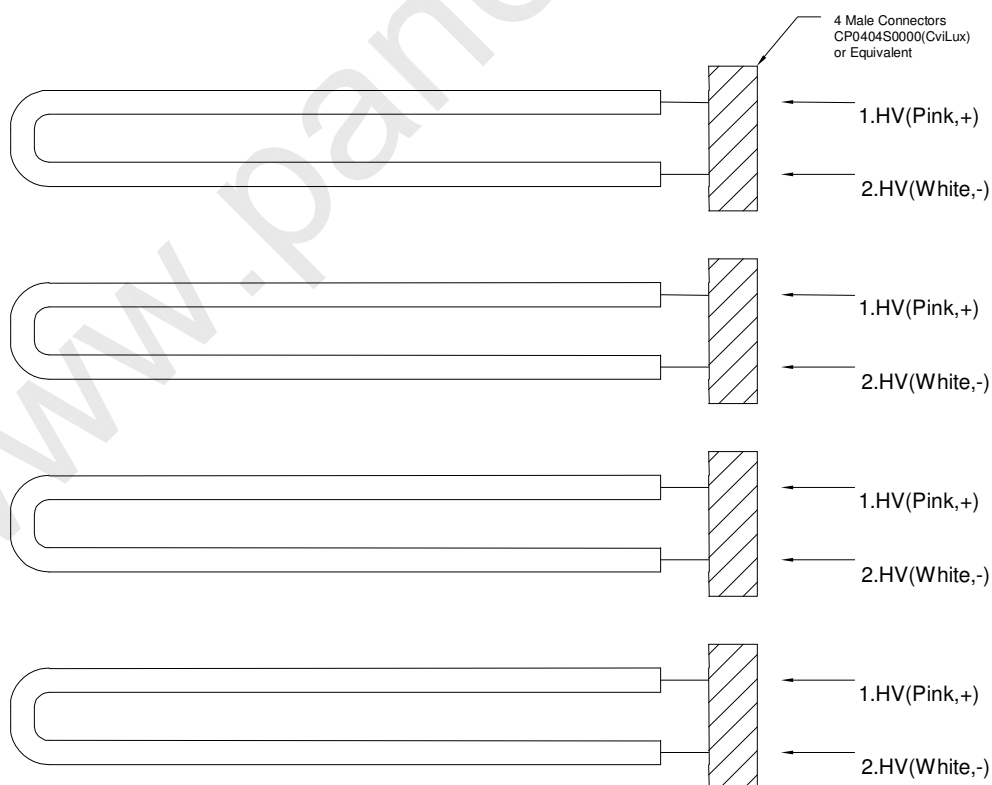
## 5.2 BACKLIGHT UNIT

The pin configuration for the housing and leader wire is shown in the table below.

Housing : 1.CP0404S0000(CviLux)

Pin No.	Symbol	Description	Wire Color
1	HV	High Voltage	Pink
2	HV	High Voltage	White

Note (1) The backlight interface housing for high voltage side is a model 1. CP0404S0000(CviLux).





### 5.3 INVERTER UNIT

CN1 : CI0114M1HR0-LA-NH (CviLux) or equivalent.

Pin No.	Symbol	Description
1	VBL	+24V Power input
2		
3		
4		
5		
6	GND	Ground
7		
8		
9		
10		
11	ERR	Normal (GND) Abnormal(Open collector)
12	BLON	BL ON/OFF
13	I_PWM	Internal PWM Control
14	E_PWM	External PWM Control

Note (1) PIN 13:Internal PWM Control (Use Pin 13): Pin 14 must open.

Note (2) PIN 14:External PWM Control (Use Pin 14): Pin 13 must open.

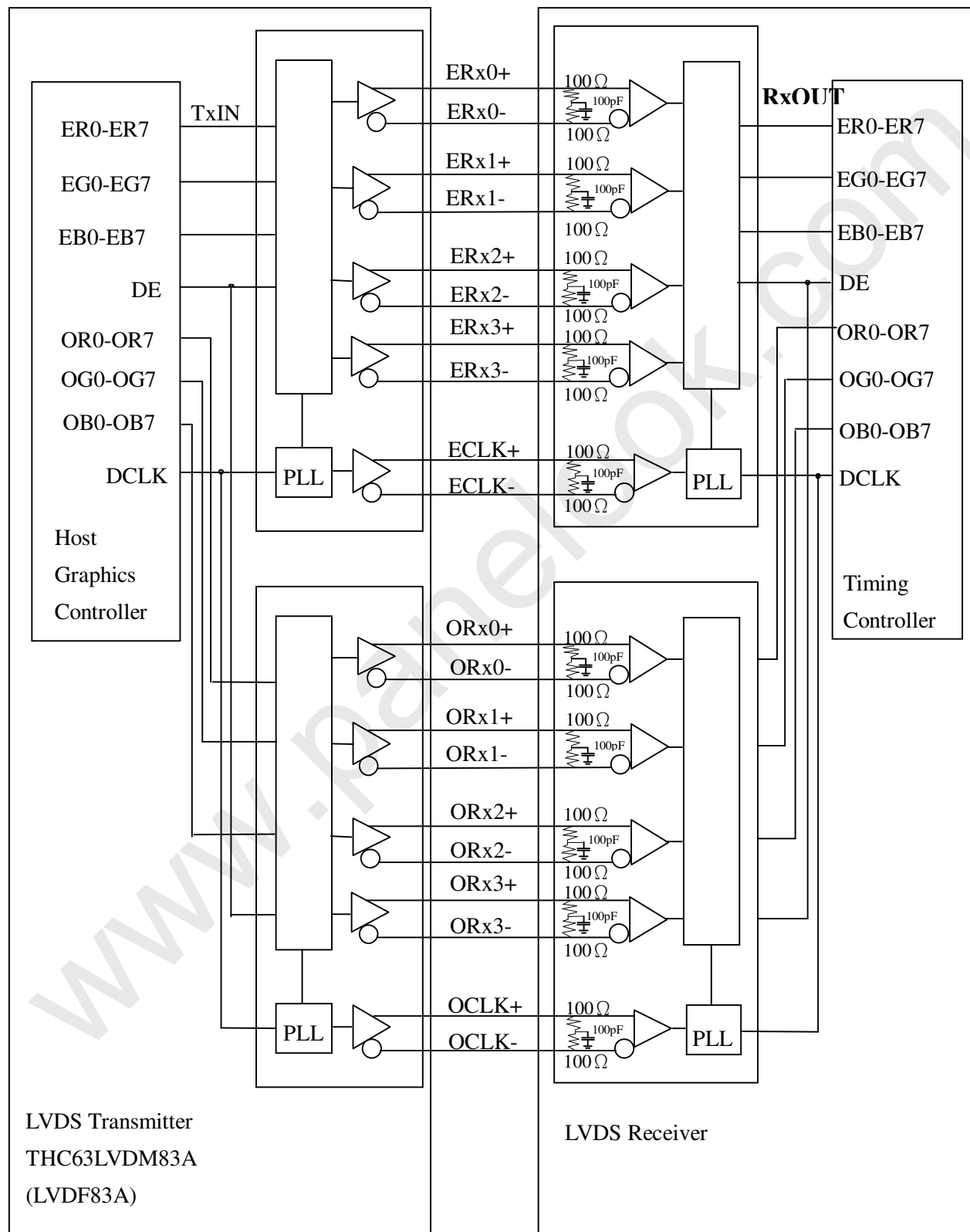
Note (3) Pin 13(I\_PWM) and Pin 14(E\_PWM) can't open in same period.

CN2-CN5 : CP042CP1MR0-NH (CviLux) or equivalent.

Pin	Name	Description
1	CCFL HOT	CCFL High Voltage
2	CCFL HOT	CCFL High Voltage

## 5.4 BLOCK DIAGRAM OF INTERFACE

CNF1



ER0~ER7: Even pixel R data

EG0~EG7: Even pixel G data

EB0~EB7: Even pixel B data

OR0~OR7: Odd pixel R data

OG0~OG7: Odd pixel G data

OB0~OB7: Odd pixel B data

DE: Data enable signal

DCLK: Data clock signal

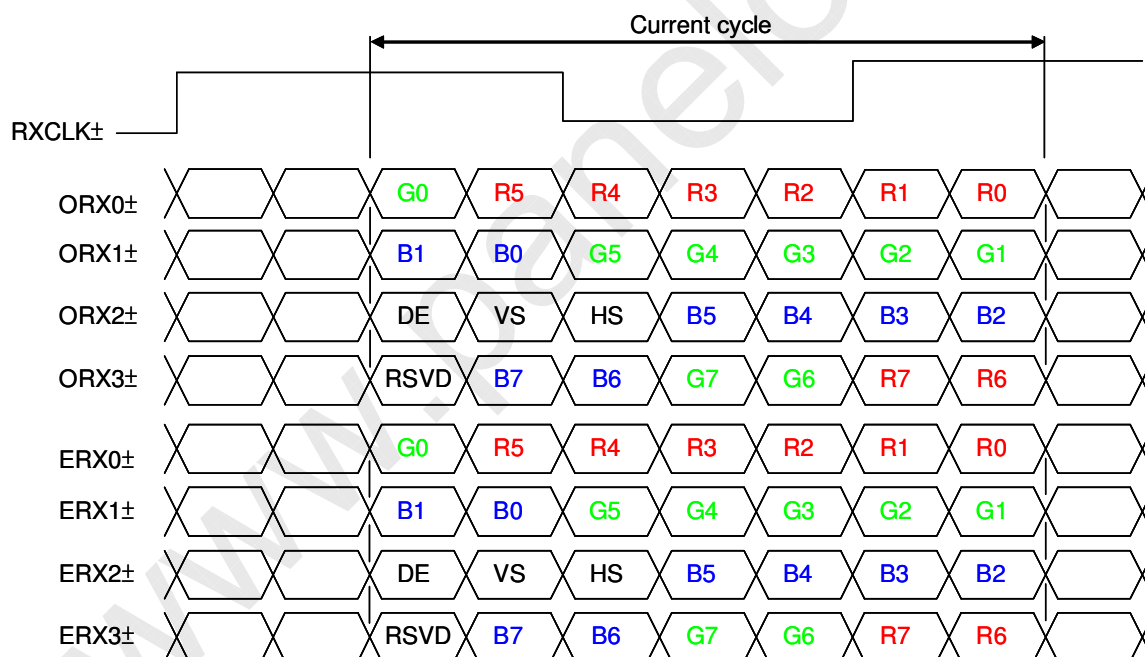
Note (1) The system must have the transmitter to drive the module.

Note (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

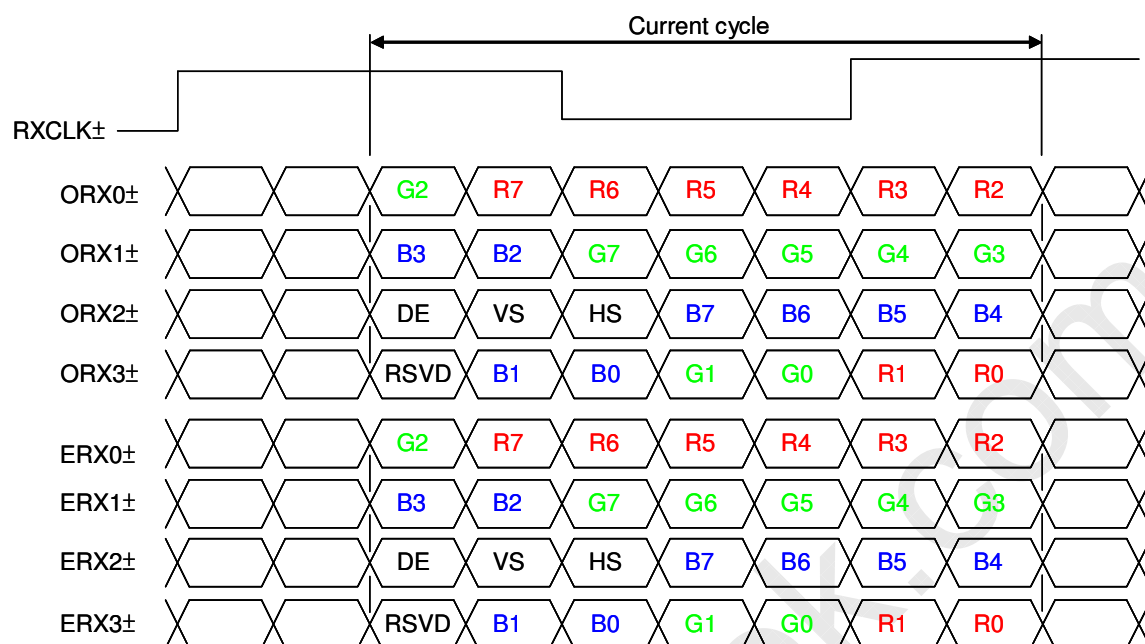
Note (3) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

## 5.5 LVDS INTERFACE

VESA LVDS format : (SELLVDS pin=H or open)



JEDIA LVDS format : (SELLVDS pin=L)



R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

Notes: (1) RSVD (reserved) pins on the transmitter shall be "H" or "L".

## 5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color.

The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

## 6. INTERFACE TIMING

### 6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

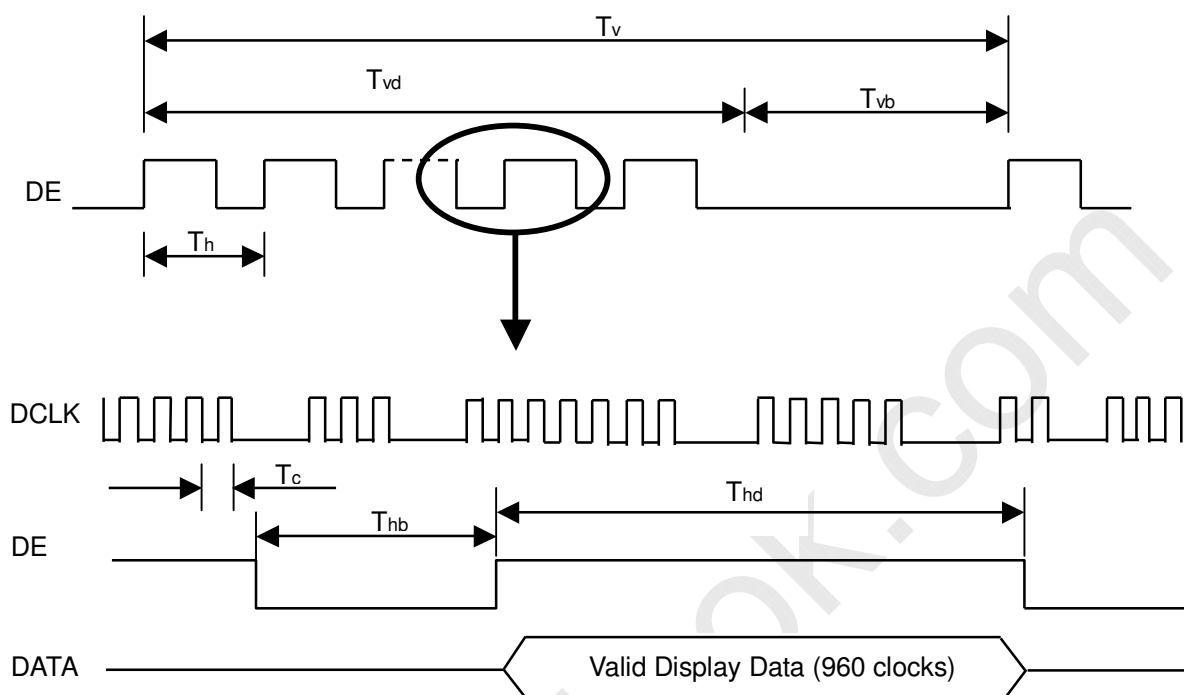
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	$F_{\text{clkin}}$ (=1/TC)	60	74.25	80	MHz	
	Input cycle to cycle jitter	$T_{\text{rcl}}$	—	—	200	ps	(3)
	Spread spectrum modulation range	$F_{\text{clkin\_mod}}$	$F_{\text{clkin}}-2\%$	—	$F_{\text{clkin}}+2\%$	MHz	(4)
	Spread spectrum modulation frequency	$F_{\text{SSM}}$			200	KHz	
LVDS Receiver Data	Setup Time	$T_{\text{lvsu}}$	600	—	—	ps	(5)
	Hold Time	$T_{\text{lvhd}}$	600	—	—	ps	
Vertical Active Display Term	Frame Rate	$F_{\text{r5}}$	47	50	53	Hz	
		$F_{\text{r6}}$	57	60	63	Hz	
	Total	$T_{\text{v}}$	1115	1125	1135	Th	$T_{\text{v}}=T_{\text{vd}}+T_{\text{vb}}$
	Display	$T_{\text{vd}}$	1080	1080	1080	Th	—
	Blank	$T_{\text{vb}}$	35	45	55	Th	—
Horizontal Active Display Term	Total	$T_{\text{h}}$	1050	1100	1150	$T_{\text{c}}$	$T_{\text{h}}=T_{\text{hd}}+T_{\text{hb}}$
	Display	$T_{\text{hd}}$	960	960	960	$T_{\text{c}}$	—
	Blank	$T_{\text{hb}}$	90	140	190	$T_{\text{c}}$	—

Note (1) Please make sure the range of pixel clock has follow the below equation :

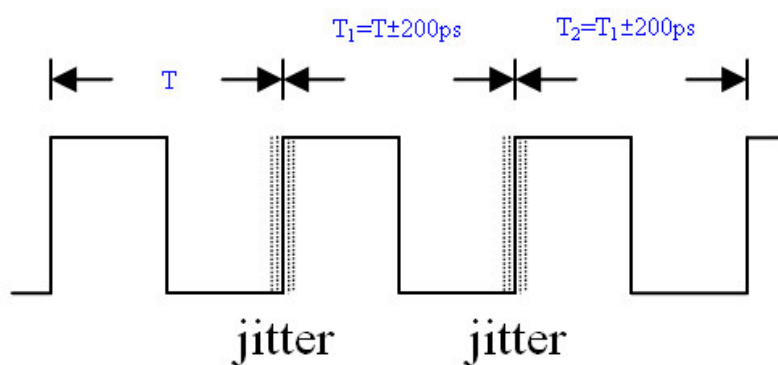
$$F_{\text{clkin}}(\text{max}) \geq F_{\text{r6}} \times T_{\text{v}} \times T_{\text{h}}$$

$$F_{\text{r5}} \times T_{\text{v}} \times T_{\text{h}} \geq F_{\text{clkin}}(\text{min})$$

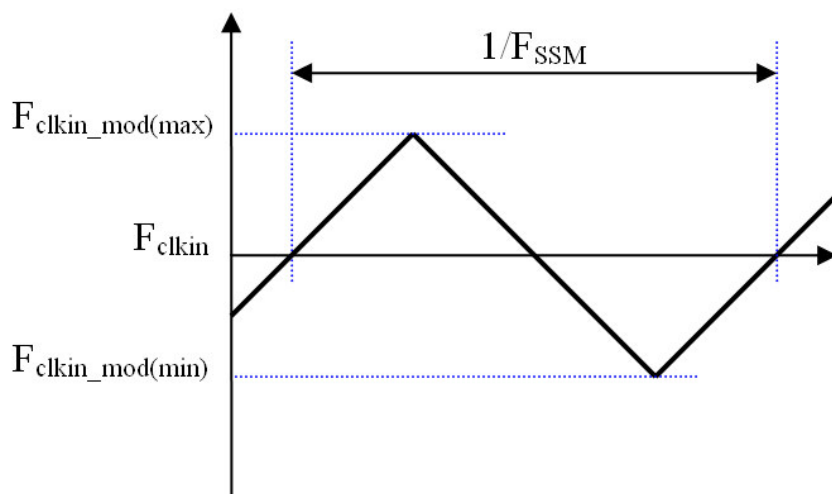
Note (2) This module is operated in DE only mode and please follow the input signal timing diagram below :

**INPUT SIGNAL TIMING DIAGRAM**

Note (3) The input clock cycle-to-cycle jitter is defined as below figures.  $Trcl = |T_1 - T_1|$

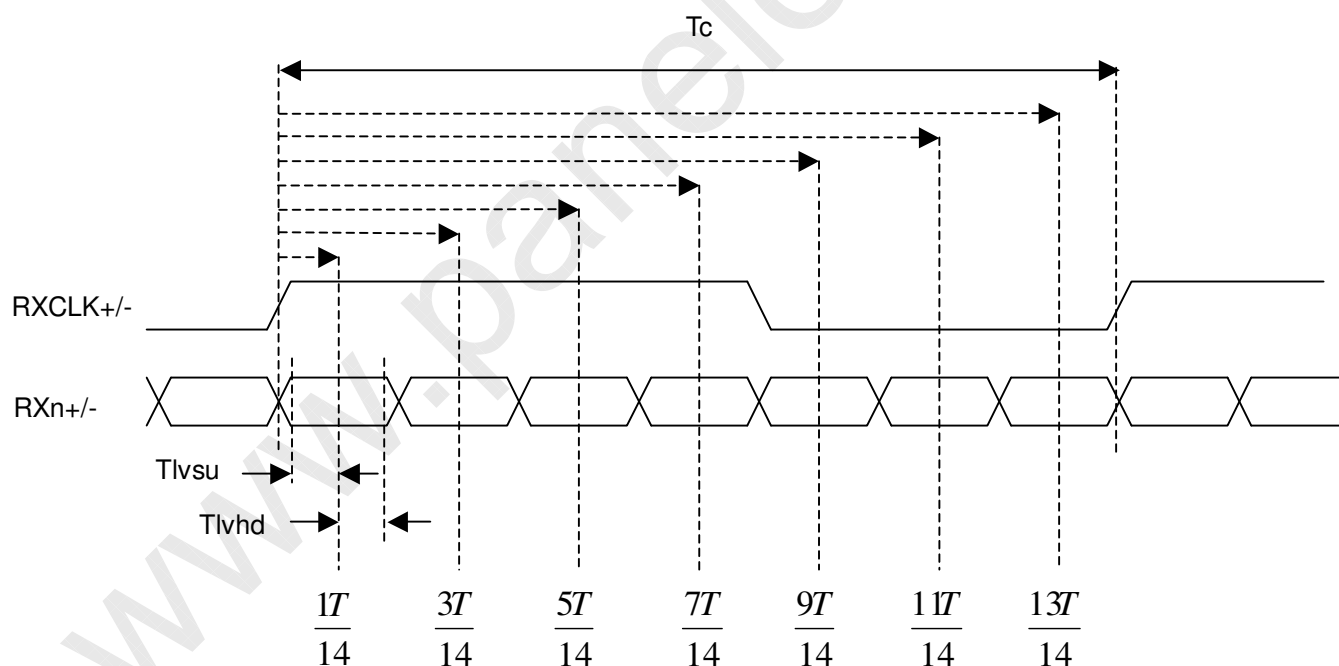


Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

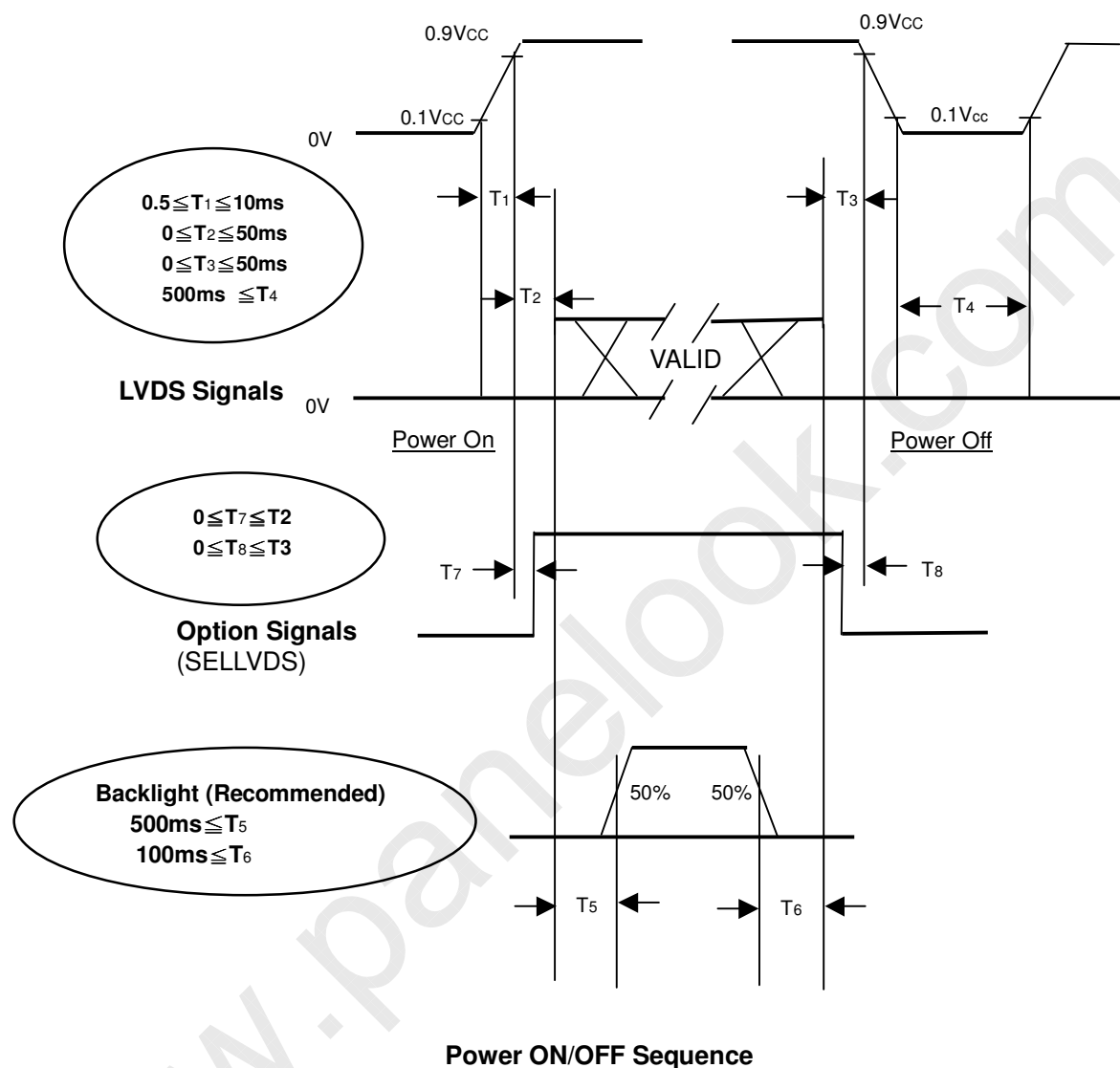
### LVDS RECEIVER INTERFACE TIMING DIAGRAM





## 6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance. If  $T_2 < 0$ , that maybe cause electrical overstress failure.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

## 7. OPTICAL CHARACTERISTICS

### 7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V <sub>CC</sub>	12.0	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	I <sub>L</sub>	7.5 ± 0.5	mA
Oscillating Frequency (Inverter)	F <sub>W</sub>	58 ± 3	KHz
Vertical Frame Rate	Fr	60	Hz

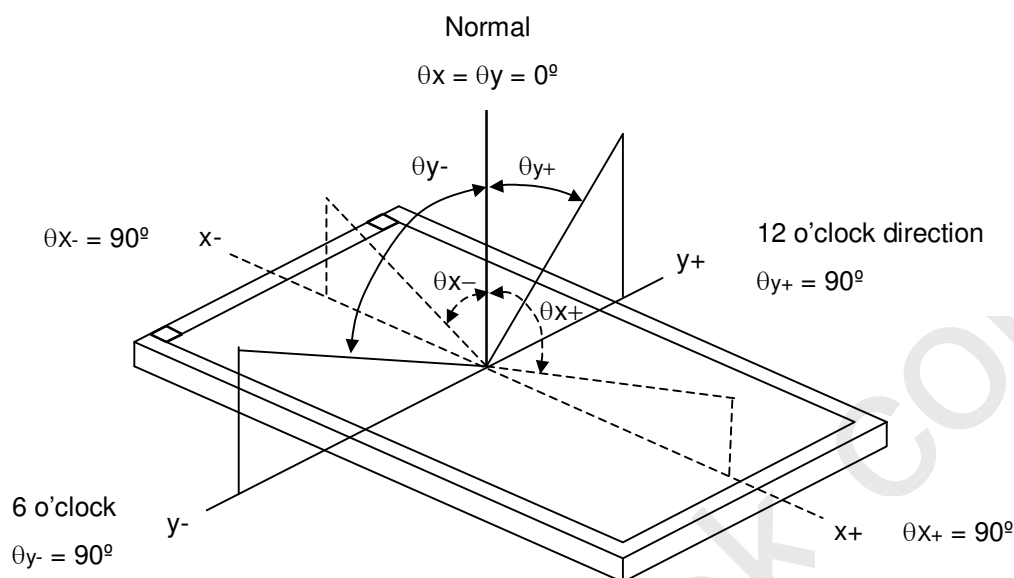
### 7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	$\theta_x=0^\circ, \theta_Y=0^\circ$  Viewing angle at normal direction	600	800		-	(2)
Response Time		T <sub>R</sub>			1.4	2.2	ms	(3)
		T <sub>F</sub>			3.6	5.8		
Center Luminance of White		L <sub>C</sub>		320	400			(4)
White Variation		δW				1.3	-	(7)
Cross Talk		CT				4	%	(5)
Color Chromaticity	Red	R <sub>x</sub>		Typ. -0.03	0.640	Typ. +0.03	-	(6)
		R <sub>y</sub>			0.330		-	
	Green	G <sub>x</sub>			0.268		-	
		G <sub>y</sub>			0.595		-	
	Blue	B <sub>x</sub>			0.150		-	
		B <sub>y</sub>			0.064		-	
	White	W <sub>x</sub>			0.280		Target	
		W <sub>y</sub>			0.290			
	Color Gamut			CG		72		%
Viewing Angle	Horizontal	θ <sub>x+</sub>	CR≥10	70	80		Deg.	(1)
		θ <sub>x-</sub>		70	80			
	Vertical	θ <sub>y+</sub>		70	80			
		θ <sub>y-</sub>		60	70			

Note (1) Definition of Viewing Angle ( $\theta_x, \theta_y$ ):

Viewing angles are measured by Autronic Conoscope Cono-80.



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = L_{255} / L_0$$

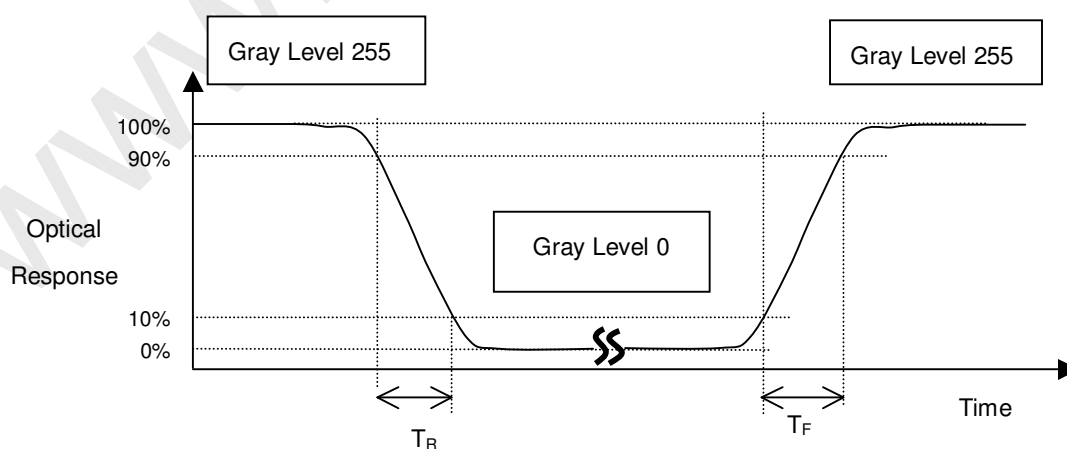
L255: Luminance of gray level 255

L0: Luminance of gray level 0

$$CR = CR(5),$$

CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (7).

Note (3) Definition of Response Time ( $T_R, T_F$ ):



Note (4) Definition of Luminance of White ( $L_C$ ):

Measure the luminance of gray level 255 at center point and 5 points

$$L_C = L(5)$$

$L(X)$  is corresponding to the luminance of the point X at the figure in Note (7).

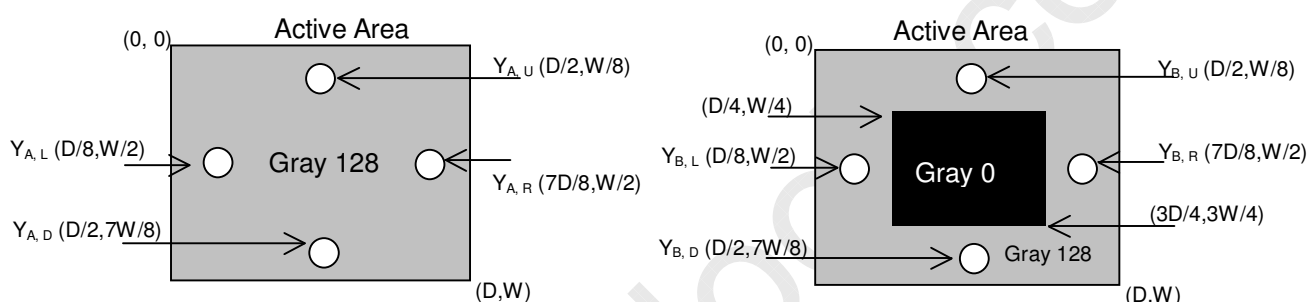
Note (5) Definition of Cross Talk (CT):

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where:

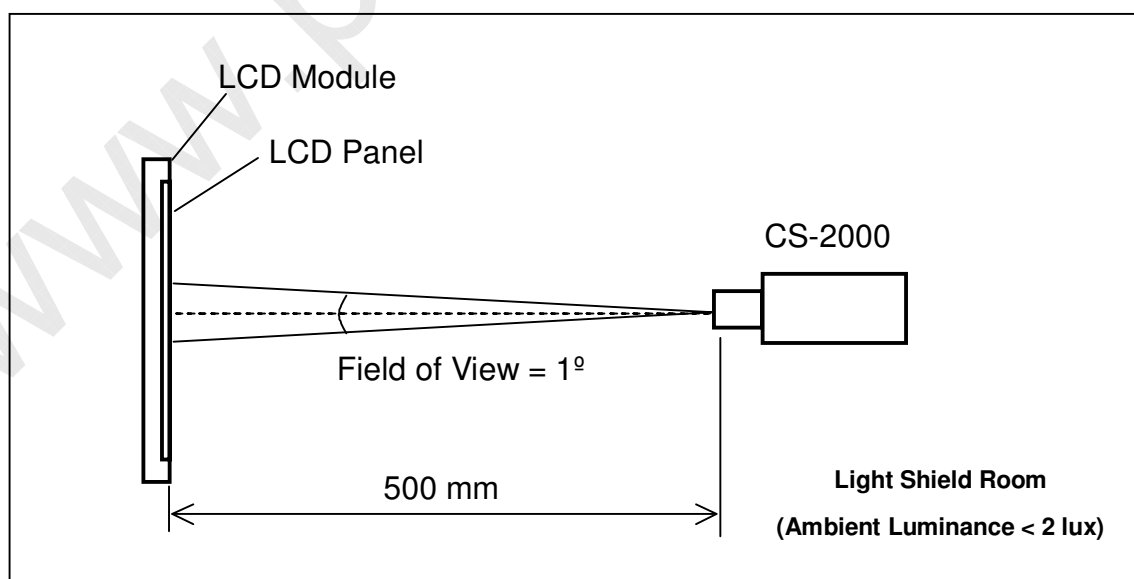
$Y_A$  = Luminance of measured location without gray level 0 pattern ( $\text{cd/m}^2$ )

$Y_B$  = Luminance of measured location with gray level 0 pattern ( $\text{cd/m}^2$ )



Note (6) Measurement Setup:

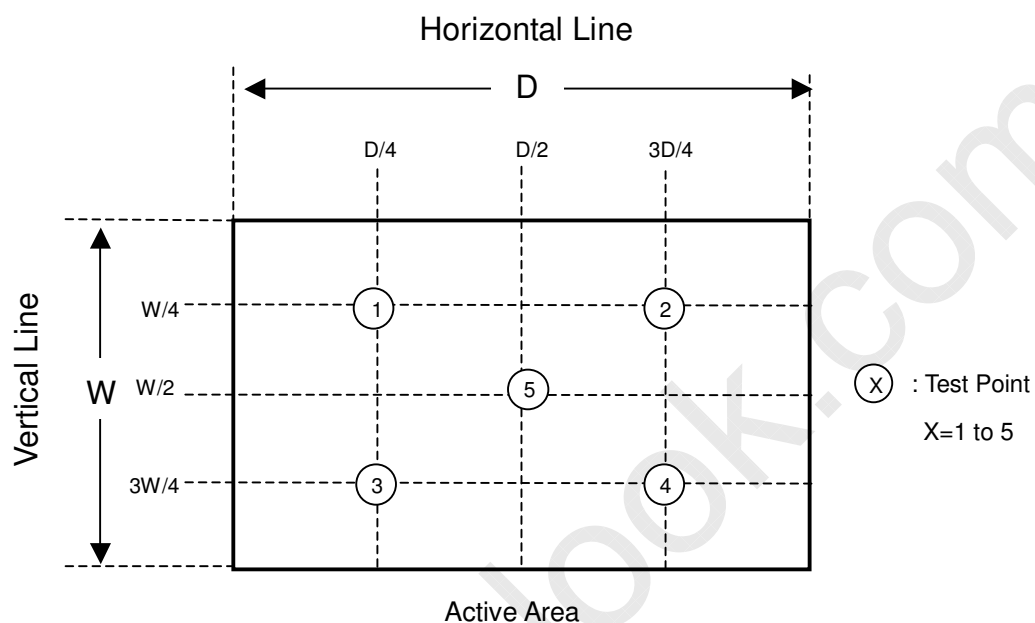
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement (CS-1000 or CA-210 calibrated by CS-2000) should be executed after lighting backlight for 1 hour in a windless room.



Note (7) Definition of White Variation ( $\delta W$ ):

Measure the luminance of gray level 255 at 5 points.

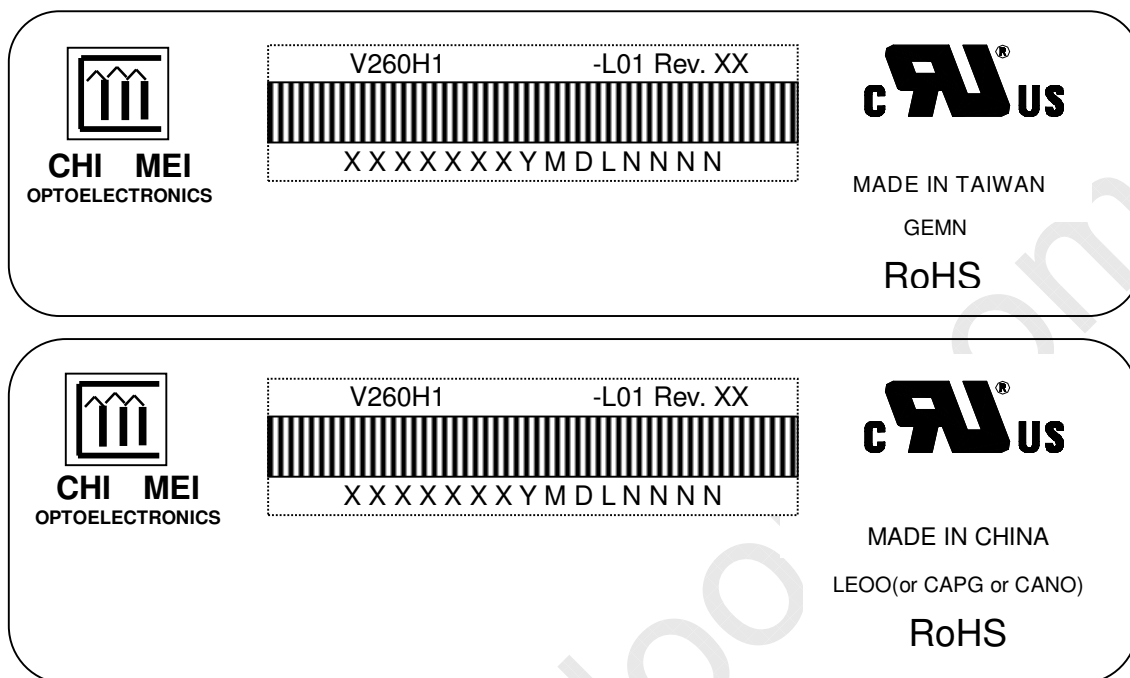
$$\delta W = \text{Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]}$$



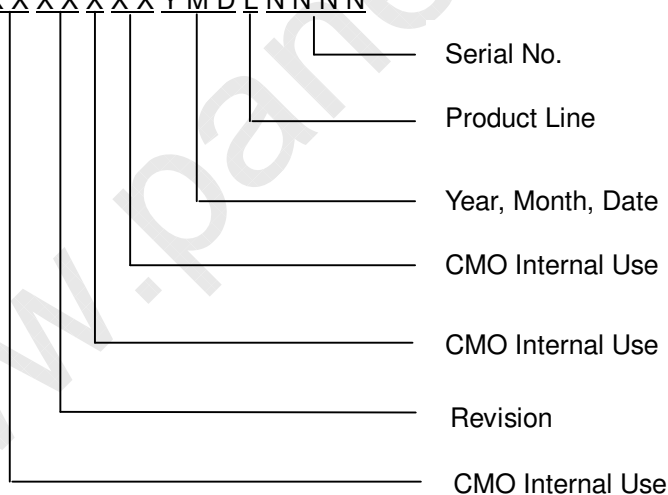
## 8. DEFINITION OF LABELS

### 8.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



- (a) Model Name: V260H1-L01
- (b) Revision: Rev. XX, for example: A0, A1... B1, B2... or C1, C2...etc.
- (c) Serial ID: XXXXXXXXYMDLNNNN



Serial ID includes the information as below:

- (a) Manufactured Date: Year: 0~9, for 2010~2019  
 Month: 1~9, A~C, for Jan. ~ Dec.  
 Day: 1~9, A~Y, for 1<sup>st</sup> to 31<sup>st</sup>, exclude I, O, and U.
- (b) Revision Code: Cover all the change
- (c) Serial No.: Manufacturing sequence of product
- (d) Product Line: 1 -> Line1, 2 -> Line 2, ...etc.

## 9. PACKAGING

### 9.1 PACKING SPECIFICATIONS

- (1) 7 LCD TV modules / 1 Box
- (2) Box dimensions : 713(L)x429(W)x453(H)mm
- (3) Weight : approximately 28.48 Kg ( 7 modules per box)

### 9.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method

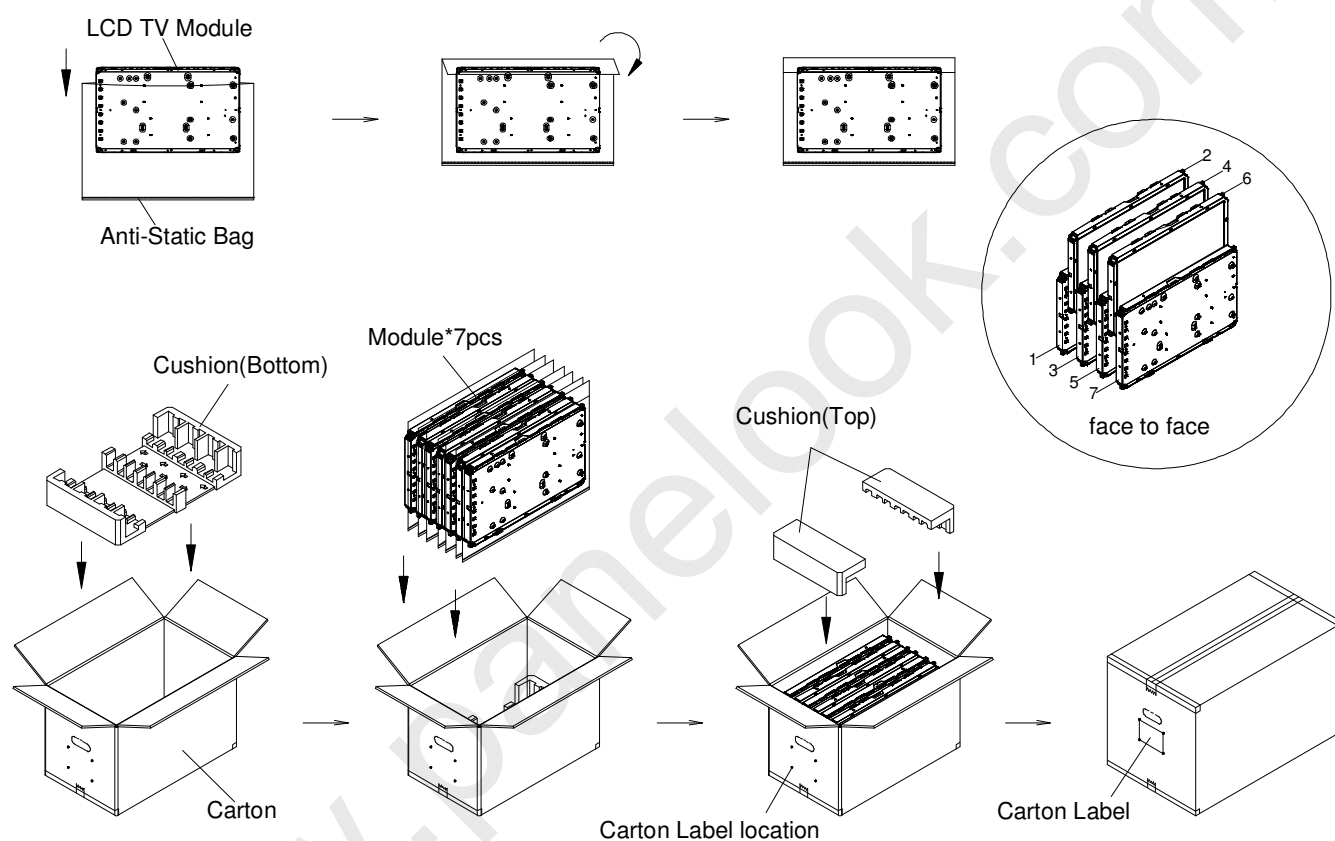
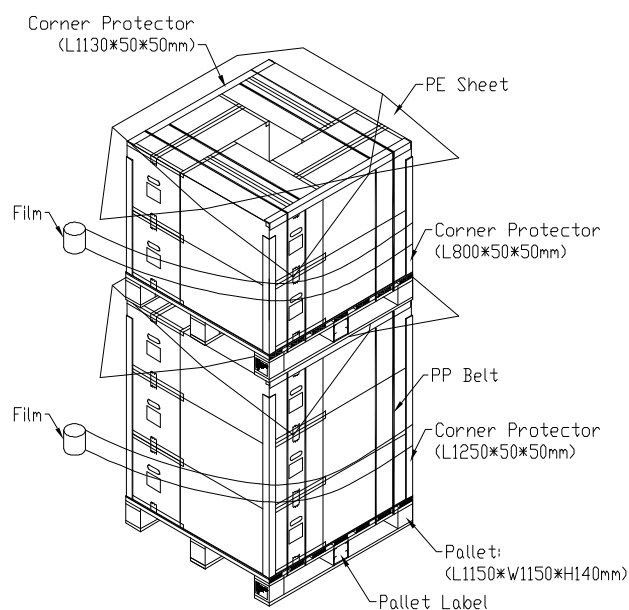
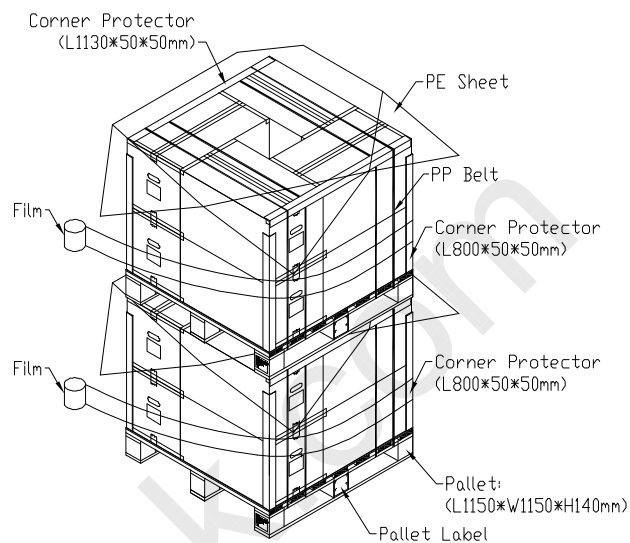


Figure.9-1 packing method

### Sea / Land Transportation (40ft HQ Container)



### Sea / Land Transportation (40ft Container)



### Air Transportation

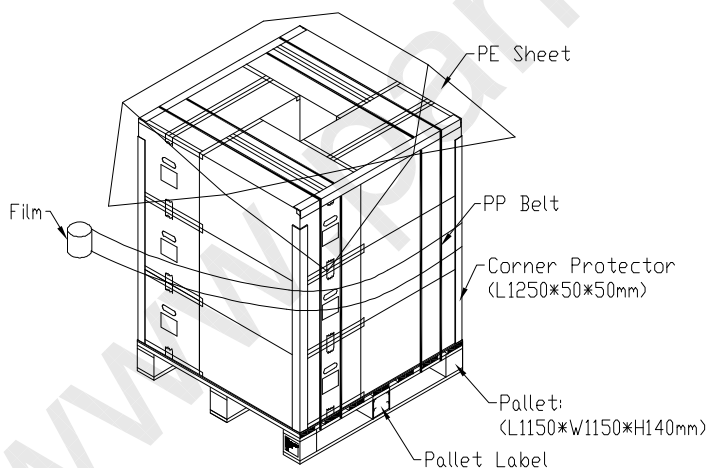


Figure.9-2 Packing method



## 10. PRECAUTIONS

### 10.1 ASSEMBLY AND HANDLING PRECAUTIONS

- (1) Do not apply rough force such as bending or twisting to the module during assembly.
- (2) It is recommended to assemble or to install a module into the user's system in clean working areas.  
The dust and oil may cause electrical short or worsen the polarizer.
- (3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and backlight.
- (4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.
- (5) Do not plug in or pull out the I/F connector while the module is in operation.
- (6) Do not disassemble the module.
- (7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- (8) Moisture can easily penetrate into LCD module and may cause the damage during operation.
- (9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.
- (10) When ambient temperature is lower than 10°C, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

### 10.2 SAFETY PRECAUTIONS

- (1) The startup voltage of a backlight is over 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the backlight unit.
- (2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- (3) After the module's end of life, it is not harmful in case of normal operation and storage.

### 10.3 STORAGE PRECAUTIONS

When storing modules as spares for a long time, the following precaution is necessary.

- (1) Do not leave the module in high temperature, and high humidity for a long time.  
It is highly recommended to store the module with temperature from 0 to 35°C at normal humidity without condensation.
- (2) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.



## 11. REGULATORY STANDARDS

### 11.1 SAFETY

The LCD module should be certified with safety regulations as follows:

Requirement	Standard	Remark
UL	UL60950-1:2006 or Ed.2:2007	
	UL60065 Ed.7:2007	
cUL/CSA	CAN/CSA C22.2 No.60950-1-03 or 60950-1-07	
	CAN/CSA C22.2 No.60065-03:2006 + A1:2006	
CB	IEC60950-1:2005 / EN60950-1:2006+ A11:2009	
	IEC60065:2001+ A1:2005 / EN60065:2002 + A1:2006 + A11:2008	

## 12. MECHANICAL CHARACTERISTICS

