UTRON

UT61512

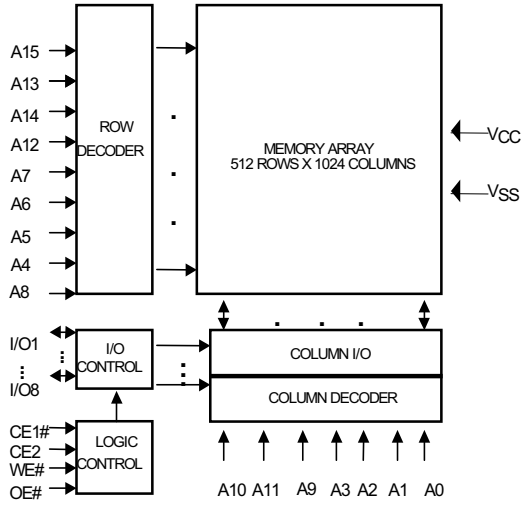
Preliminary V1.1

64K X 8 BIT HIGH SPEED CMOS SRAM

FEATURES

- Fast access time : 8/12/15 ns (max.)
- Low operating power consumption : 100 mA (typical)
- Single 5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Three state outputs
- Package : 32-pin 300 mil SOJ

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A15	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
CE1#	Chip Enable 1 input
CE2	Chip Enable 2 input
WE#	Write Enable Input
OE#	Output Enable Input
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

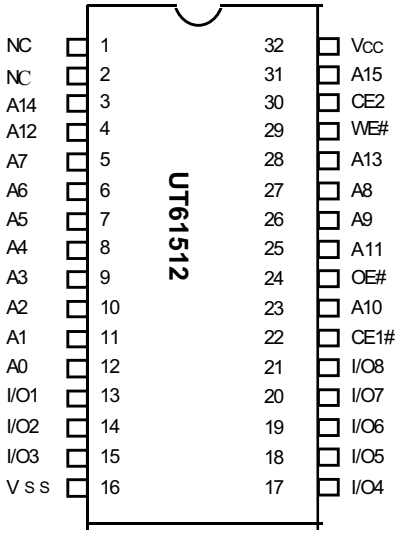
GENERAL DESCRIPTION

The UT61512 is a 524,288-bit high-speed CMOS static random access memory organized as 655,036 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

The UT61512 is designed for high-speed system applications. It is particularly suited for use in high-density high-speed system applications.

The UT61512 operates from a single 5V power supply and all inputs and outputs are fully TTL compatible.

PIN CONFIGURATION



SOJ

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ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to Vss	V_{TERM}	-0.5 to +6.5	V
Operating Temperature	T_A	0 to +70	℃
Storage Temperature	T_{STG}	-65 to +150	℃
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA
Soldering Temperature (under 10 sec)	Tsolder	260	℃

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE1#	CE2	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High - Z	I_{SB},I_{SB1}
Standby	X	L	X	X	High -Z	I_{SB},I_{SB1}
Output Disable	L	H	H	H	High - Z	I_{CC}
Read	L	H	L	H	D_{OUT}	I_{CC}
Write	L	H	X	L	D_{IN}	I_{CC}

Note: H = V_{IH}, L=V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V± 10%, T_A = 0℃ to 70℃)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	MAX.	UNIT
Input High Voltage	V_{IH}			2.2	V_{CC}+0.5	V
Input Low Voltage	V_{IL}			- 0.5	0.8	V
Input Leakage Current	I_{LI}	$V_{SS} \leqq V_{IN} \leqq V_{CC}$		- 1	1	μA
Output Leakage Current	I_{LO}	$V_{SS} \leqq V_{I/O} \leqq V_{CC}$ CE1# = V_{IH} or CE2 = V_{IL} or OE# = V_{IH} or WE# = V_{IL}		- 1	1	μA
Output High Voltage	V_{OH}	I_{OH} = - 4mA		2.4	-	V
Output Low Voltage	V_{OL}	I_{OL} = 8mA		-	0.4	V
Operating Power Supply Current	I_{CC}	CE1# = V_{IL} , CE2 = V_{IH} $I_{I/O}$ = 0mA , Cycle=Min.	- 8	-	190	mA
			- 12	-	160	mA
			- 15	-	140	mA
Standby Power Supply Current	I_{SB}	CE1# = V_{IH} or CE2 = V_{IL}		-	30	mA
	I_{SB1}	CE1# $\geqq V_{CC}$-0.2V or CE2 $\leqq$ 0.2V		-	5	mA

CAPACITANCE (T_A=25℃, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C_{IN}	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L=30pF, I_{OH}/I_{OL}=-4mA/8mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V± 10% , T_A = 0℃ to 70℃)

(1) READ CYCLE

PARAMETER	SYMBOL	UT61512-8		UT61512-12		UT61512-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	8	-	12	-	15	-	ns
Address Access Time	t_{AA}	-	8	-	12	-	15	ns
Chip Enable Access Time	t_{ACE}	-	8	-	12	-	15	ns
Output Enable Access Time	t_{OE}	-	4	-	6	-	7	ns
Chip Enable to Output in Low Z	t_{CLZ*}	2	-	3	-	4	-	ns
Output Enable to Output in Low Z	t_{OLZ*}	0	-	0	-	0	-	ns
Chip Disable to Output in High Z	t_{CHZ*}	-	4	-	6	-	7	ns
Output Disable to Output in High Z	t_{OHZ*}	-	4	-	6	-	7	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns

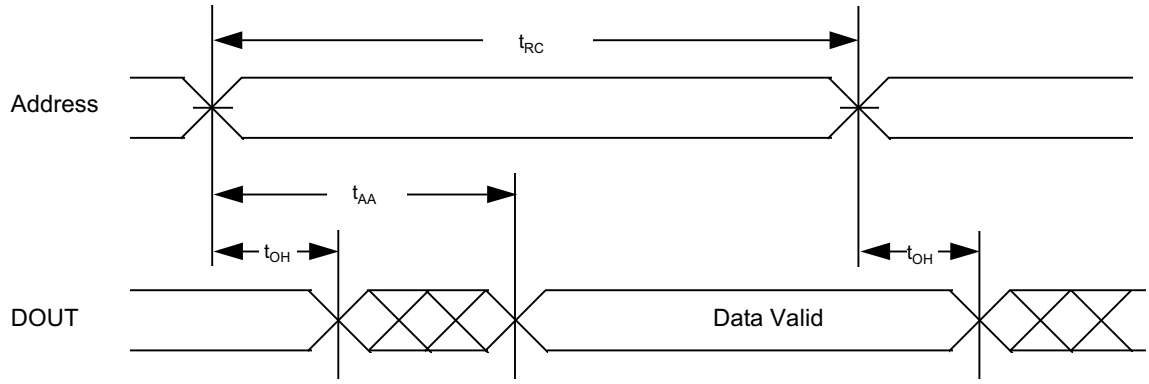
(2) WRITE CYCLE

PARAMETER	SYMBOL	UT61512-8		UT61512-12		UT61512-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	8	-	12	-	15	-	ns
Address Valid to End of Write	t_{AW}	6.5	-	10	-	12	-	ns
Chip Enable to End of Write	t_{CW}	6.5	-	10	-	12	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	6.5	-	9	-	10	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	**4**	-	**6**	-	**7**	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW*}	1.5	-	3	-	4	-	ns
Write to Output in High Z	t_{WHZ*}	**-**	**4**	-	**6**	-	**7**	ns

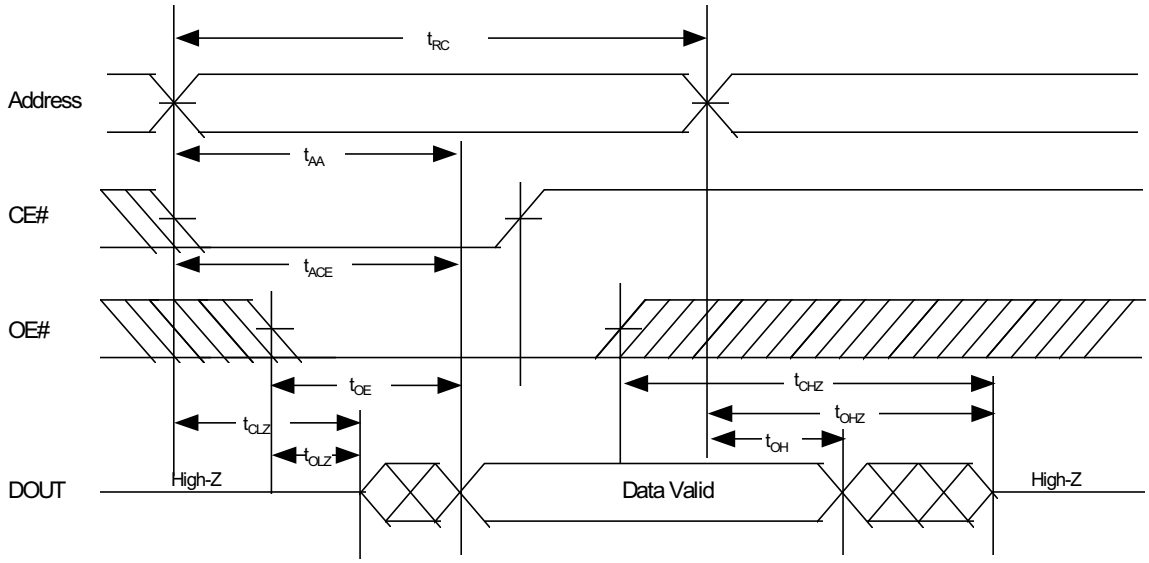
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2,4)

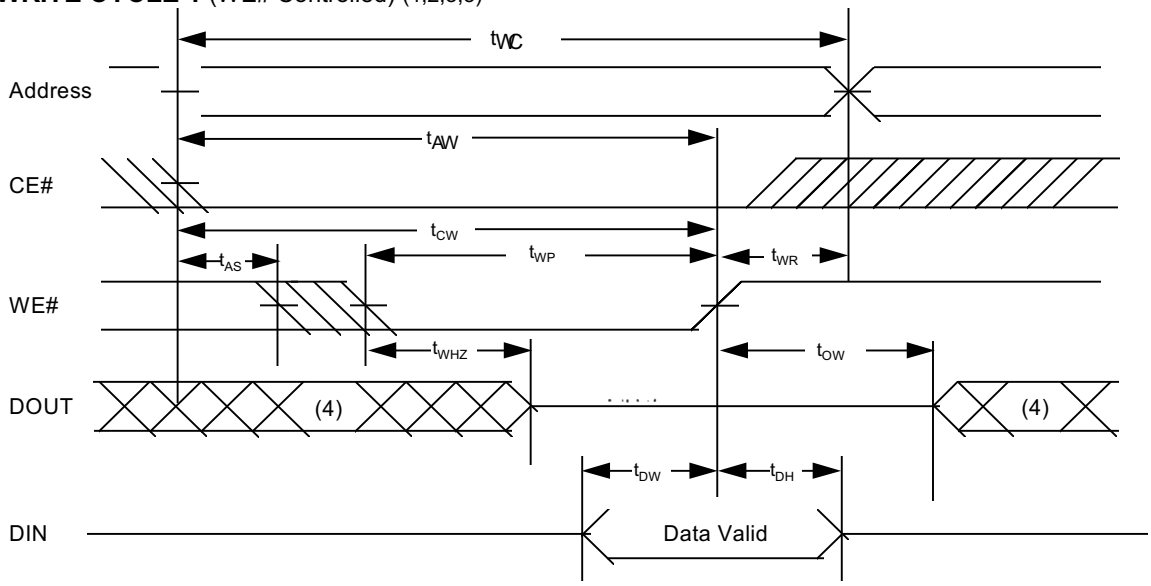


READ CYCLE 2 (CE# and OE# Controlled) (1,3,5,6)

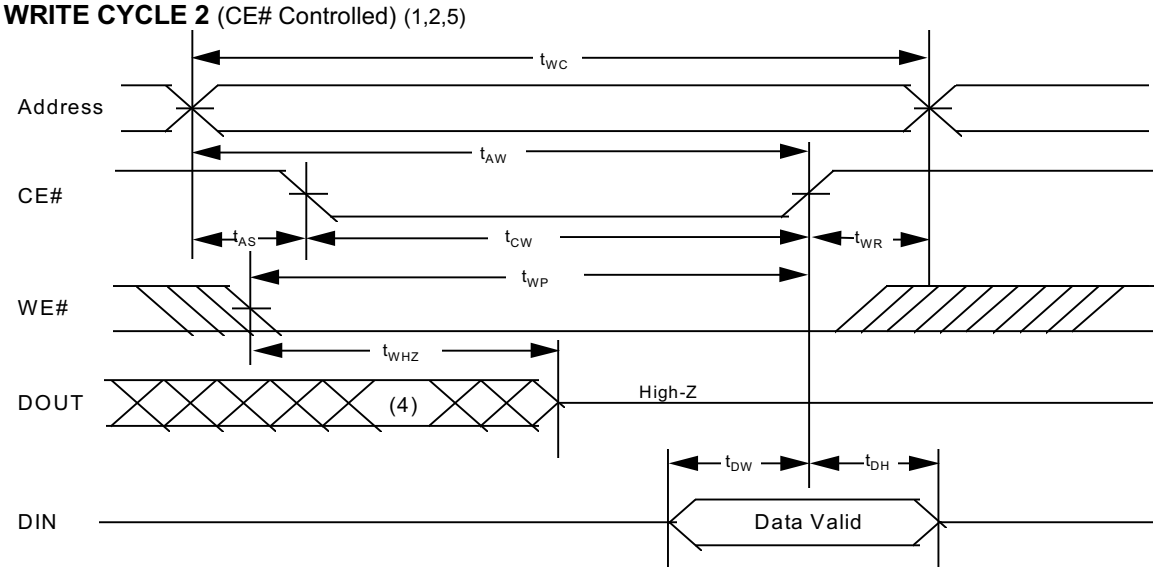


Notes :
1. WE# is HIGH for read cycle.
2. Device is continuously selected CE#=V_{IL}.
3. Address must be valid prior to or coincident with CE# transition; otherwise t_{AA} is the limiting parameter.
4. OE# is LOW.
5. t_{CLZ}, t_{OLZ}, t_{CHZ} and t_{OHZ} are specified with C_L = 5pF. Transition is measured ± 500mV from steady state.
6. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ}, t_{OHZ} is less than t_{OLZ}.

WRITE CYCLE 1 (WE# Controlled) (1,2,3,5)



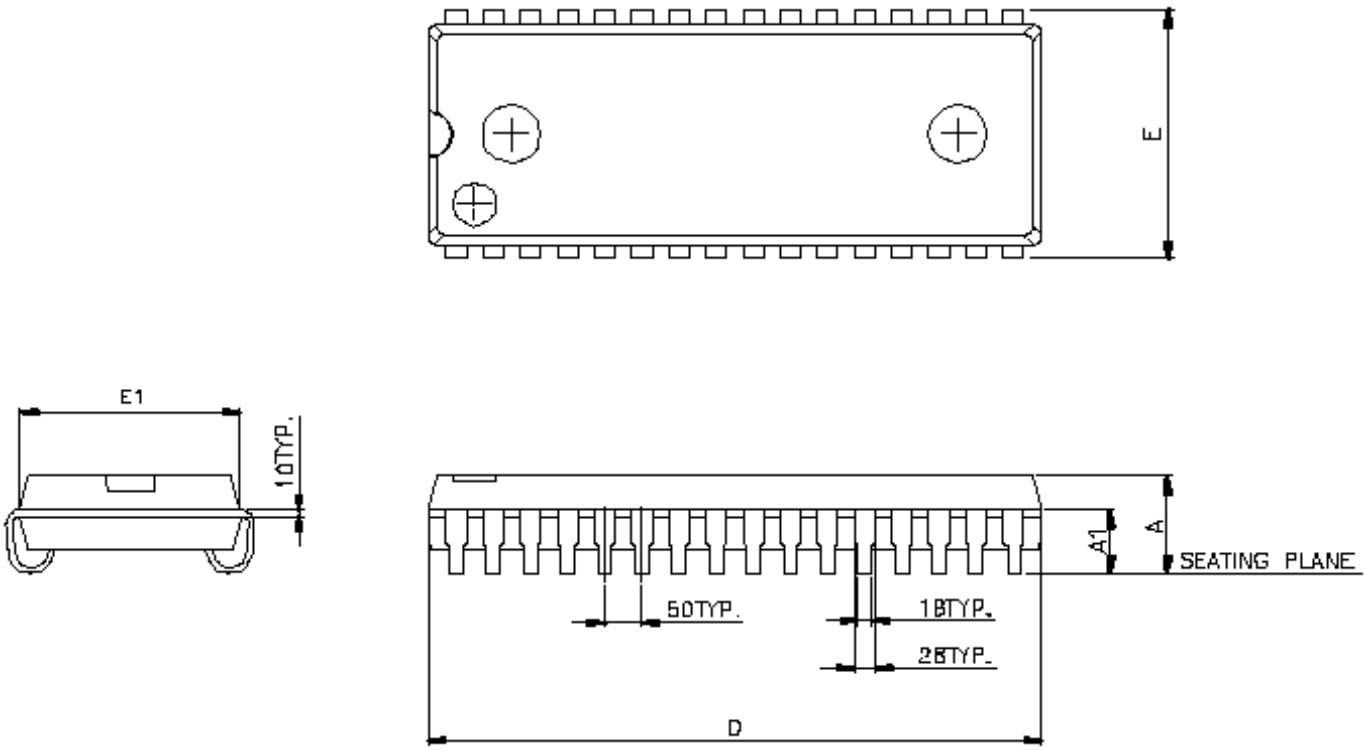
WRITE CYCLE 2 (CE# Controlled) (1,2,5)



Notes :
1. WE# or CE# must be HIGH during all address transitions.
2. A write occurs during the overlap of a low CE# and a low WE#.
3. During a WE# controlled with write cycle with OE# LOW, t_{WP} must be greater than $t_{WHZ}+t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input singals must not be applied.
5. If the CE# LOW transition occurs simultaneously with or after WE# LOW transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ± 500mV from steady state.

PACKAGE OUTLINE DIMENSION

32 pin 300 mil SOJ Package Outline Dimension



SYMBOLS	MIN.	NOR.	MAX.
A	0.128	0.138	0.148
A1	0.082	--	--
D	0.820	0.825	0.830
E	0.335 BSC.		
E1	0.295	0.300	0.305

UNIT：INCH

NOTE：

1. JEDEC OUTLINE：MO-077 AC

2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.006 INCH PER SIDE.

ORDERING INFORMATION

PART NO.	ACCESS TIME (ns)	PACKAGE
UT61512JC-8	8	32PIN SOJ
UT61512JC-12	12	32PIN SOJ
UT61512JC-15	15	32PIN SOJ