Standard Products

UT54ACTS899

9-bit Latchable Transceiver with Parity Generator/Checker
Datasheet

May 16, 2012
www.aeroflex.com/Logic

FEATURES

- ❑ Latchable transceiver with output source/sink of 24mA
- ❑ Option to select generate parity and check or "feed-through" data/parity in directions A-to-B or B-to-A
- ❑ Independent latch enable for A-to-B and B-to-A directions
- ❑ Select pin for ODD/$\overline{\text{EVEN}}$ parity
- ❑ $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$ output pins for parity checking
- ❑ Ability to simultaneously generate and check parity
- ❑ 0.6µm Commercial CMOS
- ❑ Operational environment:
  - Total dose: 100K rad(Si)
  - Single Event Latchup immune
  - SEU immune
- ❑ Standard Microcircuit Drawing 5962-06240
  - QML compliant part
- ❑ Package:
  - 28-pin ceramic flatpack

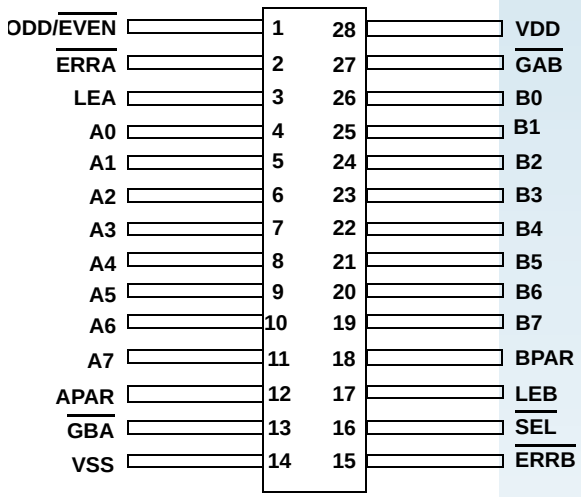
DESCRIPTION

The UT54ACTS899 is a 9-bit to 9-bit parity transceiver with transparent latches. The device can operate as a feed-through transceiver or it can generate/check parity from the 8-bit data busses in either direction. The UT54ACTS899 features independent latch enables for the A-to-B direction and the B-to-A direction, a select pin for ODD/$\overline{\text{EVEN}}$ parity, and separate error signal output pins for checking parity.

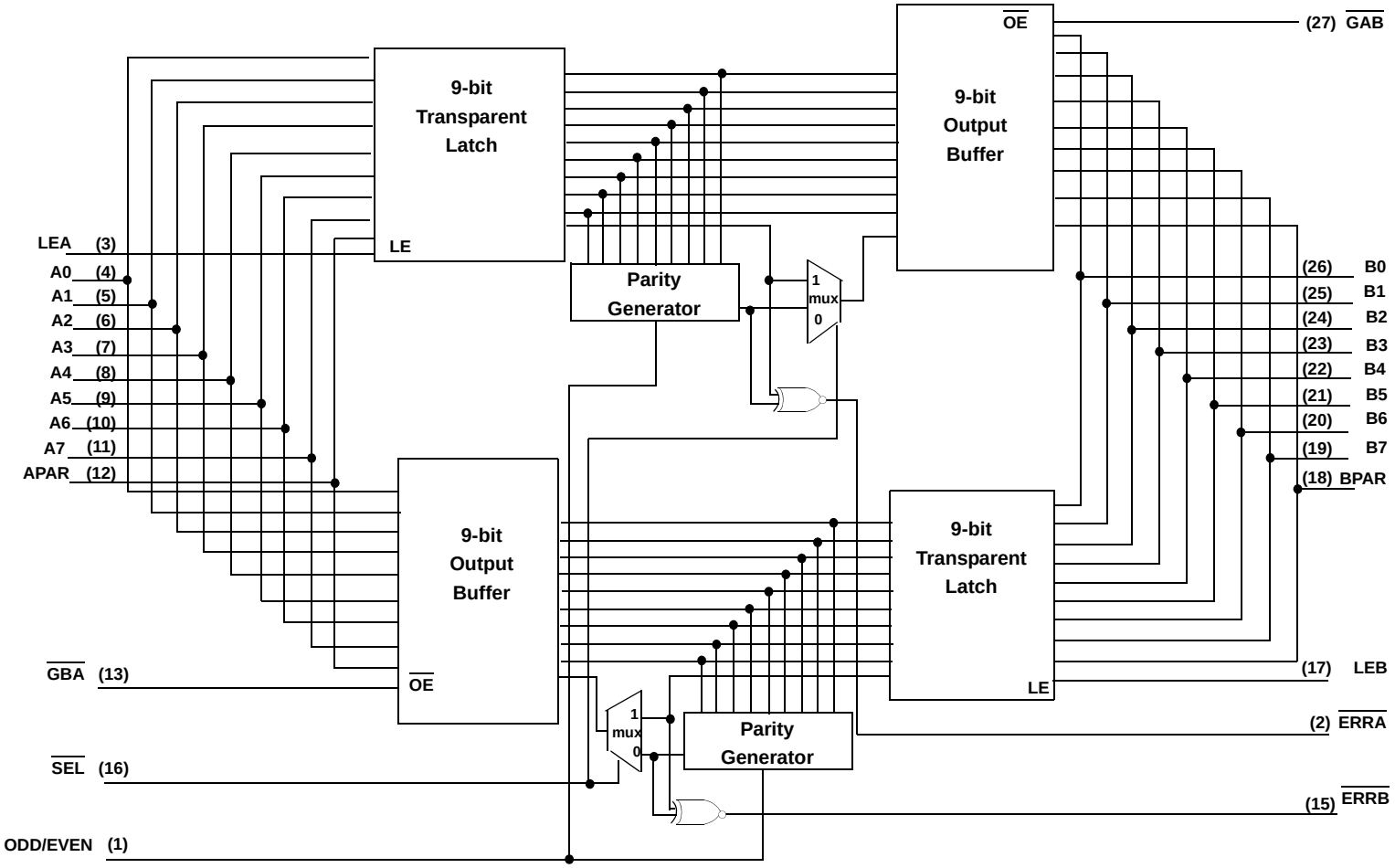
PIN DESCRIPTION

Inputs	Outputs
A0-A7	A Bus Data Inputs/Data Outputs
B0-B7	B Bus Data Inputs/Data Outputs
APAR, BPAR	A and B Bus Parity Inputs
ODD/$\overline{\text{EVEN}}$	ODD/$\overline{\text{EVEN}}$ Parity Select, Active LOW for EVEN Parity
$\overline{\text{GBA}}$, $\overline{\text{GAB}}$	Output Enables for A or B Bus, Active Low
$\overline{\text{SEL}}$	Select Pin for Feed-through or Generate Mode, LOW for Generate Mode
LEA, LEB	Latch Enables for A and B Latches, HIGH for Transparent Mode
$\overline{\text{ERRA}}$, $\overline{\text{ERRB}}$	Error Signals for Checking Generated Parity with Parity In, LOW if Error Occurs

28-Lead Flatpack
Pinout



LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The UT54ACTS899 has three principal modes of operation which are outlined below. These modes apply to both A-to-B and B-to-A directions.

- Bus A (B) communicates to Bus B (A), parity is generated and passed on to the B (A) Bus as BPAR (APAR). If LEB (LEA) is HIGH and the Mode Select ($\overline{SEL}$) is LOW, the parity generated from B[0:7] (A[0:7]) can be checked and monitored by $\overline{ERRB}$ ($\overline{ERRA}$).
- Bus A (B) communicates to Bus B (A) in a feed-through mode if $\overline{SEL}$ is HIGH. Parity is still generated and checked as $\overline{ERRA}$ and $\overline{ERRB}$ in the feed-through mode (can be used as an interrupt to signal a data/parity bit error to the CPU).
- Independent Latch Enables (LEA and LEB) allow other permutations of generating/checking. (see Function Table below)

FUNCTIONAL TABLE

INPUTS					OPERATION
$\overline{GAB}$	$\overline{GBA}$	$\overline{SEL}$	LEA	LEB	
H	H	X	X	X	Busses A and B are Tri-State (input A & B simultaneously)
H	L	L	L	H	Generates parity from B[0:7] based on O/$\overline{E}$ (Note 1). Generated parity --> APAR. Generated parity checked against BPAR and output as $\overline{ERRB}$.
H	L	L	H	H	Generates parity from B[0:7] based on O/$\overline{E}$. Generated parity --> APAR. Generated parity checked against BPAR and output as $\overline{ERRB}$. Generated parity also fed back through the A latch for generate/check as $\overline{ERRA}$.
H	L	L	X	L	Generates parity from B latch data based on O/$\overline{E}$. Generated parity --> APAR. Generated parity checked against latched BPAR and output as $\overline{ERRB}$.
H	L	H	X	H	BPAR/B[0:7] --> APAR/A[0:7] Feed-through mode. Generated parity checked against BPAR and output as $\overline{ERRB}$.
H	L	H	H	H	BPAR/B[0:7] --> APAR/A[0:7] Feed-through mode. Generated parity checked against BPAR and output as $\overline{ERRB}$. APAR/A[0:7] fed back through the A latch for generate/check as $\overline{ERRA}$.
L	H	L	H	L	Generates parity from A[0:7] based on O/$\overline{E}$. Generated parity --> BPAR. Generated parity checked against APAR and output as $\overline{ERRA}$.
L	H	L	H	H	Generates parity from A[0:7] based on O/$\overline{E}$. Generated parity --> BPAR. Generated parity checked against APAR and output as $\overline{ERRA}$. Generated parity also fed back through the B latch for generate/check as $\overline{ERRB}$.
L	H	L	L	X	Generates parity from A latch data based on O/$\overline{E}$. Generated parity --> BPAR. Generated parity checked against latched APAR and output as $\overline{ERRA}$.
L	H	H	H	L	APAR/A[0:7)]--> BPAR/B[0:7] Feed-through mode. Generated parity checked against APAR and output as $\overline{ERRA}$.
L	H	H	H	H	APAR/A[0:7] --> BPAR/B[0:7] Feed-through mode. Generated parity checked against APAR and output as $\overline{ERRA}$. BPAR/B[0:7] fed back through the B latch for generate/check as $\overline{ERRB}$.
L	L	X	X	X	Output to A bus and B bus (NOT ALLOWED).

H = High voltage level
L = Low voltage level
X = Do not care
Note 1: O/$\overline{E}$ = ODD/$\overline{EVEN}$

RADIATION HARDNESS SPECIFICATIONS [1]

PARAMETER	LIMIT	UNITS
Total Dose	1.0E5	rads(Si)
SEU Onset LET	>108	MeV-cm^2/mg
SEL Immune	>108	MeV-cm^2/mg
Neutron Fluence[2]	1.0E14	n/cm^2

Notes:
1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Not tested, inherent of CMOS technology.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	LIMIT	UNITS
V_{DD}	Supply voltage	-0.3 to 6.0	V
$V_{I/O}$	Voltage any pin during operation	-0.3 to V_{DD} +0.3	V
T_{STG}	Storage Temperature range	-65 to +150	°C
T_J	Maximum junction temperature	+175	°C
Θ_{JC}	Thermal resistance junction to case	20	°C/W
I_I	DC input current	$\pm$10	mA
P_D	Maximum power dissipation	220	mW

Note:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V_{DD}	Supply voltage	4.5 to 5.5	V
V_{IN}	Input voltage any pin	0 to V_{DD}	V
T_C	Temperature range	-55 to +125	^oC
t_{INRISE} t_{INFALL}	Maximum input rise or fall time (V_{IN} transitioning between V_{IL} (max) and V_{IH} (min))	20	ns

DC ELECTRICAL CHARACTERISTICS* [1]

(VDD = 3.3 ± 0.3V, T_C = -55°C to +125°C); Unless otherwise noted, Tc is per the temperature ordered

SYMBOL	PARAMETER	CONDITION		MIN	MAX	UNIT
V_{IL}	Low level input voltage[2]	V_{DD} from 4.5V to 5.5V			0.8	V
V_{IH}	High level input voltage[2]	V_{DD} from 4.5V to 5.5V		2.0		V
I_{IN}	Input leakage current	V_{DD} from 4.5 to 5.5 V_{IN} = V_{DD} or V_{SS}		-1	1	µA
I_{OZ}	Three-state output leakage current	V_{DD} from 4.5 to 5.5 V_{IN} = V_{DD} or V_{SS}		-10	10	µA
I_{OS}	Short-circuit output current[3, 4]	V_O = V_{DD} or V_{SS} V_{DD} from 4.5 to 5.5		-600	600	mA
V_{OL1}	Low-level output voltage[5]	I_{OL}= 24mA	-55C, +25°C		0.4	V
		I_{OL}= 24mA	+125°C		0.5	
		I_{OL}= 100µA V_{IN} = 2.0V or 0.8V V_{DD} = 4.5 to 5.5			0.2	
V_{OL2}	Low-level output voltage[5, 6]	I_{OL}= 50mA	-55C, +25°C		0.8	V
		V_{IN} = 2.0V or 0.8V V_{DD} = 5.5V	+125°C		1.0	
V_{OH1}	High-level output voltage[5]	I_{OH}= -24mA	-55, +25°C	V_{DD} - 0.64		V
		I_{OH}= -24mA	+125°C	V_{DD} - 0.8		
		I_{OH}= -100µA V_{IN} = 2.0V or 0.8V V_{DD} = 4.5 to 5.5V		V_{DD} - 0.2		
V_{OH2}	High-level output voltage[5, 6]	I_{OH}= -50mA	-55C, 25°C	V_{DD} -1.1		V
		V_{IN} = 2.0V or 0.8V V_{DD} = 5.5V	+125°C	V_{DD} -1.25		
V_{IC}+	Positive input clamp voltage	For input under test, I_{IN} = +18mA V_{DD} = 0.0V		0.4	1.5	V
V_{IC}-	Negative input clamp voltage	For input under test, I_{IN} = -18mA V_{DD} = open		-1.5	-0.4	V

P_{total}	Power dissipation[7, 8, 9]	C_L = 20pF V_{DD} from 4.5 to 5.5		1.0	mW/ MHz
I_{DDQ}	Standby Supply Current V_{DD} Pre-Rad 25°C Pre-Rad -55°C to +125°C Post-Rad 25°C	V_{IN} = V_{DD} or V_{SS} V_{DD} = 5.5 $\overline{OE}$=V_{DD} $\overline{OE}$=V_{DD} $\overline{OE}$=V_{DD}		 10 160	 µA µA
ΔI_{DDQ}	Quiescent Supply Current Delta, TTL input level Pre-Rad 25°C, Pre-Rad -55°C to +125°C Post-Rad 25°C	For input under test V_{IN} = V_{DD} - 2.1V For other inputs V_{IN} = V_{DD} or V_{SS} V_{DD} = 5.5V		1.6	mA
C_{IN}	Input capacitance [10]	*f* = 1MHz @ 0V V_{DD} from 4.5 to 5.5		21	pF
C_{OUT}	Output capacitance[10]	*f* = 1MHz @ 0V V_{DD} from 4.5 to 5.5		21	pF

Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25×C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. All specifications valid for radiation dose ≤ 1E5 rad(Si) per MIL-STD-883, Method 1019.
2. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: V_{IH} = V_{IH}(min) + 20%, - 0%; V_{IL} = V_{IL}(max) + 0%, - 50%, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to V_{IH}(min) and V_{IL}(max).
3. Not more than one output may be shorted at a time for maximum duration of one second.
4. Supplied as a design limit, but not guaranteed or tested.
5. Per MIL-PRF-38535, for current density ≤ 5.0E5 amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF-MHz.
6. Transmission driving tests are performed at V_{DD} = 5.5V, only one output loaded at a time with a duration not to exceed 2ms. The test is guaranteed, if not tested, for V_{IN}=V_{IH} minimum or V_{IL} maximum.
7. Power dissipation specified per switching output.
8. Guaranteed by characterization.
9. Power does not include power contribution of any CMOS output sink current.
10. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.

AC ELECTRICAL CHARACTERISTICS [1]

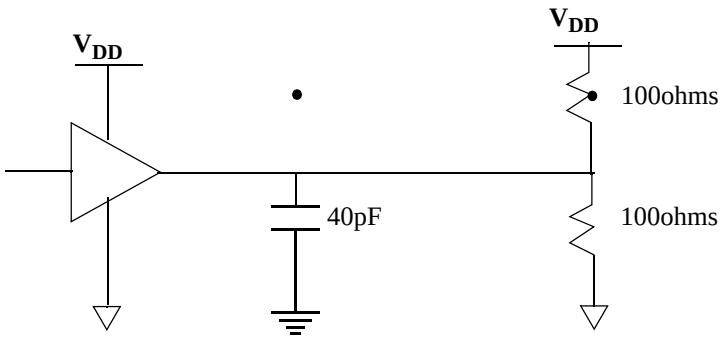
(VDD = 3.3 ± 0.3V, T_C = -55°C to +125°C); Unless otherwise noted, Tc is per the temperature ordered)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t_{PHL1}	Propagation Delay - An, Bn to Bn, An	4.0	11.5	ns
t_{PLH1}	Propagation Delay - An, Bn to Bn, An	4.0	11.5	ns
t_{PHL2}	Propagation Delay - APAR, BPAR to BPAR, APAR	4.0	11.5	ns
t_{PLH2}	Propagation Delay - APAR, BPAR to BPAR, APAR	4.0	11.5	ns
t_{PHL3}	Propagation Delay - An, Bn to BPAR, APAR	5.0	12.0	ns
t_{PLH3}	Propagation Delay - An, Bn to BPAR, APAR	5.0	12.0	ns
t_{PHL4}	Propagation Delay - An, Bn to $\overline{ERRA}$, $\overline{ERRB}$	5.0	12.0	ns
t_{PLH4}	Propagation Delay - An, Bn to $\overline{ERRA}$, $\overline{ERRB}$	5.0	12.0	ns
t_{PHL5}	Propagation Delay - ODD/$\overline{EVEN}$ to $\overline{ERRA}$, $\overline{ERRB}$	4.0	9.0	ns
t_{PLH5}	Propagation Delay - ODD/$\overline{EVEN}$ to $\overline{ERRA}$, $\overline{ERRB}$	4.0	9.0	ns
t_{PHL6}	Propagation Delay - ODD/$\overline{EVEN}$ to APAR, BPAR	4.0	9.0	ns
t_{PLH6}	Propagation Delay - ODD/$\overline{EVEN}$ to APAR, BPAR	4.0	9.0	ns
t_{PHL7}	Propagation Delay - APAR, BPAR to $\overline{ERRA}$, $\overline{ERRB}$	4.0	9.0	ns
t_{PLH7}	Propagation Delay - APAR, BPAR to $\overline{ERRA}$, $\overline{ERRB}$	4.0	9.0	ns
t_{PHL8}	Propagation Delay - $\overline{SEL}$ to APAR, BPAR	3.5	8.5	ns
t_{PLH8}	Propagation Delay - $\overline{SEL}$ to APAR, BPAR	3.5	8.5	ns
t_{PHL9}	Propagation Delay - LEA, LEB to Bn, An	3.5	8.5	ns
t_{PLH9}	Propagation Delay - LEA, LEB to An, Bn	3.5	8.5	ns
t_{PHL10}	Propagation Delay - LEA, LEB to BPAR, APAR	4.0	9.0	ns
t_{PLH10}	Propagation Delay - LEA, LEB to APAR, BPAR	4.0	9.0	ns
t_{PHL11}	Propagation Delay - LEA, LEB to $\overline{ERRA}$, $\overline{ERRB}$	5.0	12.0	ns
t_{PLH11}	Propagation Delay - LEA, LEB to $\overline{ERRA}$, $\overline{ERRB}$	5.0	12.0	ns
t_{PZH1}	Output Enable Time - $\overline{GBA}$ or $\overline{GAB}$ to An, Bn	3.5	9.5	ns

t_{PZL1}	Output Enable Time - $\overline{GBA}$ or $\overline{GAB}$ to An, Bn	3.5	9.5	ns
t_{PZH2}	Output Enable Time - $\overline{GBA}$ or $\overline{GAB}$ to BPAR or APAR	3.5	9.5	ns
t_{PZL2}	Output Enable Time - $\overline{GBA}$ or $\overline{GAB}$ to BPAR or APAR	3.5	9.5	ns
t_{PHZ1}	Output Disable Time - $\overline{GBA}$ or $\overline{GAB}$ to An, Bn	2.0	6.0	ns
t_{PLZ1}	Output Disable Time - $\overline{GBA}$ or $\overline{GAB}$ to An, Bn	2.0	6.0	ns
t_{PHZ2}	Output Disable Time - $\overline{GBA}$ or $\overline{GAB}$ to BPAR, to APAR	2.0	6.0	ns
t_{PLZ2}	Output Disable Time - $\overline{GBA}$ or $\overline{GAB}$ to BPAR, to APAR	2.0	6.0	ns
t_S	Setup Time, High or Low, An, Bn, APAR, BPAR to LEA, LEB	1.0		ns
t_H	Hold Time, High or Low, An, Bn, APAR, BPAR to LEA, LEB	1.5		ns
t_W[2]	Pulse Width for LEA, LEB	4.0		ns
f_{MAX}[2]	Maximum clock frequency		80	MHz

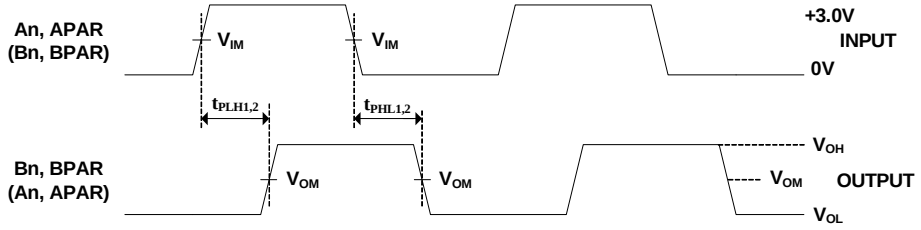
Notes:
* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25×C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.
1. All specifications valid for radiation >1E5 rads(Si) per MIL-STD-883, Method 1019.
2. Verified by functional test.

Test Load or Equivalent[1]



Notes
1. Equivalent test circuit means that DUT performance will be correlated and remain guaranteed to the applicable test circuit, above, whenever a test platform change necessitates a deviation from the applicable test circuit.

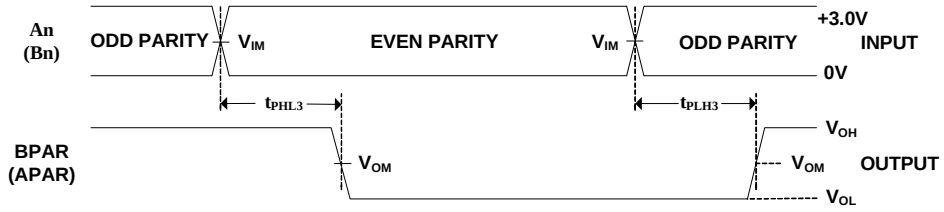
AC TIMING DIAGRAMS



Note:
1. V_{IM} = 1.5V, $V_{OM} = V_{DD}/2$

2. $\overline{SEL}$ = 3.0V = H

Figure 1. Propagation Delay, An to Bn, Bn to An, APAR to BPAR, BPAR to APAR

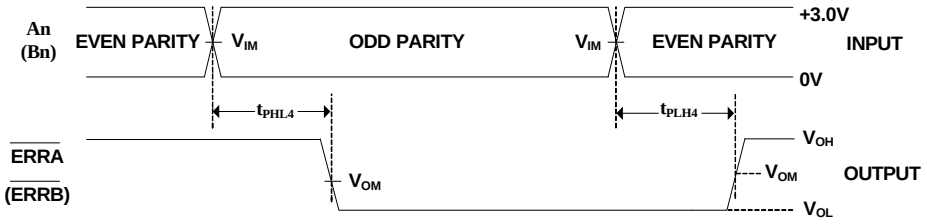


Note:
1. V_{IM} = 1.5V, $V_{OM} = V_{DD}/2$

2. SEL = ODD/$\overline{EVEN}$ = V_{SS} = L

3. LEA (LEB) = 3.0V = H

Figure 2. Propagation Delay, An to BPAR, or Bn to APAR (with Even Parity Mode Shown)

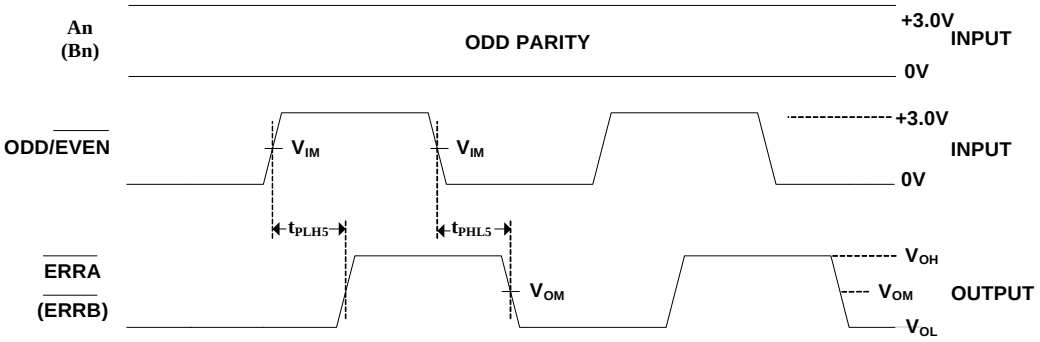


Note:
1. V_{IM} = 1.5V, $V_{OM} = V_{DD}/2$

2. APAR (BPAR) = ODD/$\overline{EVEN}$ = V_{SS} = L

3. LEA (LEB) = 3.0V = H

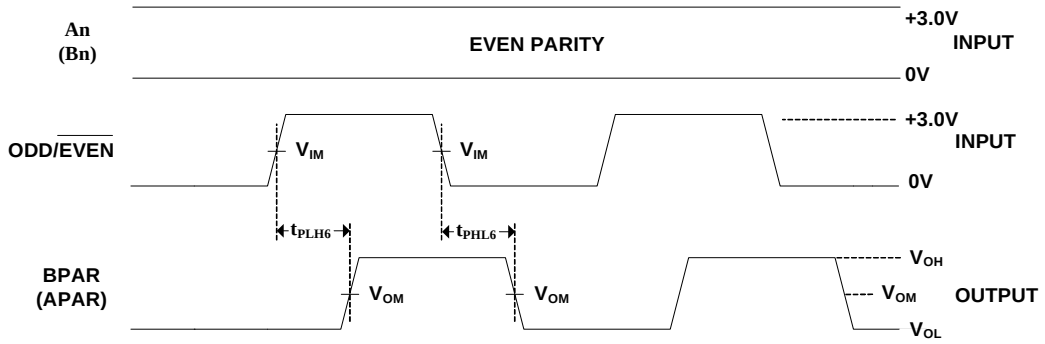
Figure 3. Propagation Delay, An to $\overline{ERRA}$ or Bn to $\overline{ERRB}$ (with Even Parity Mode Shown)



Note:
1. V_{IM} = 1.5V, $V_{OM} = V_{DD}/2$

2. APAR (BPAR) = V_{SS} = L

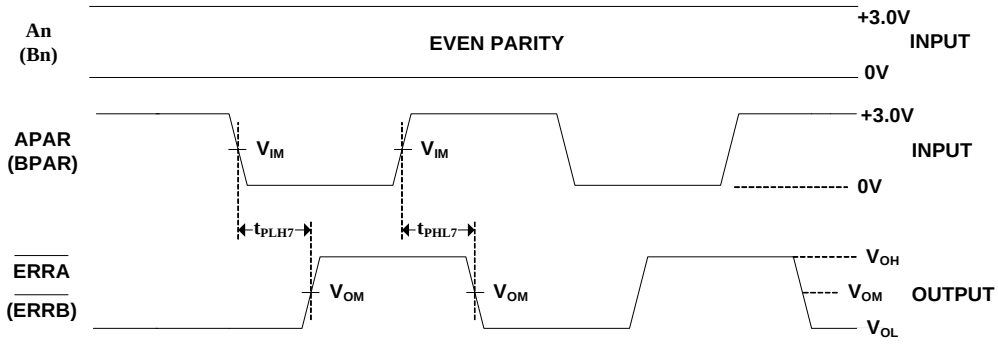
Figure 4. Propagation Delay, ODD/$\overline{EVEN}$ to $\overline{ERRA}$ or ODD/$\overline{EVEN}$ to $\overline{ERRB}$



Note:
1. V_{IM} = 1.5V, $V_{OM} = V_{DD}/2$

2. SEL = APAR (BPAR) = V_{SS} = L

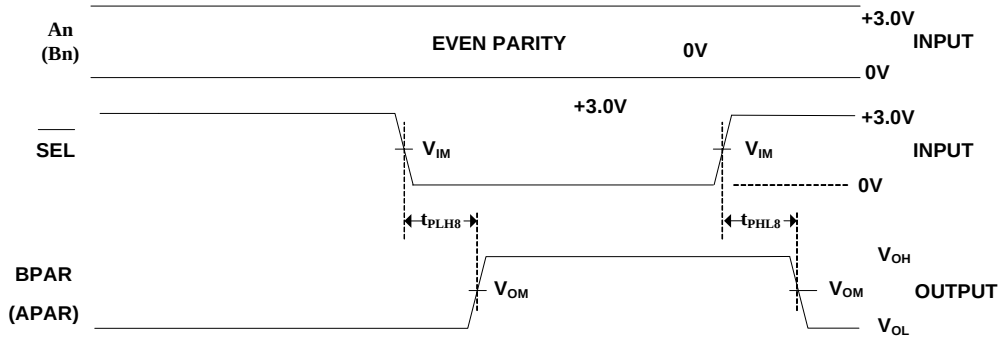
Figure 5. Propagation Delay, ODD/$\overline{\text{EVEN}}$ to APAR or ODD/$\overline{\text{EVEN}}$ to BPAR (with Even Parity Mode Shown)



Note:
1. V_{IM} = 1.5V, $V_{OM} = V_{DD}/2$

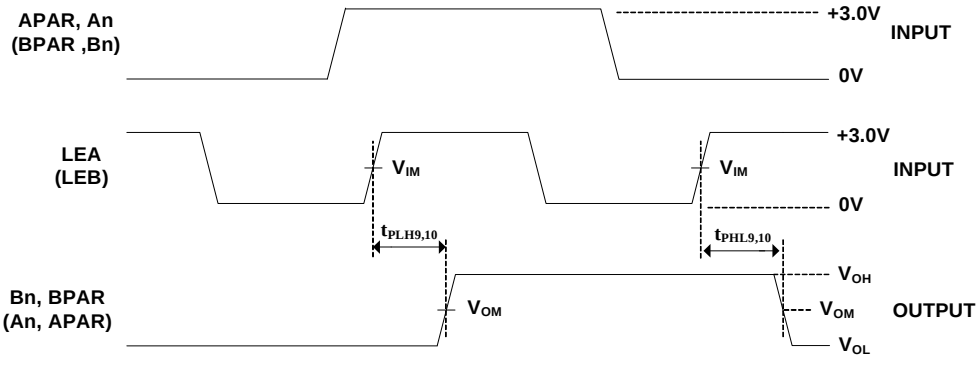
2. ODD/$\overline{\text{EVEN}}$ = V_{SS} = L

Figure 6. Propagation Delay, APAR to $\overline{\text{ERRA}}$ or BPAR to $\overline{\text{ERRB}}$
(With Even Parity Mode Shown with Even Data Parity. Odd Parity Mode would cause Inverted Output.)



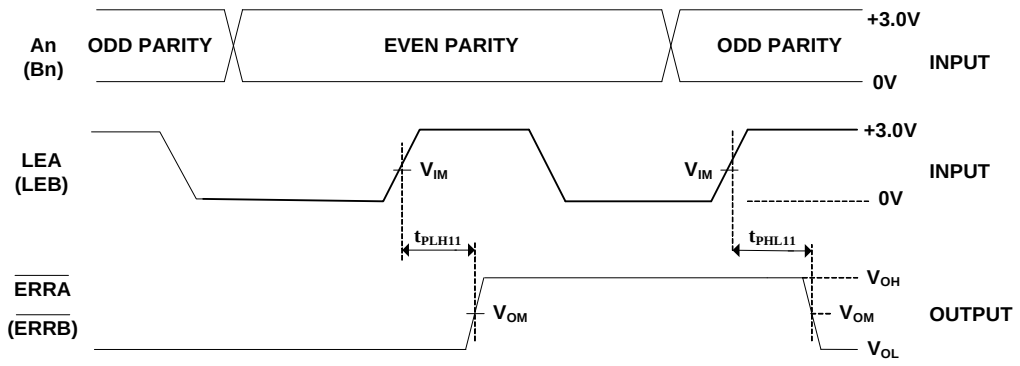
Note:
1. V_{IM} = 1.5V, $V_{OM} = V_{DD}/2$
2. ODD/$\overline{\text{EVEN}}$ = 3.0V = H
3. APAR (BPAR) = V_{SS} = L

Figure 7. Propagation Delay, $\overline{\text{SEL}}$ to BPAR or $\overline{\text{SEL}}$ to APAR
(With Odd Parity Mode Shown with Even Data Parity. Even Parity Mode would cause Inverted Output.)



Note:
1. V_{IM} = 1.5V, $V_{OM} = V_{DD}/2$
2. $\overline{\text{SEL}}$ = 3.0V = H

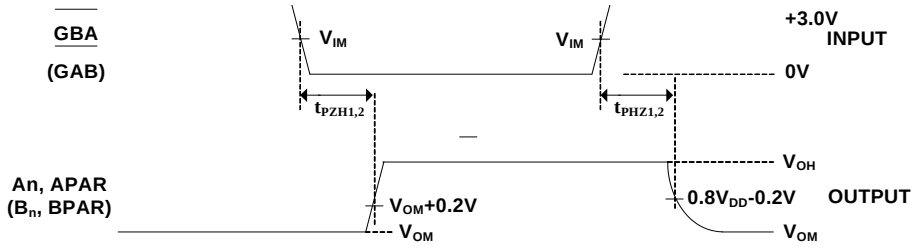
Figure 8. Propagation Delay, LEA to BPAR or LEB to APAR, LEA to Bn or LEB to An



Note:
1. V_{IM} = 1.5V, V_{OM} = V_{DD}/2

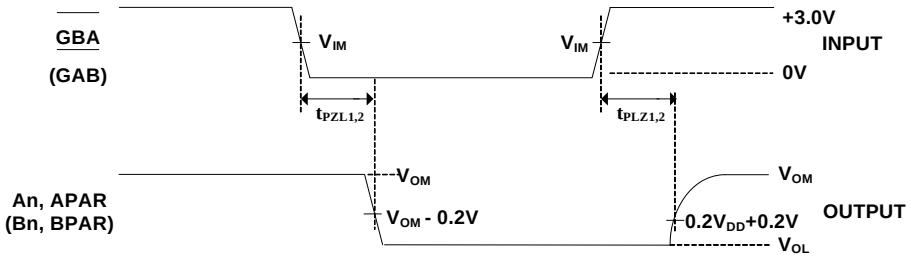
2. APAR (BPAR) = ODD/$\overline{\text{EVEN}}$ = 3.0V = H

Figure 9. Propagation Delay, LEA to $\overline{\text{ERRA}}$ or LEB to $\overline{\text{ERRB}}$ (with Odd Parity Mode Shown)



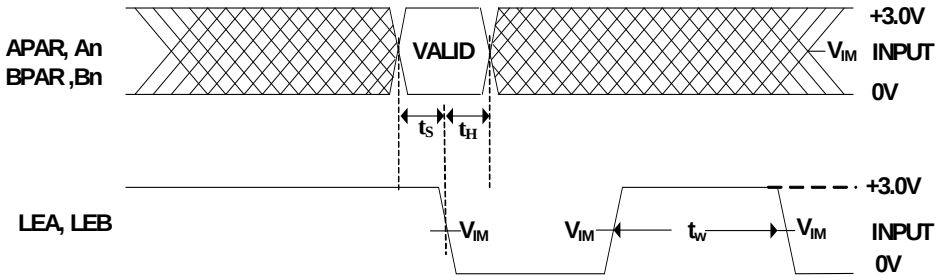
Note:
1. V_{IM} = 1.5V, V_{OM} = V_{DD}/2

Figure 10. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Note:
1. V_{IM} = 1.5V, V_{OM} = V_{DD}/2

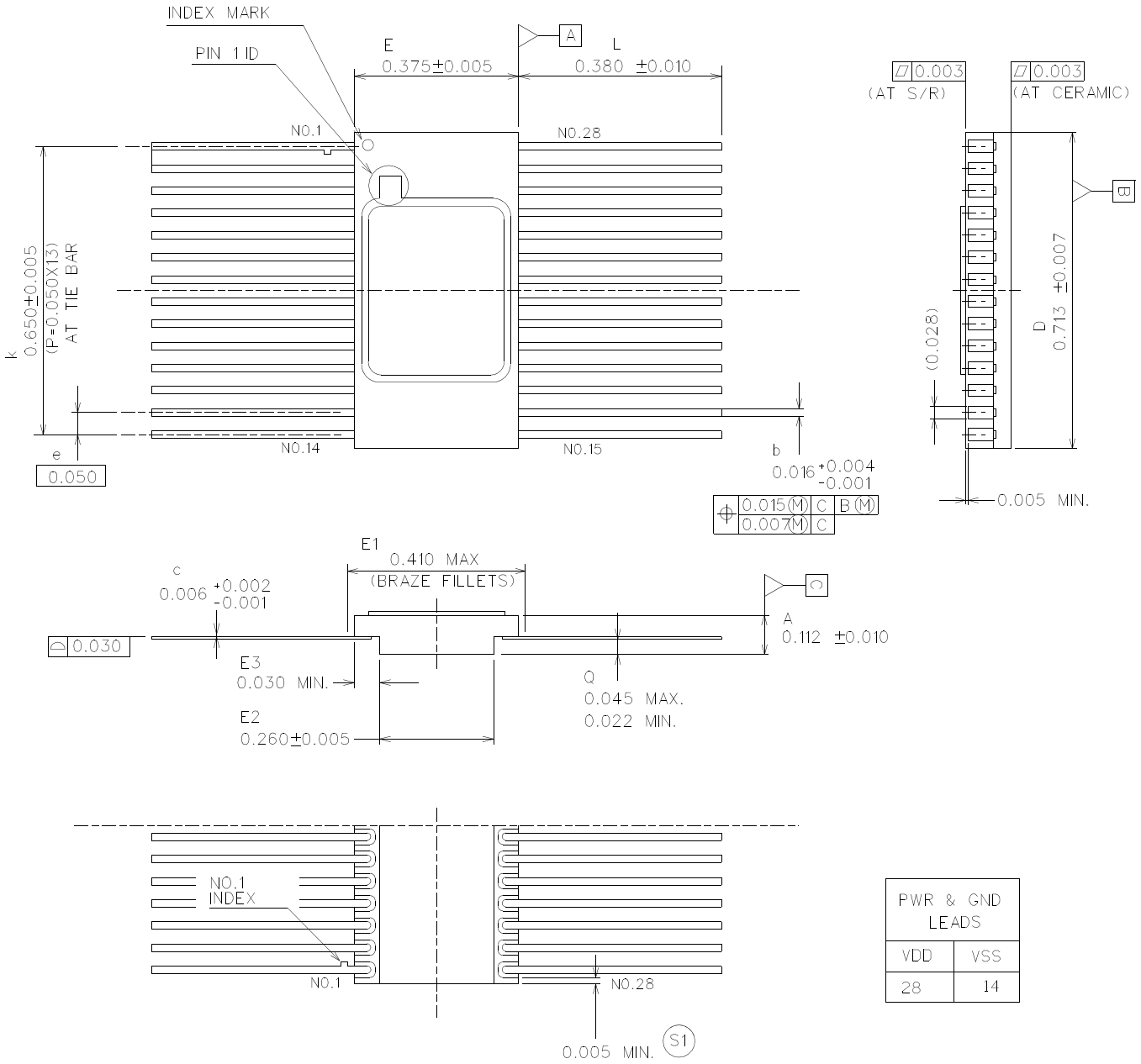
Figure 11. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level



Note:
1. V_{IM} = 1.5V, V_{OM} = V_{DD}/2

Figure 12. Data Setup and Hold Times, Pulse Width High

Packaging



PWR & GND LEADS	
VDD	VSS
28	14

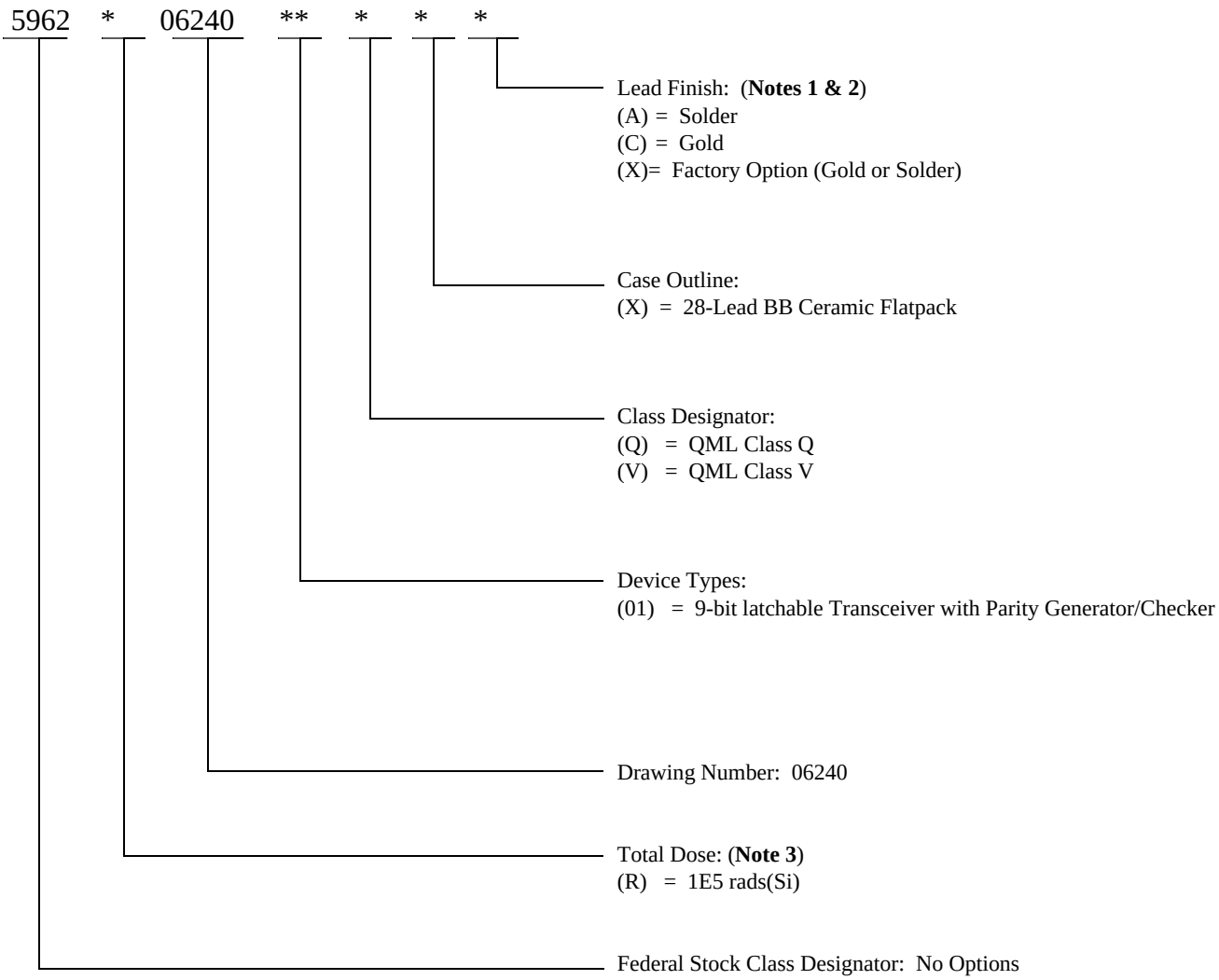
NOTE:

1. Seal ring is connected to V_{SS}.
2. Units are in inches.
3. All exposed metalized areas must be gold plated 100 to 225 microinches thick and all bottom side exposed metalized areas must be gold plated to 60 microinches thick nominal. Both sides shall be over electroplated nickel undercoating 100 to 350 microinches per MIL-PRF-38535.

Figure 13. 28-pin Ceramic Flatpack

ORDERING INFORMATION

UT54ACTS899: SMD



Notes:

1. Lead finish (A, C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Total dose radiation must be specified when ordering. QML-Q and QML-V are not available without radiation hardening. For prototyping inquiries, contact factory.

Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced Hi-Rel

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