

UT54ACTS00E

Quadruple 2-Input NAND Gates

April 2015

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Datasheet

FEATURES

- 0.6μm CRH CMOS process
 - Latchup immune
- High speed
- Low power consumption
- Wide power supply operating range from 3.0V to 5.5V
- Available QML Q or V processes
- 14-lead flatpack
- UT54ACTS00E - SMD 5962-96513

DESCRIPTION

The UT54ACTS00E is a performance and voltage enhanced version of the UT54ACTS00 quadruple, two-input NAND gate. The circuit performs the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

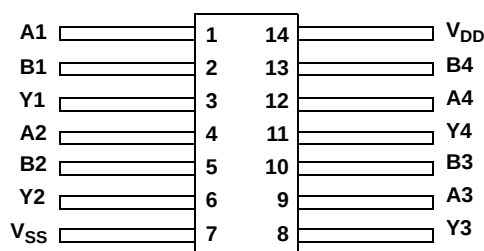
The device is characterized over full military temperature range of -55°C to +125°C.

FUNCTION TABLE

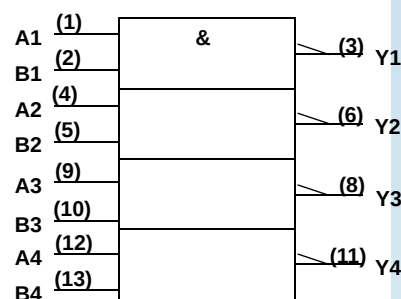
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

PINOUT

**14-Lead Flatpack
TopView**



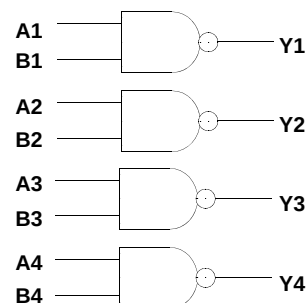
LOGIC SYMBOL



Note:

1. Logic symbol in accordance with ANSI/IEEE standard 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM



OPERATIONAL ENVIRONMENT ¹

PARAMETER	LIMIT	UNITS
Total Dose	1.0E6	rads(Si)
SEU Threshold ²	108	MeV-cm ² /mg
SEL Threshold	120	MeV-cm ² /mg
Neutron Fluence	1.0E14	n/cm ²

Notes:

1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Device storage elements are immune to SEU affects.

ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	LIMIT	UNITS
V _{DD}	Supply voltage	-0.3 to 7.0	V
V _{I/O}	Voltage any pin	-0.3 to V _{DD} +0.3	V
T _{STG}	Storage Temperature range	-65 to +150	°C
T _J	Maximum junction temperature	+175	°C
T _{LS}	Lead temperature (soldering 5 seconds)	+300	°C
Θ _{JC}	Thermal resistance junction to case	15	°C/W
I _I	DC input current	±10	mA
P _D ²	Maximum package power dissipation permitted @ T _C = +125°C	3.2	W

Note:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Per MIL-STD-883, method 1012.1, Section 3.4.1, $P_D = (T_{J(max)} - T_{C(max)}) / \Theta_{JC}$

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V _{DD}	Supply voltage	3.0 to 5.5	V
V _{IN}	Input voltage any pin	0 to V _{DD}	V
T _C	Temperature range	-55 to + 125	°C

DC ELECTRICAL CHARACTERISTICS FOR THE UT54ACTS00E⁷($V_{DD} = 3.0V$ to $5.5V$; $V_{SS} = 0V$ ⁶; $-55^{\circ}C < T_C < +125^{\circ}C$)

SYMBOL	DESCRIPTION	CONDITION	MIN	MAX	UNIT
V_{IL1}	Low-level input voltage ¹	V_{DD} from 4.5V to 5.5V		0.8	V
V_{IL2}	Low-level input voltage ¹	V_{DD} from 3.0V to 3.6V		0.8	V
V_{IH1}	High-level input voltage ¹	V_{DD} from 4.5V to 5.5V	0.5 V_{DD}		V
V_{IH2}	High-level input voltage ¹	V_{DD} from 3.0V to 3.6V	2.0		V
I_{IN}	Input leakage current	$V_{IN} = V_{DD}$ or V_{SS}	-1	1	μA
V_{OL1}	Low-level output voltage ³	$I_{OL} = 8mA$ $V_{DD} = 4.5V$ to $5.5V$		0.4	V
V_{OL2}	Low-level output voltage ³	$I_{OL} = 6mA$ $V_{DD} = 3.0V$ to $3.6V$		0.4	V
V_{OH1}	High-level output voltage ³	$I_{OH} = -8mA$ V_{DD} from 4.5V to 5.5V	0.7 V_{DD}		V
V_{OH2}	High-level output voltage ³	$I_{OH} = -6mA$ V_{DD} from 3.0V to 3.6V	2.4		V
I_{OS1}	Short-circuit output current ^{2,4}	$V_O = V_{DD}$ and V_{SS} V_{DD} from 4.5V to 5.5V	-200	+200	mA
I_{OS2}	Short-circuit output current ^{2,4}	$V_O = V_{DD}$ and V_{SS} V_{DD} from 3.0V to 3.6V	-100	+100	mA
I_{OL1}	Low level output current ¹⁰	$V_{IN} = V_{DD}$ or V_{SS} $V_{OL} = 0.4V$ V_{DD} from 4.5V to 5.5V	+8		mA
I_{OL2}	Low level output current ¹⁰	$V_{IN} = V_{DD}$ or V_{SS} $V_{OL} = 0.4V$ V_{DD} from 3.0V to 3.6V	+6		mA
I_{OH1}	High level output current ¹⁰	$V_{IN} = V_{DD}$ or V_{SS} $V_{OH} = V_{DD}-0.4V$ V_{DD} from 4.5V to 5.5V	-8		mA
I_{OH2}	High level output current ¹⁰	$V_{IN} = V_{DD}$ or V_{SS} $V_{OH} = V_{DD}-0.4V$ V_{DD} from 3.0V to 3.6V	-6		mA

P_{total1}	Power dissipation ^{2, 8, 9}	$C_L = 50\text{pF}$ $V_{DD} = 4.5\text{V to } 5.5\text{V}$		1	mW/ MHz
P_{total2}	Power dissipation ^{2, 8, 9}	$C_L = 50\text{pF}$ $V_{DD} = 3.0\text{V to } 3.6\text{V}$		0.5	mW/ MHz
I_{DDQ}	Quiescent Supply Current	$V_{IN} = V_{DD} \text{ or } V_{SS}$ $V_{DD} \text{ from } 3.6\text{V to } 5.5\text{V}$		25	μA
ΔI_{DDQ}	Quiescent Supply Current Delta	For input under test $V_{IN} = V_{DD} - 2.1\text{V}$ For all other inputs $V_{IN} = V_{DD} \text{ or } V_{SS}$ $V_{DD} = 5.5\text{V}$		1.6	mA
C_{IN}	Input capacitance ⁵	$f = 1\text{MHz}$ $V_{DD} = 5\text{V}$		15	pF
C_{OUT}	Output capacitance ⁵	$f = 1\text{MHz}$ $V_{DD} = 0\text{V}$		15	pF

Notes:

- Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}(\text{min}) + 20\%$, -0% ; $V_{IL} = V_{IL}(\text{max}) + 0\%$, -50% , as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$.
- Supplied as a design limit but not guaranteed or tested.
- Per MIL-PRF-38535, for current density $\leq 5.0\text{E}5 \text{ amps/cm}^2$, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765pF/MHz.
- Not more than one output may be shorted at a time for maximum duration of one second.
- Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
- Maximum allowable relative shift equals 50mV.
- For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 method 1019 condition A up to the maximum TID level procured.
- Power dissipation specified per switching output.
- Power does not include power contribution of any TTL output sink current.
- Guaranteed by characterization, but not tested.

AC ELECTRICAL CHARACTERISTICS FOR THE UT54ACTS00E²

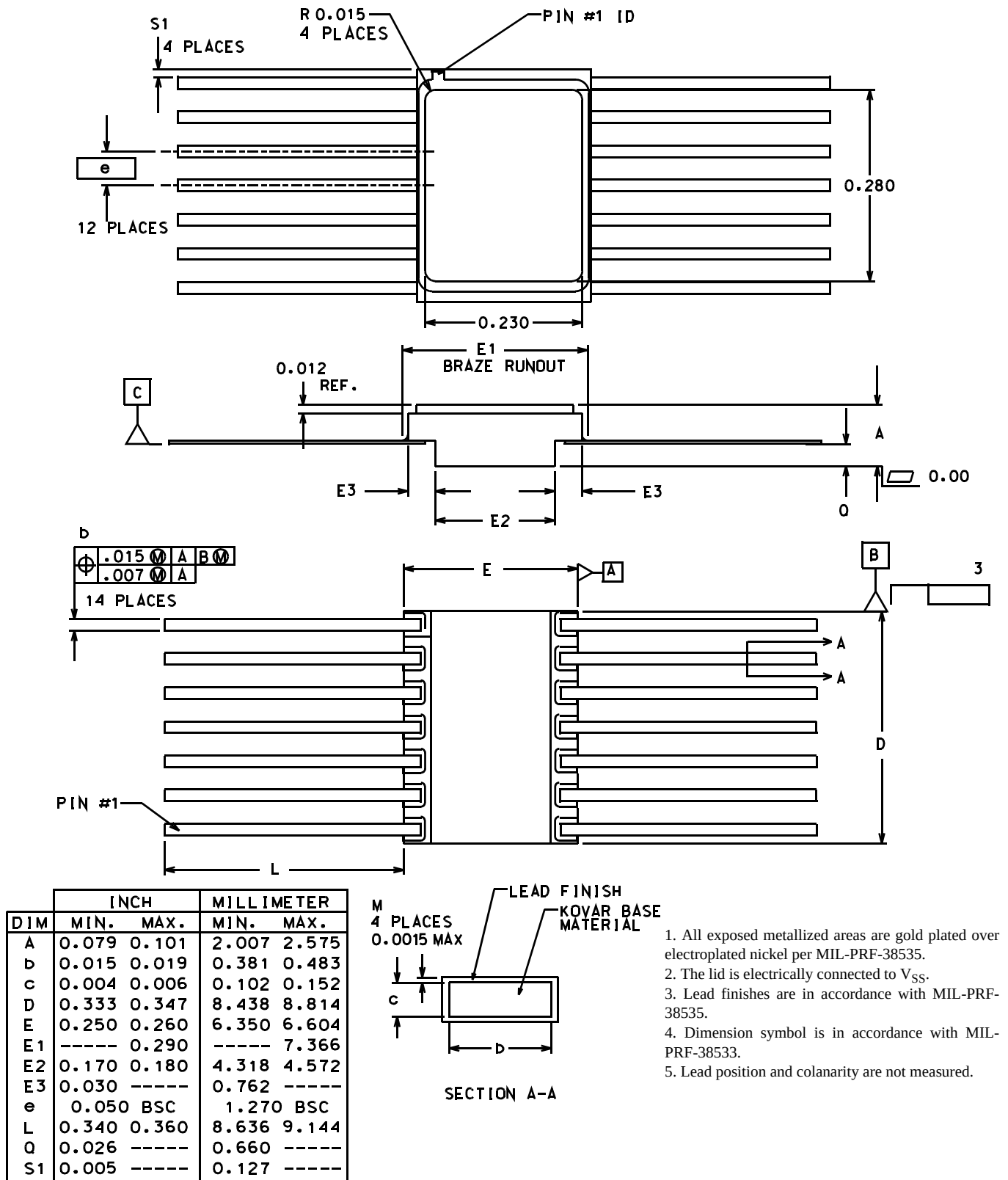
($V_{DD} = 3.0V$ to $5.5V$; $V_{SS} = 0V$ ¹; $-55^{\circ}C < T_C < +125^{\circ}C$)

SYMBOL	PARAMETER	CONDITION	V_{DD}	MINIMUM	MAXIMUM	UNIT
t_{PLH}	Input to Yn	$C_L = 50pF$	4.5V to 5.5V	1	8	ns
			3.0V to 3.6V	3	15	
t_{PHL}	Input to Yn	$C_L = 50pF$	4.5V to 5.5V	1	8	ns
			3.0V to 3.6V	3	15	

Notes:

1. Maximum allowable relative shift equals 50mV.
2. For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 method 1019 condition A up to the maximum TID level procured.

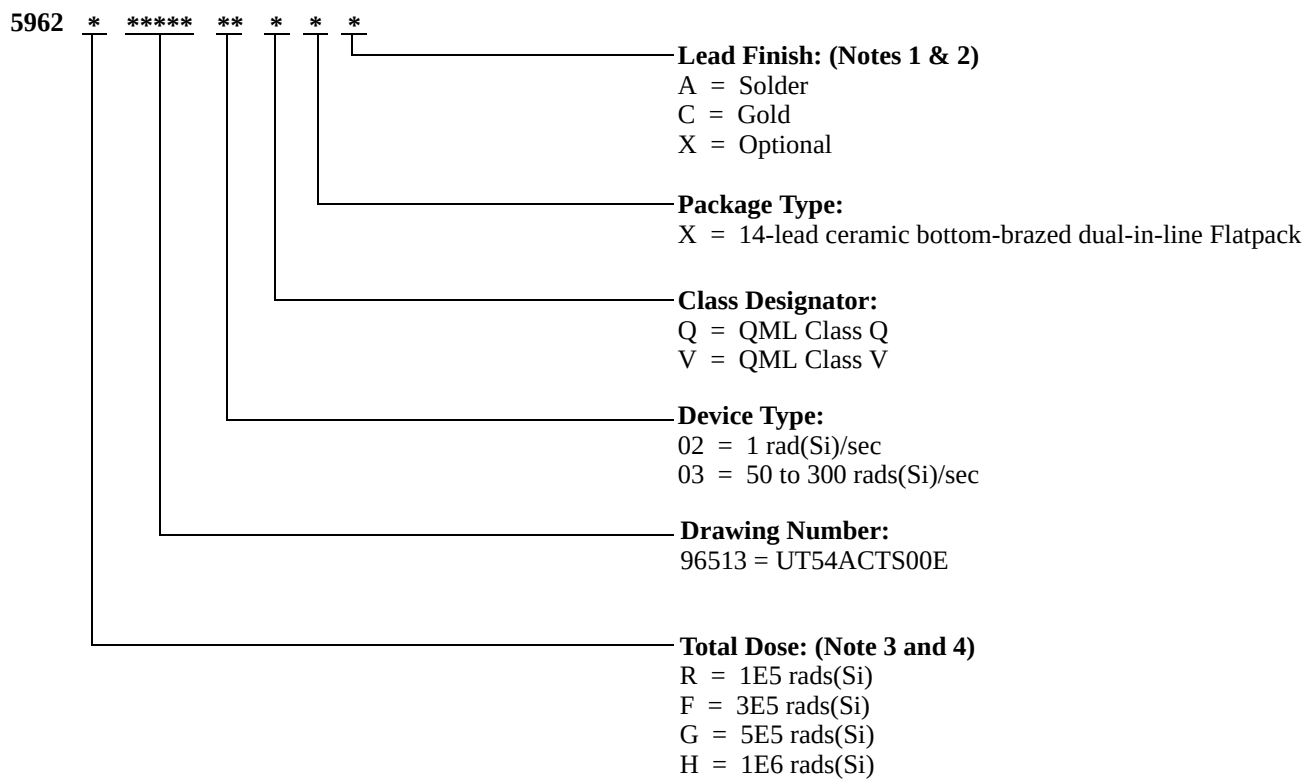
Packaging



1. All exposed metallized areas are gold plated over electroplated nickel per MIL-PRF-38535.
2. The lid is electrically connected to V_{SS} .
3. Lead finishes are in accordance with MIL-PRF-38535.
4. Dimension symbol is in accordance with MIL-PRF-38533.
5. Lead position and colanarity are not measured.

Figure 1. 14 Lead Flatpack

Ordering Information: UT54ACTS00E: SMD



Notes:

- Lead finish (A,C, or X) must be specified.
- If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
- Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening. For prototype inquiries, contact factory.
- Device type 02 is only offered with a TID tolerance guarantee of 3E5 rads(Si) or 1E6 rads(Si) and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A and section 3.11.2. Device type 03 is only offered with a TID tolerance guarantee of 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.

Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced HiRel

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Our passion for performance is defined by three attributes represented by these three icons: solution-minded, performance-driven and customer-focused

Datasheet Revision History

Revision Date	Description of Change
April 2015 Version 1.0.0	Initial Release of Datasheet