

UT54ACS283/UT54ACTS283

4-Bit Binary Full Adders

Datasheet

November 2010

www.aeroflex.com/logic



FEATURES

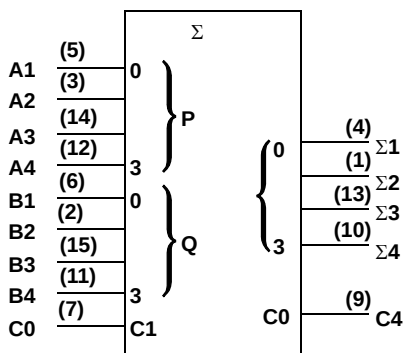
- ❑ 1.2 μ CMOS
 - Latchup immune
- ❑ High speed
- ❑ Low power consumption
- ❑ Single 5 volt supply
- ❑ Available QML Q or V processes
- ❑ Flexible package
 - 16-pin DIP
 - 16-lead flatpack
- ❑ UT54ACS283- SMD 5962-96584
- ❑ UT54ACTS283 - SMD 5962-96585

DESCRIPTION

The UT54ACS283 and the UT54ACTS283 are 4-bit binary adders. The adders perform addition of two 4-bit binary words. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained as the fifth bit. The adders feature full internal look-ahead across all four bits for fast carry generation.

The devices are characterized over full military temperature range of -55°C to +125°C.

LOGIC SYMBOL

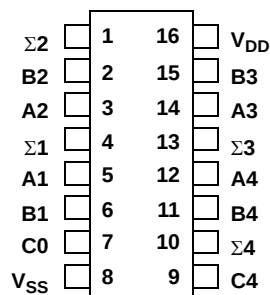


Note:

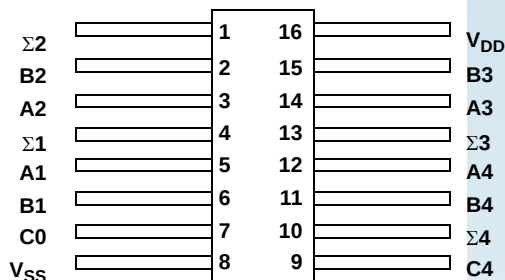
1. Logic symbol in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PINOUTS

16-Pin DIP Top View



16-Lead Flatpack Top View



FUNCTION TABLE

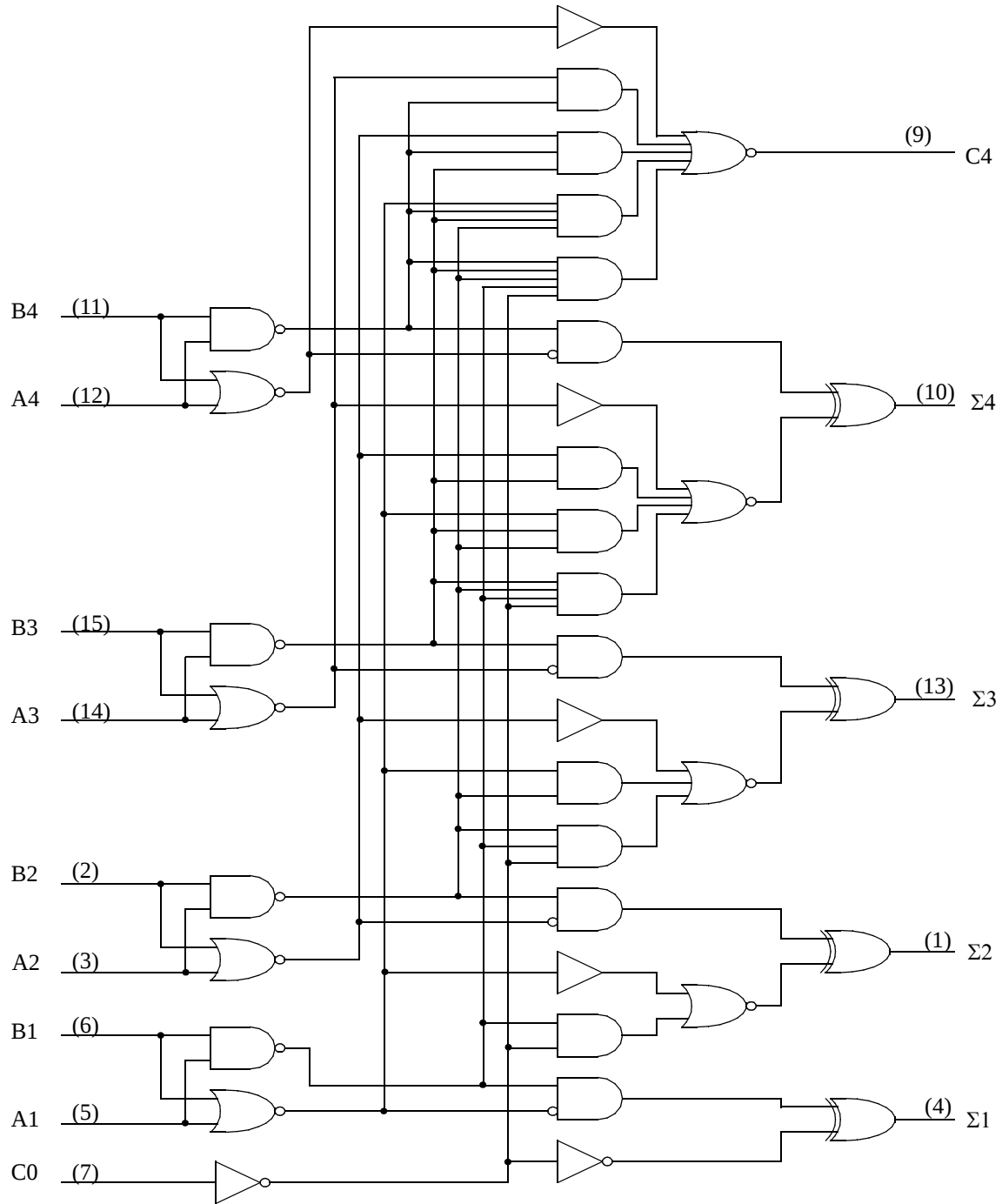
INPUT								OUTPUT											
								When C0 = L			When C2 = L			When C0 = H			When C2 = H		
A1	A3	B1	B3	A2	A4	B2	B4	$\Sigma 1$	$\Sigma 3$	$\Sigma 2$	$\Sigma 4$	C2	C4	$\Sigma 1$	$\Sigma 3$	$\Sigma 2$	$\Sigma 4$	C2	C4
L		L		L		L		L		L		L		H		L		L	
H		L		L		L		H		L		L		L		H		L	
L		H		L		L		H		L		L		L		H		L	
H		H		L		L		L		H		L		H		H		L	
L		L		H		L		L		H		L		H		H		L	
H		L		H		L		H		H		L		L		L		H	
L		H		H		L		H		H		L		L		L		H	
H		H		H		L		L		L		H		H		L		H	
L		L		L		H		L		H		L		H		H		L	
H		L		L		H		H		H		L		L		L		H	
L		H		L		H		H		H		L		L		L		H	
H		H		L		H		L		L		H		H		L		H	
L		L		H		H		L		L		H		H		L		H	
H		L		H		H		H		L		H		L		H		H	
L		H		H		H		H		L		H		L		H		H	
H		H		H		H		L		H		H		H		H		H	

H = high level, L = low level

Note:

Input conditions at A1, A2, B1, B2, and C0 are used to determine outputs $\Sigma 1$ and $\Sigma 2$ and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs $\Sigma 3$, $\Sigma 4$, and C4.

LOGIC DIAGRAM



OPERATIONAL ENVIRONMENT¹

PARAMETER	LIMIT	UNITS
Total Dose	1.0E6	rads(Si)
SEU Threshold ²	80	MeV-cm ² /mg
SEL Threshold	120	MeV-cm ² /mg
Neutron Fluence	1.0E14	n/cm ²

Notes:

1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Device storage elements are immune to SEU affects.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	LIMIT	UNITS
V _{DD}	Supply voltage	-0.3 to 7.0	V
V _{I/O}	Voltage any pin	-.3 to V _{DD} +.3	V
T _{STG}	Storage Temperature range	-65 to +150	°C
T _J	Maximum junction temperature	+175	°C
T _{LS}	Lead temperature (soldering 5 seconds)	+300	°C
Θ _{JC}	Thermal resistance junction to case	20	°C/W
I _I	DC input current	±10	mA
P _D	Maximum power dissipation	1	W

Note:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V _{DD}	Supply voltage	4.5 to 5.5	V
V _{IN}	Input voltage any pin	0 to V _{DD}	V
T _C	Temperature range	-55 to + 125	°C

DC ELECTRICAL CHARACTERISTICS ⁷(V_{DD} = 5.0V ±10%; V_{SS} = 0V ⁶, -55°C < T_C < +125°C); Unless otherwise noted, T_c is per the temperature range ordered.

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V _{IL}	Low-level input voltage ¹ ACTS ACS			0.8 .3V _{DD}	V
V _{IH}	High-level input voltage ¹ ACTS ACS		.5V _{DD} .7V _{DD}		V
I _{IN}	Input leakage current ACTS/ACS	V _{IN} = V _{DD} or V _{SS}	-1	1	μA
V _{OL}	Low-level output voltage ³ ACTS ACS	I _{OL} = 8.0mA I _{OL} = 100μA		0.40 0.25	V
V _{OH}	High-level output voltage ³ ACTS ACS	I _{OH} = -8.0mA I _{OH} = -100μA	.7V _{DD} V _{DD} - 0.25		V
I _{OS}	Short-circuit output current ^{2,4} ACTS/ACS	V _O = V _{DD} and V _{SS}	-200	200	mA
I _{OL}	Output current ¹⁰ (Sink)	V _{IN} = V _{DD} or V _{SS} V _{OL} = 0.4V	8		mA
I _{OH}	Output current ¹⁰ (Source)	V _{IN} = V _{DD} or V _{SS} V _{OH} = V _{DD} - 0.4V	-8		mA
P _{total}	Power dissipation ^{2, 8, 9}	C _L = 50pF		1.9	mW/ MHz
I _{DDQ}	Quiescent Supply Current	V _{DD} = 5.5V		10	μA
ΔI _{DDQ}	Quiescent Supply Current Delta ACTS	For input under test V _{IN} = V _{DD} - 2.1V For all other inputs V _{IN} = V _{DD} or V _{SS} V _{DD} = 5.5V		1.6	mA
C _{IN}	Input capacitance ⁵	f = 1MHz @ 0V		15	pF
C _{OUT}	Output capacitance ⁵	f = 1MHz @ 0V		15	pF

Notes:

1. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH(min)} + 20\%$, $- 0\%$; $V_{IL} = V_{IL(max)} + 0\%$, $- 50\%$, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH(min)}$ and $V_{IL(max)}$.
2. Supplied as a design limit but not guaranteed or tested.
3. Per MIL-PRF-38535, for current density $\leq 5.0E5$ amps/cm², the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF/MHz.
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
6. Maximum allowable relative shift equals 50mV.
7. All specifications valid for radiation dose $\leq 1E6$ rads(Si).
8. Power does not include power contribution of any TTL output sink current.
9. Power dissipation specified per switching output.
10. This value is guaranteed based on characterization data, but not tested.

AC ELECTRICAL CHARACTERISTICS ²

($V_{DD} = 5.0V \pm 10\%$; $V_{SS} = 0V$ ¹, $-55^{\circ}C < T_C < +125^{\circ}C$); Unless otherwise noted, T_C is per the temperature range ordered.

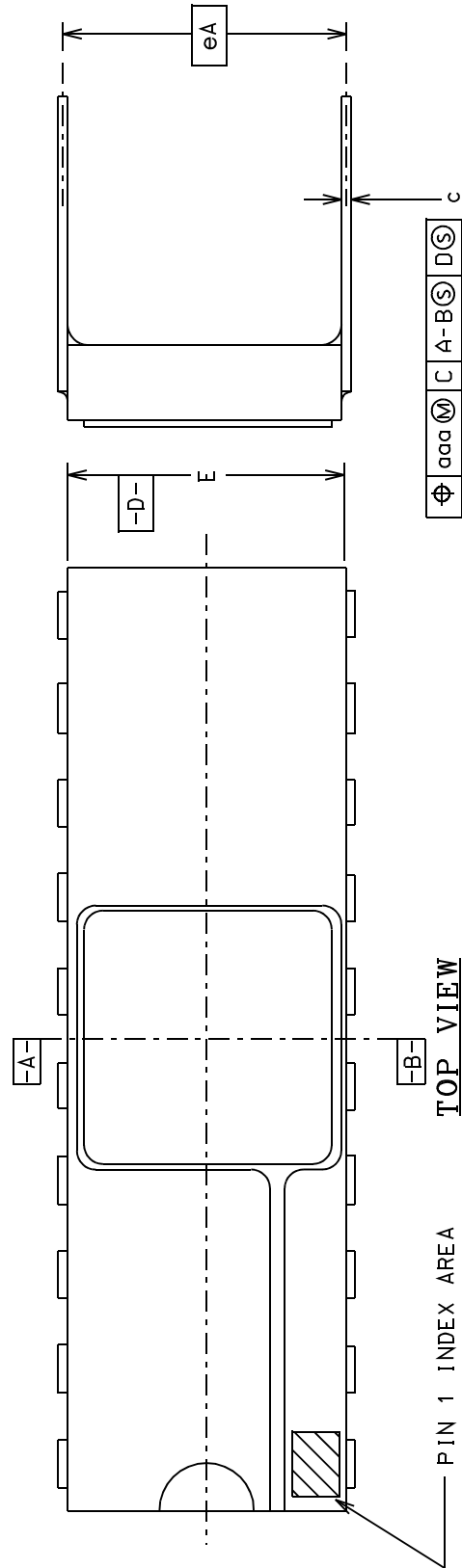
SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t_{PLH}	Propagation delay C0 to Σn	2	16	ns
t_{PHL}	Propagation delay C0 to Σn	2	19	ns
t_{PLH}	Propagation delay C0 to C4	2	16	ns
t_{PHL}	Propagation delay C0 to C4	2	17	ns
t_{PLH}	Propagation delay An, Bn to C4	2	16	ns
t_{PHL}	Propagation delay An, Bn to C4	2	15	ns
t_{PLH}	Propagation delay An, Bn to Σn	2	14	ns
t_{PHL}	Propagation delay An, Bn to Σn	2	16	ns

Notes:

1. Maximum allowable relative shift equals 50mV.
2. All specifications valid for radiation dose $\leq 1E6$ rads(Si).

PACKAGING

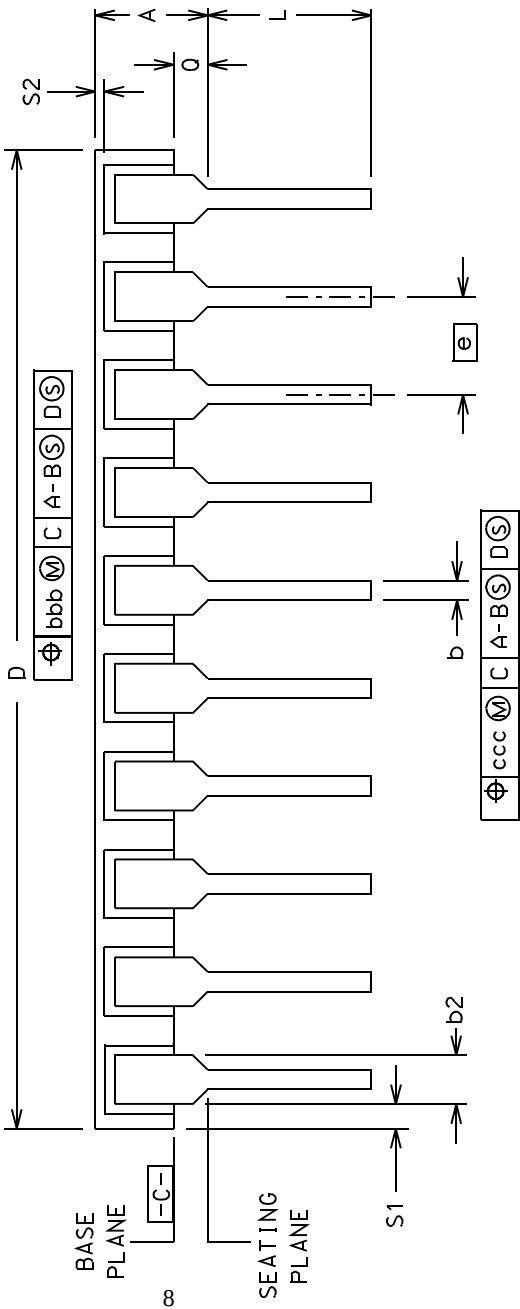
Side-Brazed Packages



SIDE VIEW

TOP VIEW

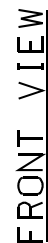
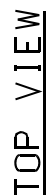
PIN 1 INDEX AREA



FRONT VIEW

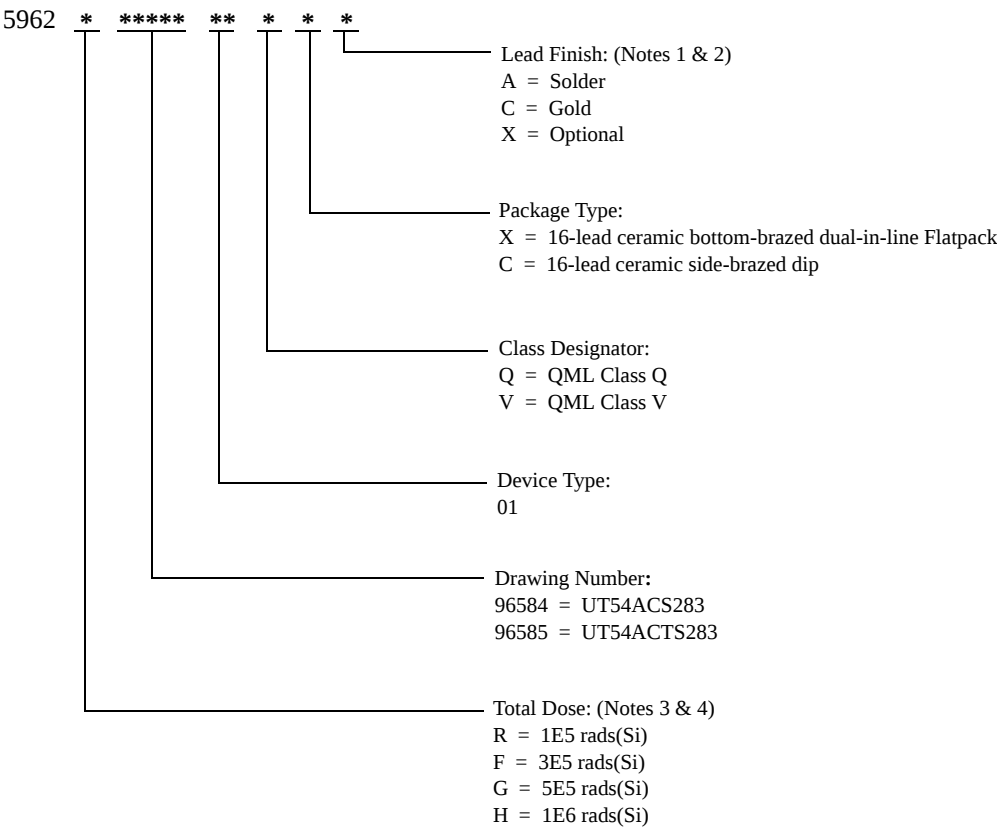
PKG CONFIG	LEAD COUNT	MIL-STD- 1835 DWG CONF C	DIMENSION SYMBOLS														
			A	b	b2	c	D	E	e	eA	L	Q	S1	S2	aaa	bbb	ccc
-01	14	D-1	0.200 -----	0.026 0.014	0.065 0.045	0.018 0.008	0.785 -----	0.310 0.220	0.100 BSC	0.300 BSC	0.200 0.125	0.060 0.015	0.005 -----	0.005 -----	0.015 -----	0.030 -----	0.010 -----
-02	16	D-2	0.200 -----	0.026 0.014	0.065 0.045	0.018 0.008	0.840 -----	0.310 0.220	0.100 BSC	0.300 BSC	0.200 0.125	0.060 0.015	0.005 -----	0.005 -----	0.015 -----	0.030 -----	0.010 -----
-03	20	D-8	0.200 -----	0.026 0.014	0.065 0.045	0.018 0.008	1.060 -----	0.310 0.220	0.100 BSC	0.300 BSC	0.200 0.125	0.070 0.015	0.005 -----	0.005 -----	0.015 -----	0.030 -----	0.010 -----

PIN #1 ID MARK



PKG CONFIG	LEAD COUNT	MIL-STD 1835 DWG CONF B	DIMENSION SYMBOLS												
			A	b	c	D	E	E1	E2	E3	e	k	L	Q	S1
-03	14	F-2A	0.115 0.045	0.022 0.015	0.009 0.004	0.390 -----	0.260 0.235	0.290 -----	----- 0.130	----- BSC	0.015 0.008	0.370 0.270	0.045 0.026	----- 0.005	
-04	16	F-5A	0.115 0.045	0.022 0.015	0.009 0.004	0.440 -----	0.285 0.245	0.315 -----	----- 0.130	0.050 BSC	0.015 0.008	0.370 0.250	0.045 0.026	----- 0.005	
-05	20	F-9A	0.115 0.045	0.022 0.015	0.009 0.004	0.540 -----	0.300 0.245	0.330 -----	----- 0.130	0.050 BSC	0.015 0.008	0.370 0.250	0.045 0.026	----- 0.000	

UT54ACS283/UT54ACTS283: SMD



- Notes:**
1. Lead finish (A,C, or X) must be specified.
 2. If an “X” is specified when ordering, part marking will match the lead finish and will be either “A” (solder) or “C” (gold).
 3. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening. For prototype inquiries, contact factory.
 4. Device type 02 is only offered with a TID tolerance guarantee of 3E5 rads(Si) or 1E6 rads(Si) and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A and section 3.11.2. Device type 03 is only offered with a TID tolerance guarantee of 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.

Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced Hi-Rel

COLORADO

Toll Free: 800-645-8862
Fax: 719-594-8468

INTERNATIONAL

Tel: 805-778-9229
Fax: 805-778-1980

NORTHEAST

Tel: 603-888-3975
Fax: 603-888-4585

SE AND MID-ATLANTIC

Tel: 321-951-4164
Fax: 321-951-4254

WEST COAST

Tel: 949-362-2260
Fax: 949-362-2266

CENTRAL

Tel: 719-594-8017
Fax: 719-594-8468

www.aeroflex.com info-ams@aeroflex.com

Aeroflex UTM Microelectronic Systems Inc. (Aeroflex) reserves the right to make changes to any products and services herein at any time without notice. Consult Aeroflex or an authorized sales representative to verify that the information in this data sheet is current before using this product. Aeroflex does not assume any responsibility or liability arising out of the application or use of any product or service described herein, except as expressly agreed to in writing by Aeroflex; nor does the purchase, lease, or use of a product or service from Aeroflex convey a license under any patent rights, copyrights, trademark rights, or any other of the intellectual rights of Aeroflex or of third parties.



Our passion for performance is defined by three attributes represented by these three icons: solution-minded, performance-driven and customer-focused