



UT45N04H

Preliminary

Power MOSFET

45A, 40V N-CHANNEL POWER MOSFET

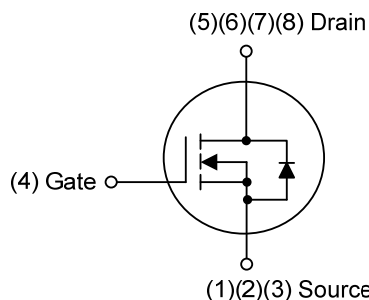
DESCRIPTION

The UTC **UT45N04H** is a N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

FEATURES

- * $R_{DS(ON)} \leq 8.0 \text{ m}\Omega$ @ $V_{GS}=10V$, $I_D=20A$
- * Improved dv/dt capability
- * High Switching Speed
- * Fast switching

SYMBOL

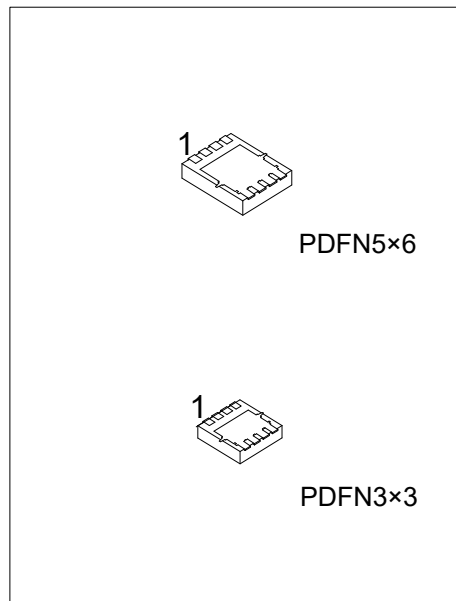


ORDERING INFORMATION

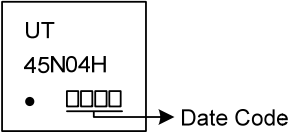
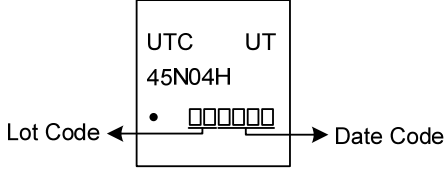
Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT45N04HL-P3030-R	UT45N04HG-P3030-R	PDFN3×3	S	S	S	G	D	D	D	D	Tape Reel
UT45N04HL-P5060-R	UT45N04HG-P5060-R	PDFN5×6	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UT45N04HG-P3030-R	(1) Packing Type	(1) R: Tape Reel
	(2) Package Type	(2) P3030: PDFN3×3, P5060: PDFN5×6
	(3) Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free



■ MARKING

PDFN3×3	PDFN5×6
	

■ ABSOLUTE MAXIMUM RATINGS ($T_c=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	40	V
Gate-Source Voltage		V_{GSS}	± 20	V
Drain Current	Continuous ($V_{\text{GS}}=10\text{V}$)	I_{D}	45	A
	Pulsed (Note 2)	I_{DM}	90	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	38	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	1.9	V/ns
Power Dissipation	PDFN3×3	P_{D}	32	W
	PDFN5×6		41	W
Junction Temperature		T_{J}	+150	$^{\circ}\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L=0.1\text{mH}$, $I_{\text{AS}}=27.6\text{A}$, $V_{\text{DD}}=25\text{V}$, $R_{\text{G}}=25\Omega$, Starting $T_{\text{J}}=25^{\circ}\text{C}$

4. $I_{\text{SD}} \leq 30\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{\text{DD}} \leq BV_{\text{DSS}}$, Starting $T_{\text{J}} = 25^{\circ}\text{C}$

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction-to-Ambient	PDFN3×3	θ_{JA}	75	$^{\circ}\text{C}/\text{W}$
	PDFN5×6		65	$^{\circ}\text{C}/\text{W}$
Junction-to-Case	PDFN3×3	θ_{JC}	3.9	$^{\circ}\text{C}/\text{W}$
	PDFN5×6		3.05	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

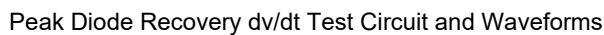
■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	V _{GS} =0V, I _D =250μA	40			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =40V, V _{GS} =0V			1	μA
Gate- Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	2.0		4.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =20A			8.0	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		1860		pF
Output Capacitance		C _{OSS}			235		pF
Reverse Transfer Capacitance		C _{RSS}			200		pF
SWITCHING PARAMETERS							
Total Gate Charge		Q _G	V _{DS} =32V, V _{GS} =10V, I _D =45A (Note 2)		70		nC
Gate to Source Charge		Q _{GS}			14		nC
Gate to Drain Charge		Q _{GD}			24		nC
Turn-ON Delay Time		t _{D(ON)}	V _{DD} =20V, V _{GS} =10V, I _D =45A, R _G =3.3Ω, (Note 2)		10		ns
Rise Time		t _R			18		ns
Turn-OFF Delay Time		t _{D(OFF)}			40		ns
Fall-Time		t _F			20		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Continuous Drain-Source Diode Forward Current		I _S				45	A
Maximum Pulsed Drain-Source Diode Forward Current		I _{SM}				90	A
Drain-Source Diode Forward Voltage		V _{SD}	I _S =45A, V _{GS} =0V			1.4	V
Body Diode Reverse Recovery Time		t _{rr}	I _F =30A, V _{GS} =0V, di/dt=100A/μs		27		ns
Body Diode Reverse Recovery Charge		Q _{rr}			11		nC

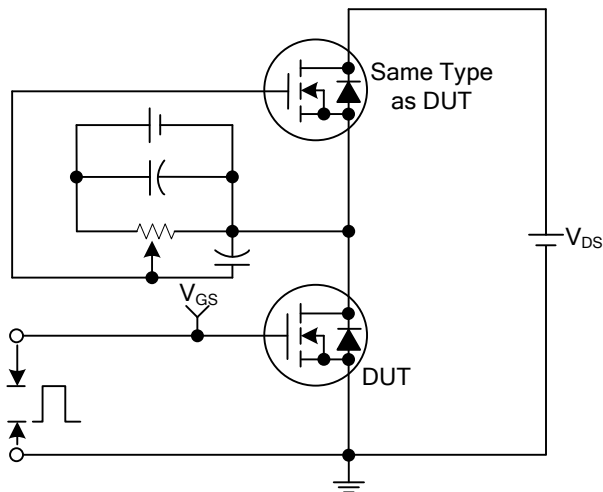
Notes: 1. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%.

2. Essentially independent of operating ambient temperature.

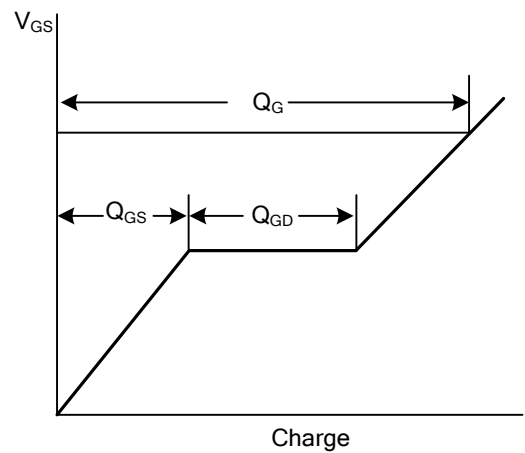
dv/dt controlled by R_G
 I_{SD} controlled by pulse period



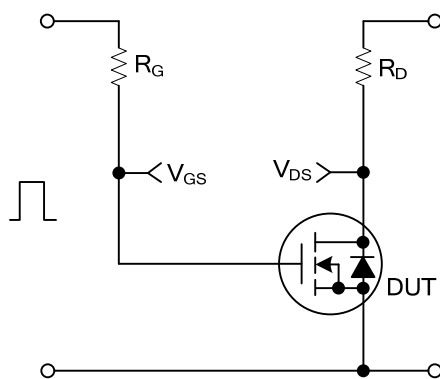
■ TEST CIRCUITS AND WAVEFORMS



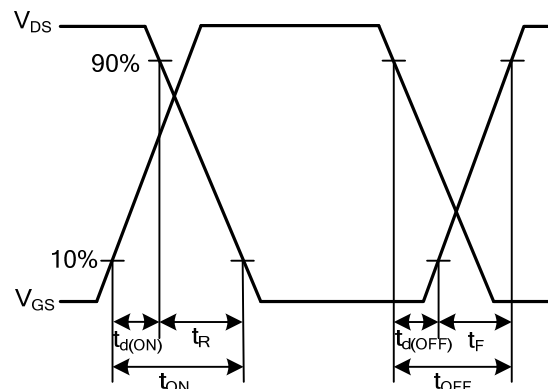
Gate Charge Test Circuit



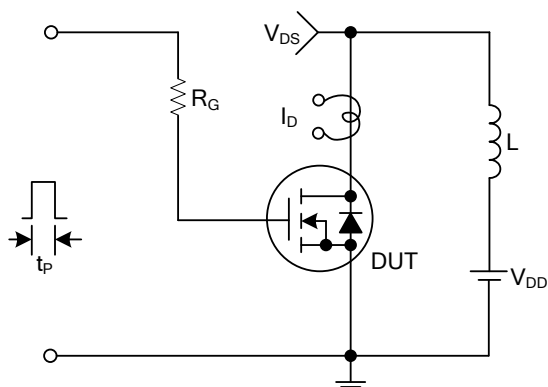
Gate Charge Waveforms



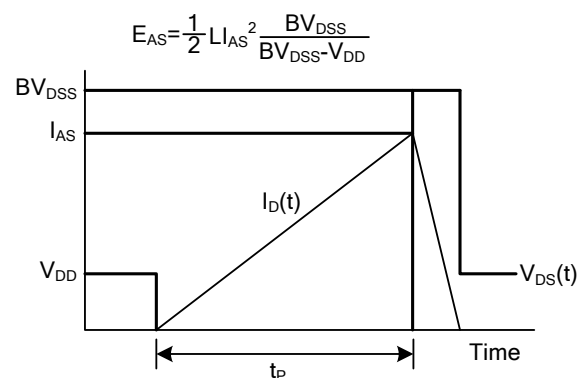
Resistive Switching Test Circuit



Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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