



UT35P02

Preliminary

POWER MOSFET

-35A, -20V P-CHANNEL POWER MOSFET

DESCRIPTION

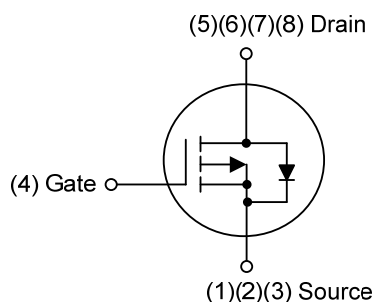
The UTC **UT35P02** is P-channel enhancement mode power MOSFET using UTC's advanced technology to provide customers with ideal for low voltage inverter applications.

The UTC **UT35P02** is suitable for high efficiency synchronous rectification in SMPS, UPS, hard switched and high frequency circuits.

FEATURES

- * $R_{DS(ON)} \leq 16 \text{ m}\Omega$ @ $V_{GS} = -4.5\text{V}$, $I_D = -10\text{A}$
 $R_{DS(ON)} \leq 25 \text{ m}\Omega$ @ $V_{GS} = -2.5\text{V}$, $I_D = -8.8\text{A}$
- * High Cell Density Trench Technology
- * High Power and Current Handling Capability

SYMBOL

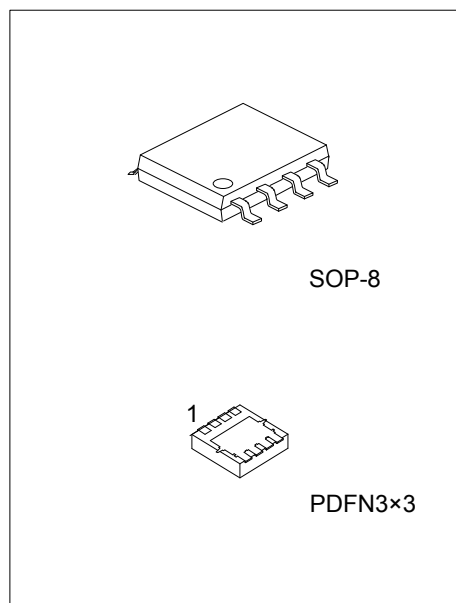


ORDERING INFORMATION

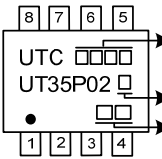
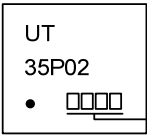
Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT35P02L-S08-R	UT35P02G-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel
UT35P02L-P3030-R	UT35P02G-P3030-R	PDFN3×3	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UT35P02G-S08-R 		(1) R: Tape Reel (2) S08: SOP-8, P3030: PDFN3×3 (3) G: Halogen Free and Lead Free, L: Lead Free
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MARKING

SOP-8	PDFN3×3
 <p> UTC □□□□ → Date Code UT35P02 □ → L: Lead Free □ → G: Halogen Free • □□ → Lot Code </p>	 <p> UT 35P02 • □□□□ → Date Code </p>

■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	-20	V
Gate-Source Voltage		V_{GSS}	± 12	V
Continuous Drain Current	Continuous	I_{D}	-35	A
Pulsed Drain Current	Pulsed (Note 2)	I_{DM}	-70	A
Single Pulsed Avalanche Energy		E_{AS}	97.7	mJ
Power Dissipation	SOP-8	P_{D}	1.8	W
	PDFN3×3		26	W
Junction Temperature		T_{J}	+150	$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L=0.1\text{mH}$, $I_{\text{AS}}=-44.2\text{A}$, $V_{\text{DD}}=-10\text{V}$, $R_{\text{G}}=25\Omega$, Starting $T_{\text{J}} = 25^{\circ}\text{C}$

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-8	θ_{JA}	90	$^{\circ}\text{C/W}$
	PDFN3×3		60	$^{\circ}\text{C/W}$
Junction to Case	SOP-8	θ_{JC}	69	$^{\circ}\text{C/W}$
	PDFN3×3		4.8	$^{\circ}\text{C/W}$

Note: Device mounted on FR-4 substrate P_{C} board, 2oz copper, with 1inch square copper plate.

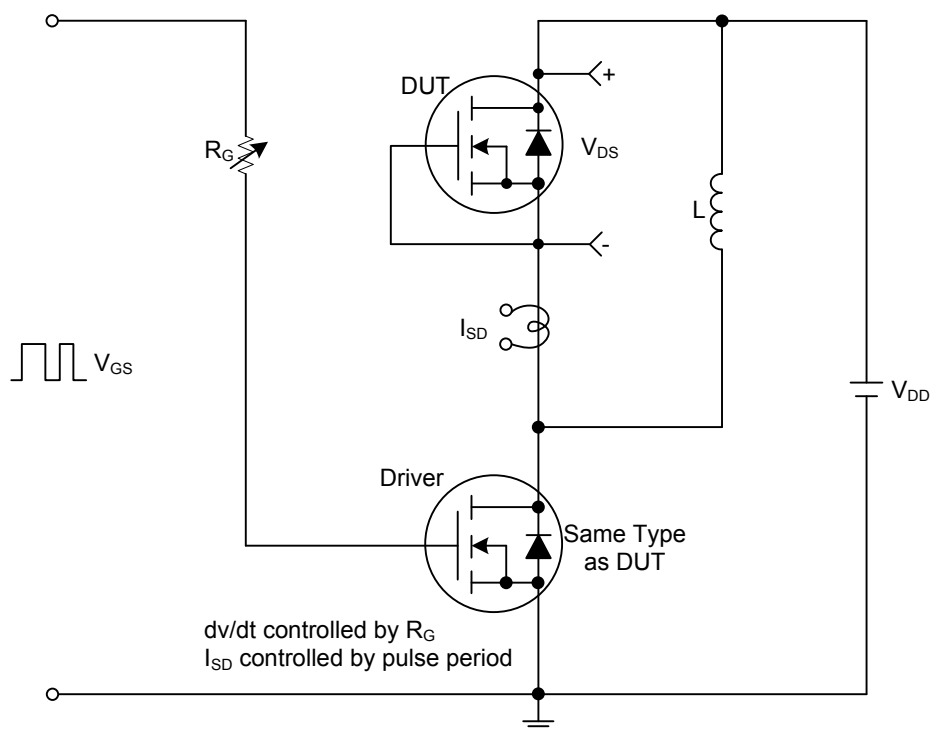
■ ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	$I_D=-250\mu A$, $V_{GS}=0V$	-20			V
Drain-Source Leakage Current		I_{DSS}	$V_{DS}=-20V$, $V_{GS}=0V$, $T_J=25^{\circ}C$			-1	μA
Gate-Source Leakage Current	Forward	I_{GSS}	$V_{GS}=+12V$, $V_{DS}=0V$			+100	nA
	Reverse		$V_{GS}=-12V$, $V_{DS}=0V$			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=-250\mu A$	-0.5		-2.5	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	$V_{GS}=-4.5V$, $I_D=-10A$			16	m Ω
			$V_{GS}=-2.5V$, $I_D=-8.8A$			25	m Ω
DYNAMIC PARAMETERS							
Input Capacitance		C_{ISS}	$V_{GS}=0V$, $V_{DS}=-10V$, $f=1.0MHz$		3849		pF
Output Capacitance		C_{OSS}			580		pF
Reverse Transfer Capacitance		C_{RSS}			545		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		Q_G	$V_{DS}=-16V$, $V_{GS}=-10V$, $I_D=-35A$, $I_D=1mA$ (Note 1, 2)		75		nC
Gate to Source Charge		Q_{GS}			9		nC
Gate to Drain Charge		Q_{GD}			10		nC
Turn-on Delay Time (Note 1)		$t_{D(ON)}$	$V_{DS}=-10V$, $V_{GS}=-10V$, $I_D=-35A$, $R_G=6\Omega$ (Note 1, 2)		12		ns
Rise Time		t_R			18		ns
Turn-off Delay Time		$t_{D(OFF)}$			82		ns
Fall-Time		t_F			45		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I_S				-35	A
Maximum Body-Diode Pulsed Current		I_{SM}				-70	A
Drain-Source Diode Forward Voltage (Note 1)		V_{SD}	$I_S=-2.1A$, $V_{GS}=0V$			-1.4	V
Body Diode Reverse Recovery Time		t_{rr}	$I_S=-30A$, $V_{GS}=0V$,		7.4		ns
Reverse Recovery Charge		Q_{rr}	$di_F/dt=100A/\mu s$ (Note 1)		3.9		ns

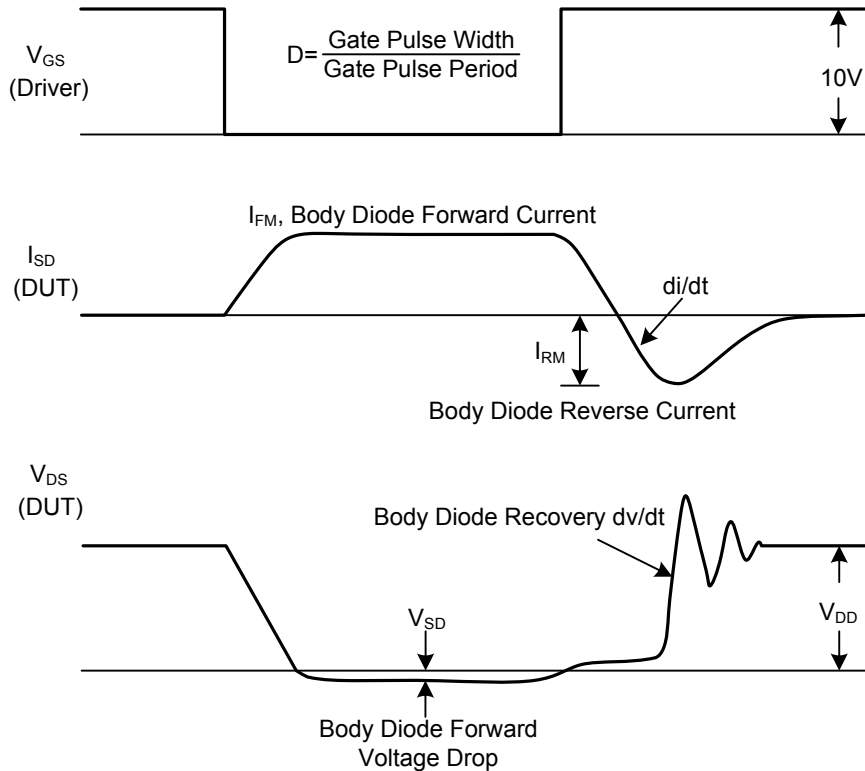
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS



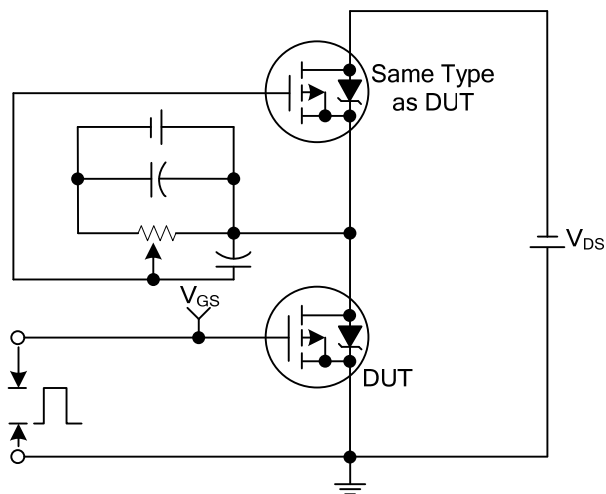
Peak Diode Recovery dv/dt Test Circuit



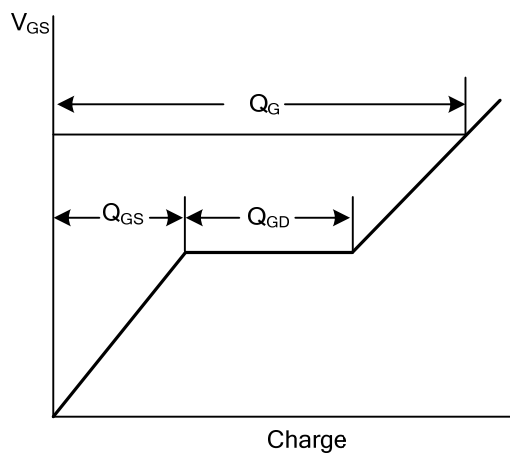
Peak Diode Recovery dv/dt Test Circuit and Waveforms

Peak Diode Recovery dv/dt Waveforms

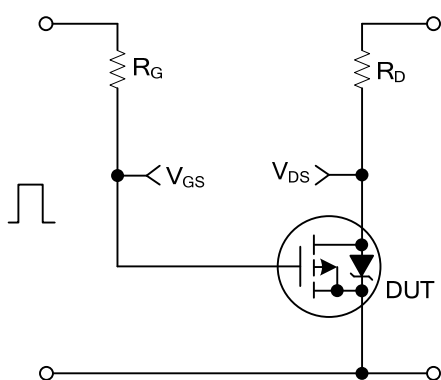
■ TEST CIRCUITS AND WAVEFORMS



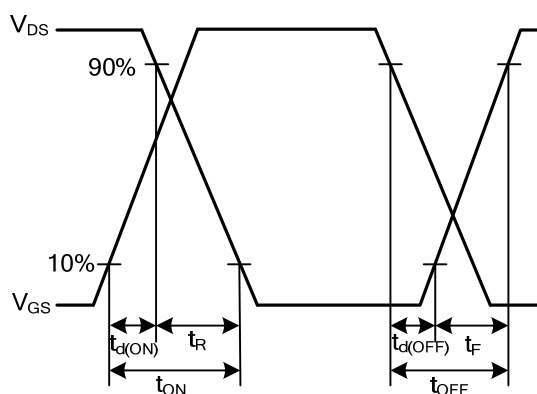
Gate Charge Test Circuit



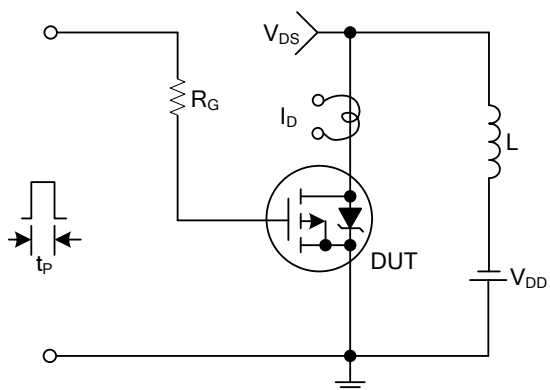
Gate Charge Waveforms



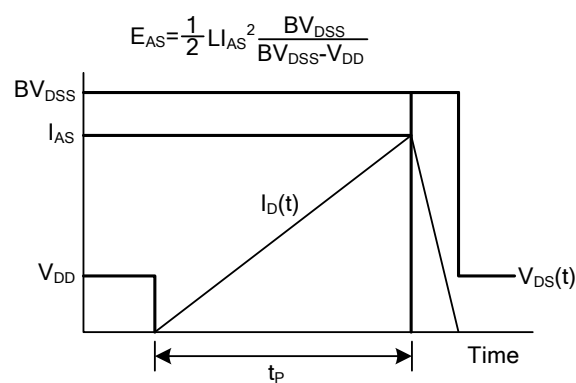
Resistive Switching Test Circuit



Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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