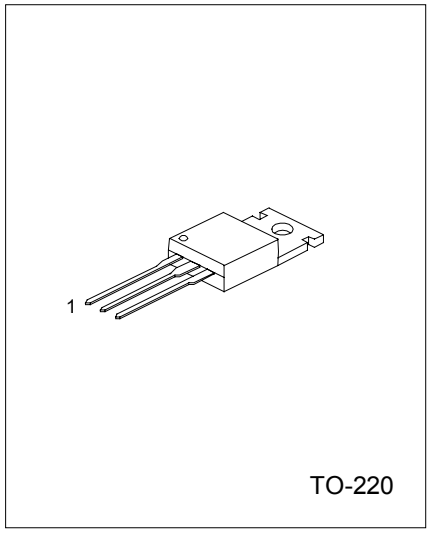
## TRIACS

### DESCRIPTION

Passivated , sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.




1:MT1 2:MT2 3:GATE

### SYMBOL


### ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Repetitive Peak Off-State Voltage<br>UT137E-5<br>UT137E-6<br>UT137E-8 | $V_{DRM}$ | <br>500*<br>600*<br>800 | V |
| RMS On-state Current<br>Full sine wave; Tmb≤102°C | $I_{T(RMS)}$ | 8 | A |
| Non-Repetitive Peak. On-State Current<br>Full sine wave; Tj=25°C prior to surge<br>t=20ms<br>t=16.7ms | $I_{TSM}$ | <br><br>65<br>71 | A |
| $I^2t$ For Fusing (t=10ms) | $I^2t$ | 21 | $A^2s$ |
| Repetitive Rate of Rise of On-state Current after Triggering<br>$I_{TM}$=12A;$I_G$=0.2A,$dI_G/dt$=0.2A/μs<br>T2+ G+<br>T2+ G-<br>T2- G-<br>T2- G+ | $dI_T/dt$ | <br><br>50<br>50<br>50<br>10 | A/μs |
| Peak Gate Voltage | $V_{GM}$ | 5 | V |
| Peak Gate Current | $I_{GM}$ | 2 | A |
| Peak Gate Power | $P_{GM}$ | 5 | W |
| Average Gate Power (Over any 20ms period) | $P_{G(AV)}$ | 0.5 | W |
| Operating Junction Temperature | Tj | 125 | °C |
| Storage Temperature | Tstg | -40~150 | °C |

*Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6A/μs.

## THERMAL RESISTANCES

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Thermal Resistance Junction to Mounting Base<br>Full cycle<br>Half cycle | Rth j-mb | | | 2.0<br>2.4 | K/W |
| Thermal Resistance Junction to Ambient<br>In free air | Rth j-a | | 60 | | K/W |

## STATIC CHARACTERISTICS (Tj=25°C,unless otherwise specified)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Gate Trigger Current | $I_{GT}$ | $V_D$=12V, $I_T$=0.1A | | | | |
| | | T2+ G+ | | 2.5 | 10 | mA |
| | | T2+ G- | | 4.0 | 10 | |
| | | T2- G- | | 5.0 | 10 | |
| | | T2- G+ | | 11 | 25 | |
| Latching Current | $I_L$ | $V_D$=12V, $I_{GT}$=0.1A | | | | |
| | | T2+ G+ | | 3.0 | 25 | mA |
| | | T2+ G- | | 14 | 35 | |
| | | T2- G- | | 3.0 | 25 | |
| | | T2- G+ | | 4.0 | 35 | |
| Holding Current | $I_H$ | $V_D$=12V, $I_{GT}$=0.1A | | 2.5 | 20 | mA |
| On-State Voltage | $V_T$ | $I_T$=10A | | 1.3 | 1.65 | V |
| Gate Trigger Voltage | $V_{GT}$ | $V_D$=12V, $I_T$=0.1A | | 0.7 | 1.5 | V |
| | | $V_D$=400V, $I_T$=0.1A, Tj=125°C | 0.25 | 0.4 | | V |
| Off-state Leakage Current | $I_D$ | $V_D$=$V_{DRM(max)}$ , Tj=125°C | | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS(Tj=25°C,unless otherwise specified)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Critical Rate of Rise of off-state Voltage | $dV_D/dt$ | $V_{DM}$=67% $V_{DRM(max)}$, Tj=125°C Exponential waveform,Gate open circuit | | 50 | | V/μs |
| Gate Controlled Turn-on Time | tgt | $I_{TM}$=12A,$V_D$=$V_{DRM(max)}$,$I_G$=0.1A $dI_G/dt$=5A/μs | | 2 | | μs |

## TYPICAL CHARACTERISTICS

Figure 1.Maximum on -state Dissipation.Ptot vs RMS On-state Current,$I_{T(RMS)}$,Where $\alpha$ =conduction Angle.

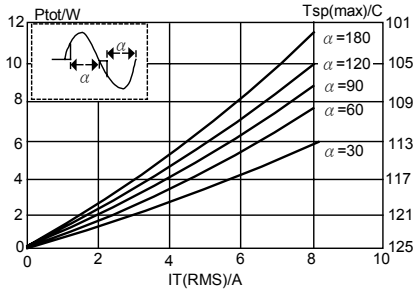



Figure 2. Maximum Permissible Non-repetitive Peak On-state Current $I_{TSM}$,vs Pulse Width $t_p$,for Sinusoidal Currents,$t_p \leqq 20ms$

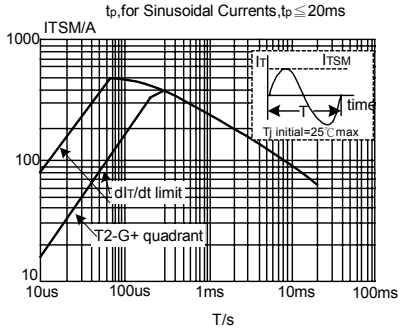



Figure 3 .Maximum Permissible Non-Repetitive peak on-state Current $I_{TSM}$,vs Number of Cycles, for Sinusoidal Currents,f=50Hz

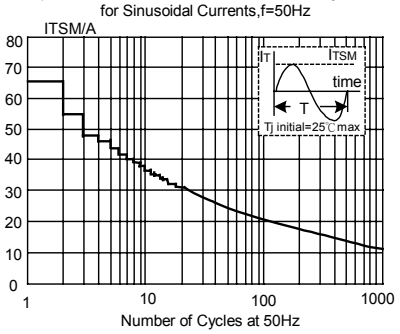



Figure 4.Maximum Permissible RMS Current $I_{T(RMS)}$ vs mounting baseTemperature $T_{mb}$

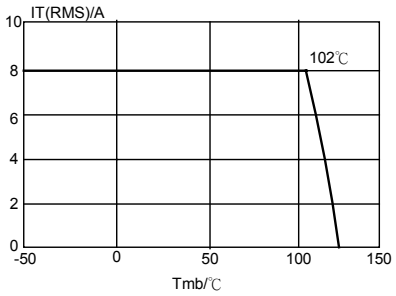



Figure 5.Maximum Permissible Repetitive RMS on-state Current $I_{T(RMS)}$,vs Surge Duration,for Sinusoidal Currents,f=50Hz;Tmb≦102℃

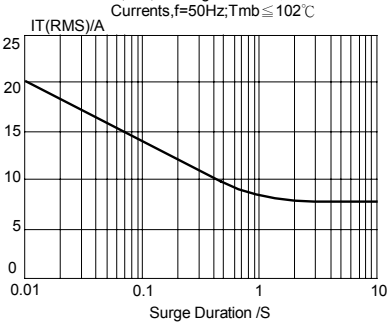



Figure 6.Normalised Gate Trigger Voltage $V_{GT}(Tj)$/ $V_{GT}(25℃)$,vs Junction Temperature Tj

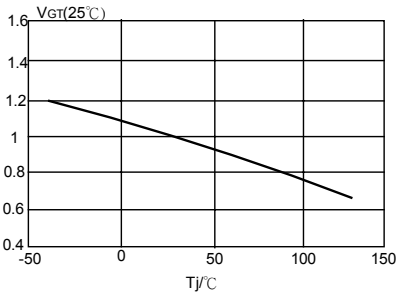


Figure 7.Normalised Gate Trigger Current
$I_{GT}(Tj)/I_{GT}(25℃)$,vs Junction Temperature Tj

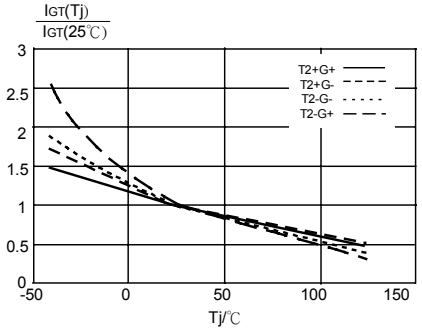



Figure 8.Normalised Latching Current
$I_L(Tj)/I_L(25℃)$,vs Junction Temperature Tj

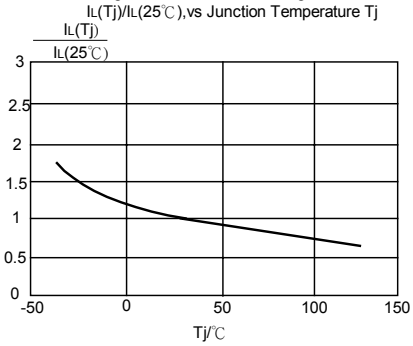



Figure 9.Normalised Holding Current
$I_H(Tj)/I_H(25℃)$,vs Junction Temperature Tj

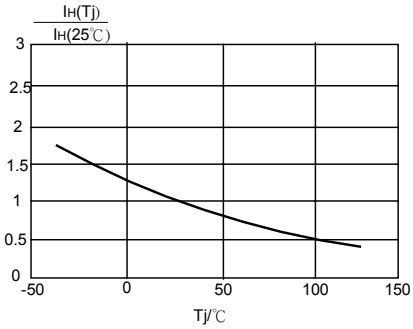



Figure 10.Typical and Maximum
On-state Characteristic

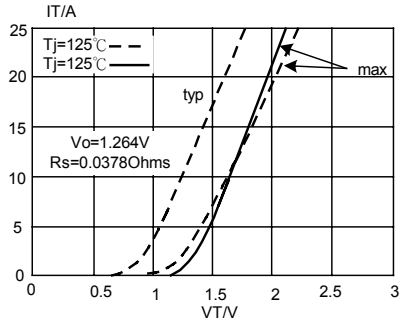



Figure 11.Transient Thermal Impedance
Zth j-mb,vs Pulse Width tp

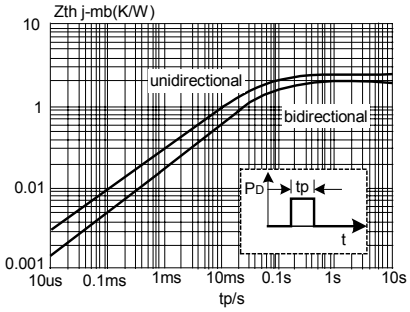



Figure 12.Typical ,critical rate of rise of off-state
voltage,$dV_D/dt$ versus junction temperature Tj