

TOSHIBA THYRISTOR SILICON PLANAR TYPE

SF8G48,SF8J48,USF8G48,USF8J48

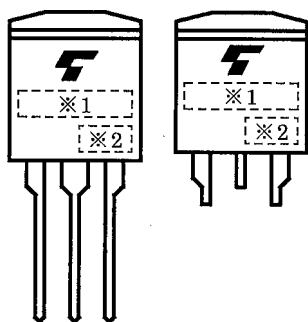
MEDIUM POWER CONTROL APPLICATIONS

- Repetitive Peak Off-State Voltage : $V_{DRM}=400,600V$
Repetitive Peak Reverse Voltage : $V_{RRM}=400,600V$
- Average On-State Current : $I_T (AV) = 8A$
- Gate Trigger Current : $I_{GT}=10mA$ Max.

Unit in mm

SF8G48 · SF8J48	USF8G48 · USF8J48
1. CATHODE 2. ANODE 3. GATE	1. CATHODE 2. ANODE (BACK SIDE) 3. GATE
JEDEC —	JEDEC —
JEITA —	JEITA —
TOSHIBA 13-10J1B	TOSHIBA 13-10J2B

Weight : 1.7g

MARKING

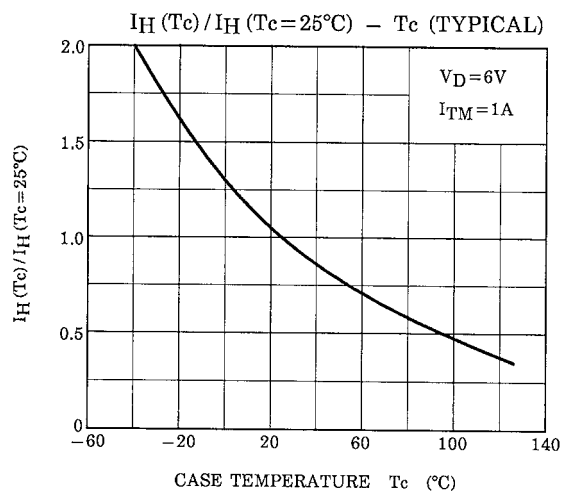
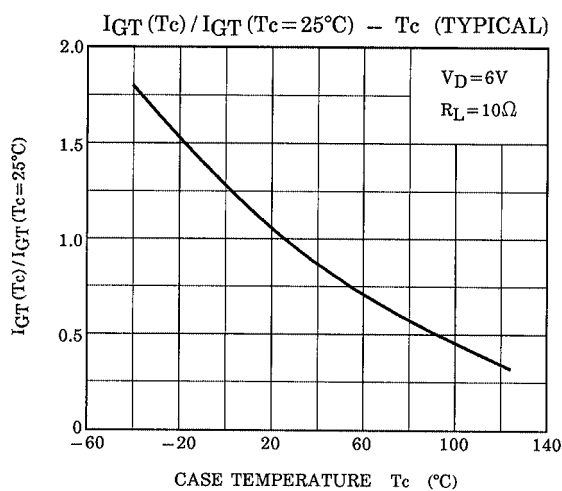
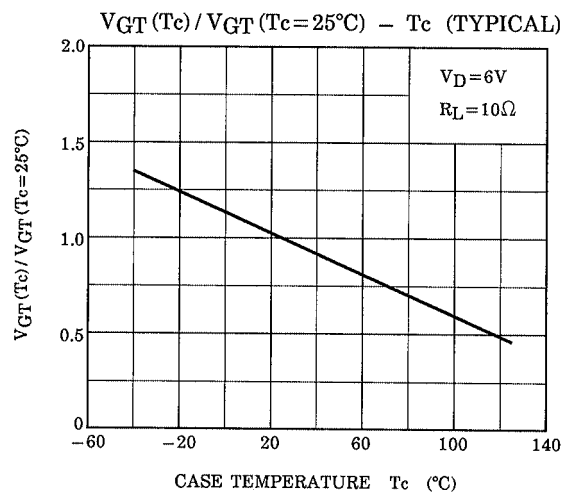
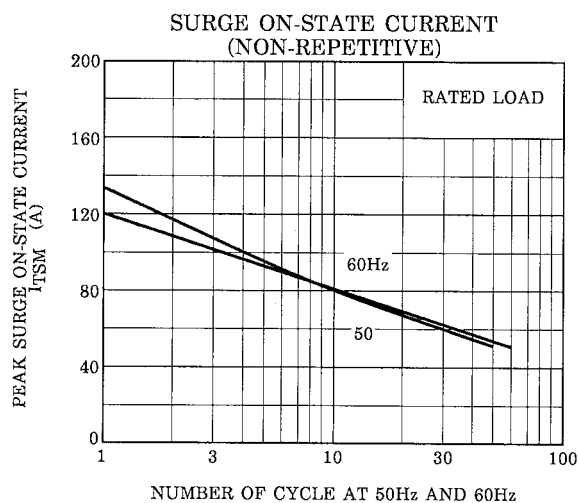
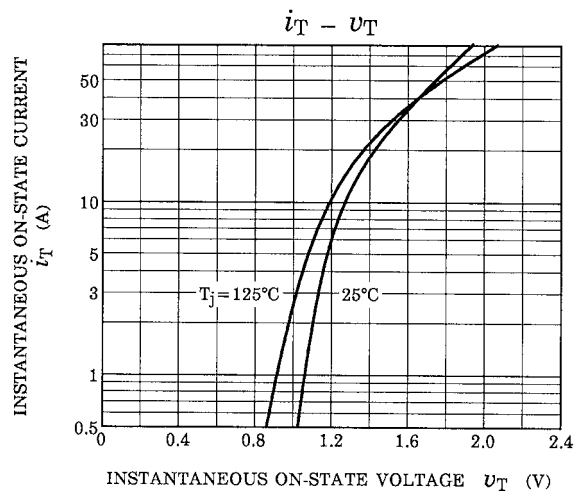
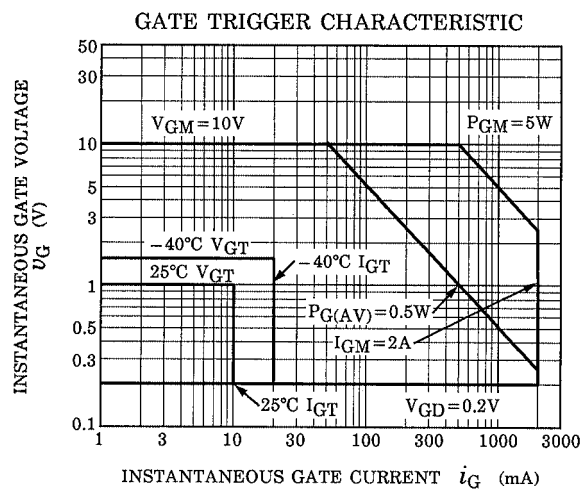
*1	MARK	F8G48	TYPE NAME	SF8G48, USF8G48
		F8J48		SF8J48, USF8J48
*2	Lot Number ← Month (Starting from Alphabet A) ↑ Year (Last Decimal Digit of the Year of Manufacture)			

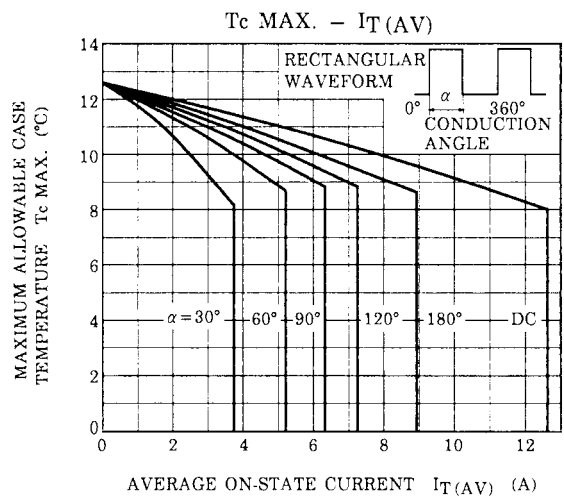
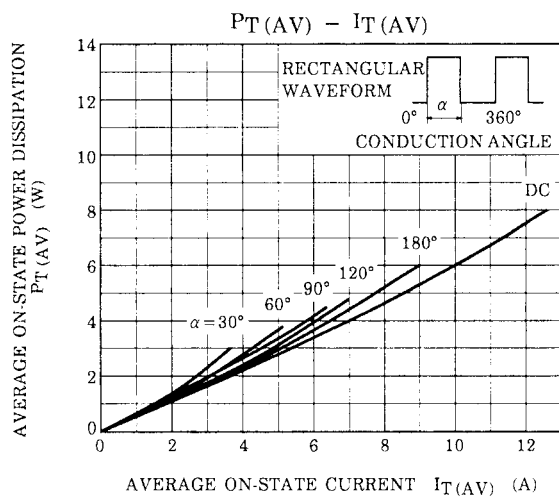
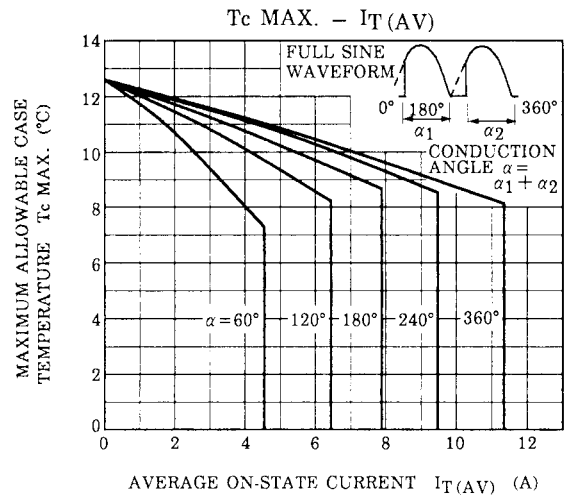
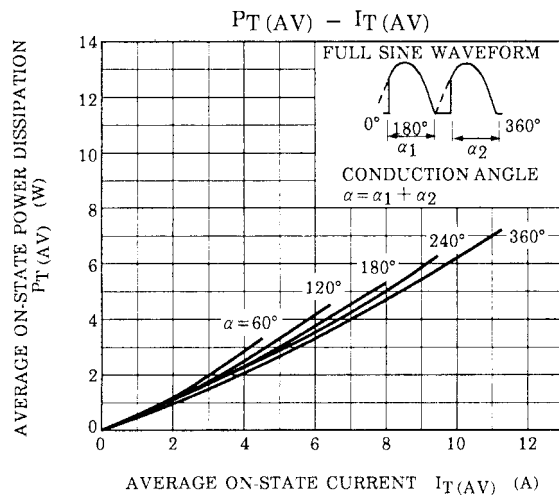
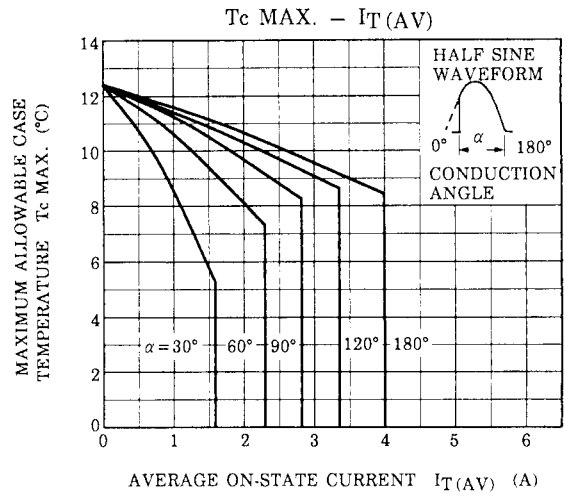
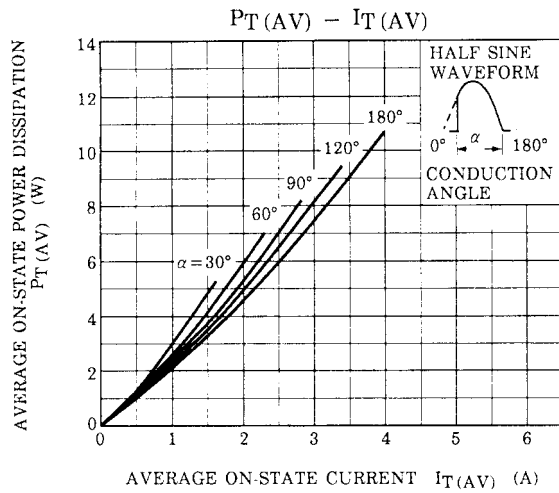
MAXIMUM RATINGS (Ta=25°C)

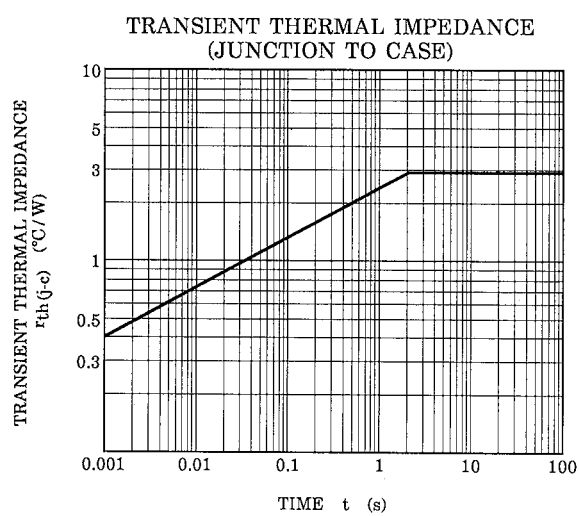
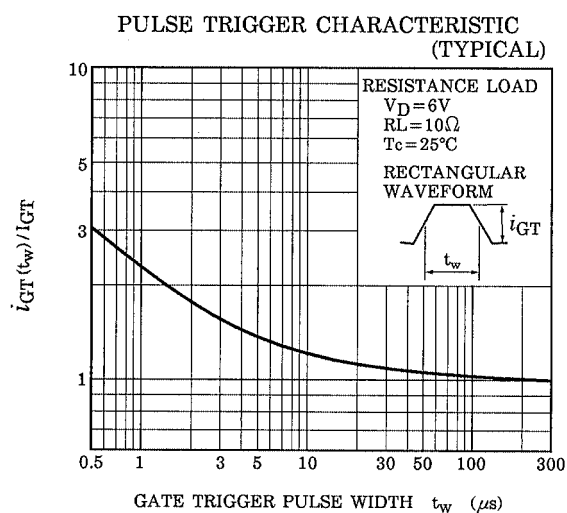
CHARACTERISTIC		SYMBOL	RATING	UNIT
Repetitive Peak Off-State Voltage and Repetitive Peak Reverse Voltage	SF8G48	V_{DRM} V_{RRM}	400	V
	USF8G48			
	SF8J48		600	
	USF8J48			
Non-Repetitive Peak Reverse Voltage (Non-Repetitive<5ms $T_j=0\sim 125^{\circ}\text{C}$)	SF8G48	V_{RSM}	500	V
	USF8G48			
	SF8J48		720	
	USF8J48			
Average On-State Current		$I_T (AV)$	8	A
R.M.S On-State Current		$I_T (RMS)$	12.6	A
Peak One Cycle Surge On-State Current (Non-Repetitive)		I_{TSM}	120 (50Hz)	A
			132 (60Hz)	
I^2t Limit Value		I^2t	72	A^2s
Critical Rate of Rise of On-State Current (Note 1)		di/dt	100	A / μs
Peak Gate Power Dissipation		P_{GM}	5	W
Average Gate Power Dissipation		$P_G (AV)$	0.5	W
Peak Forward Gate Voltage		V_{FGM}	10	V
Peak Reverse Gate Voltage		V_{RGM}	-5	V
Peak Forward Gate Current		I_{GM}	2	A
Junction Temperature		T_j	-40~125	$^{\circ}\text{C}$
Storage Temperature Range		T_{stg}	-40~125	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS (Ta=25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Repetitive Peak Off-State Current and Repetitive Peak Reverse	I_{DRM} I_{RRM}	$V_{DRM}=V_{RRM}=\text{Rated}$	—	—	10	μA
Peak On-State Voltage	V_{TM}	$I_{TM}=25\text{A}$	—	—	1.5	V
Gate Trigger Voltage	V_{GT}	$V_D=6\text{V}$, $R_L=10\Omega$	—	—	1.0	V
Gate Trigger Current	I_{GT}		—	—	10	mA
Gate Non-Trigger Voltage	V_{GD}	$V_D=\text{Rated}\times 2/3$, $T_c=125^{\circ}\text{C}$	0.2	—	—	V
Critical Rate of Rise of Off-State Voltage	dv/dt	$V_{DRM}=\text{Rated}$, $T_c=125^{\circ}\text{C}$ Exponential Rise	—	50	—	V / μs
Holding Current	I_H	$V_D=6\text{V}$, $I_{TM}=1\text{A}$	—	—	40	mA
Latching Current	I_L	$V_D=6\text{V}$, $f=50\text{Hz}$ $t_{gw}=50\mu\text{s}$, $i_G=30\text{mA}$	—	—	50	mA
Thermal Resistance	$R_{th (j-c)}$	Junction to Case, DC	—	—	2.8	$^{\circ}\text{C} / \text{W}$







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