

TOSHIBA THYRISTOR SILICON PLANAR TYPE

USF05G49**LOW POWER SWITCHING AND CONTROL APPLICATIONS**

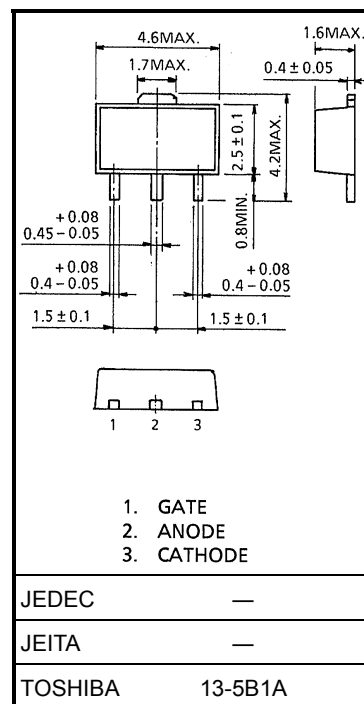
- Repetitive Peak Off-State Voltage : $V_{DRM} = 400\text{ V}$
Repetitive Peak Reverse Voltage : $V_{RRM} = 400\text{ V}$
- Average On-State Current : $I_T(\text{AV}) = 500\text{ mA}$

MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Repetitive Peak Off-State Voltage and Repetitive Peak Reverse Voltage	V_{DRM} V_{RRM}	400	V
Non-Repetitive Peak Reverse Voltage (Non-Repetitive < 5ms, $T_j = 0 \sim 125^\circ\text{C}$)	V_{RSM}	500	V
Average On-State Current (Half Sine Waveform)	$I_T(\text{AV})$	500	mA
R.M.S On-State Current	$I_T(\text{RMS})$	800	mA
Peak One Cycle Surge On-State Current (Non-Repetitive)	I_{TSM}	9 (50Hz) 10 (60Hz)	A
I^2_t Limit Value	I^2_t	0.4	A^2s
Critical Rate of Rise of On-State Current (Note 1)	di/dt	10	$\text{A}/\mu\text{s}$
Peak Gate Power Dissipation	P_{GM}	0.1	W
Average Gate Power Dissipation	$P_{G(\text{AV})}$	0.01	W
Peak Forward Gate Voltage	V_{FGM}	3.5	V
Peak Reverse Gate Voltage	V_{RGM}	-5	V
Peak Forward Gate Current	I_{GM}	125	mA
Junction Temperature	T_j	$-40 \sim 125$	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	$-40 \sim 125$	$^\circ\text{C}$

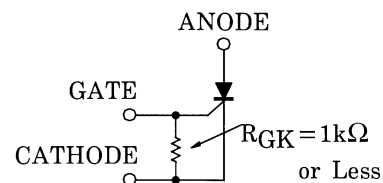
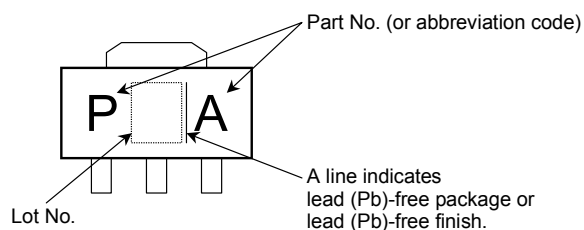
Note 1: di/dt Test condition: $i_G = 5\text{ mA}$, $t_{GW} = 10\mu\text{s}$, $t_{gr} \leq 250\text{ ns}$

Unit: mm



Weight: 0.2 g (typ.)

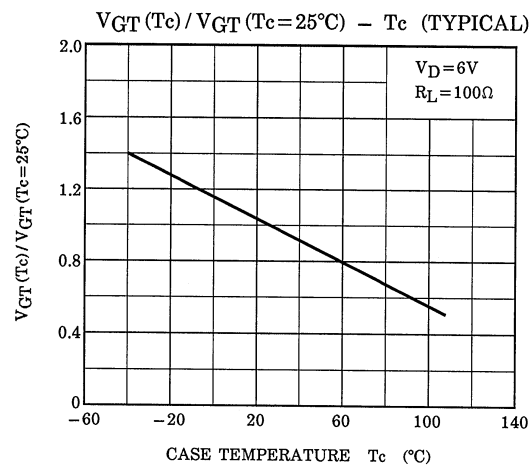
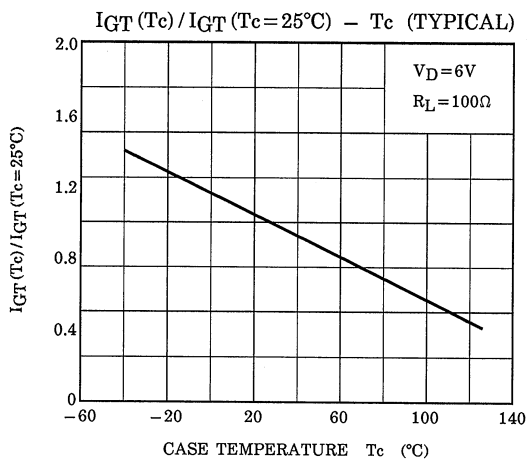
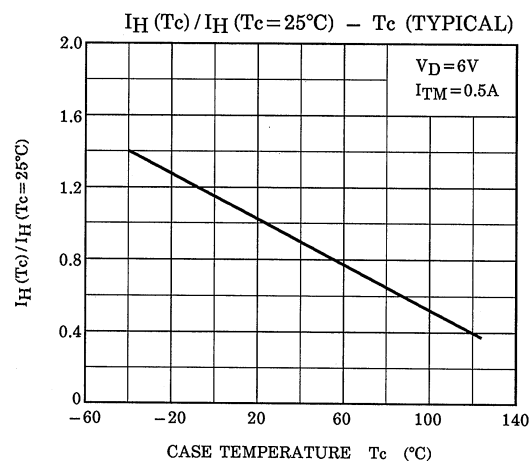
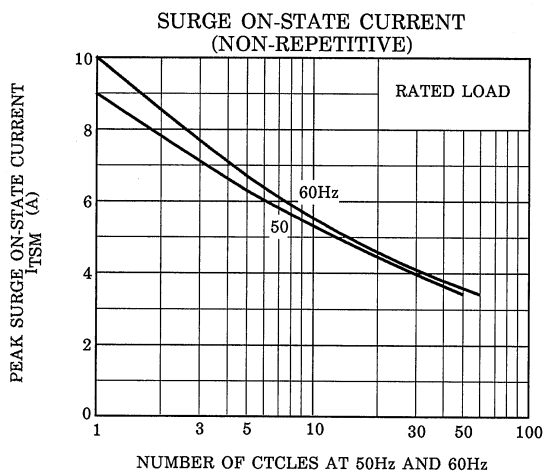
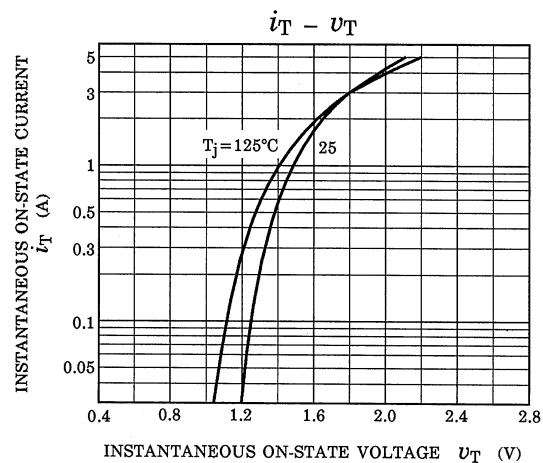
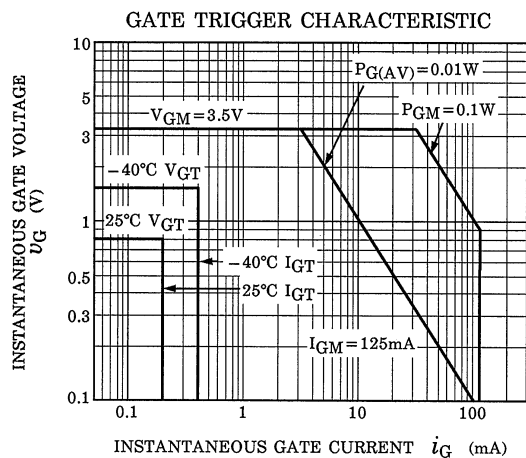
Note: Should be used with gate resistance as shown below.

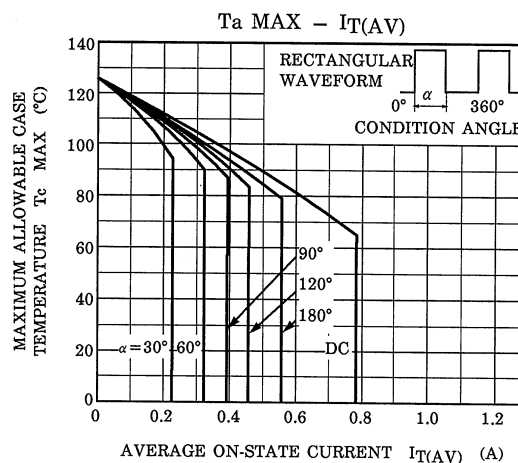
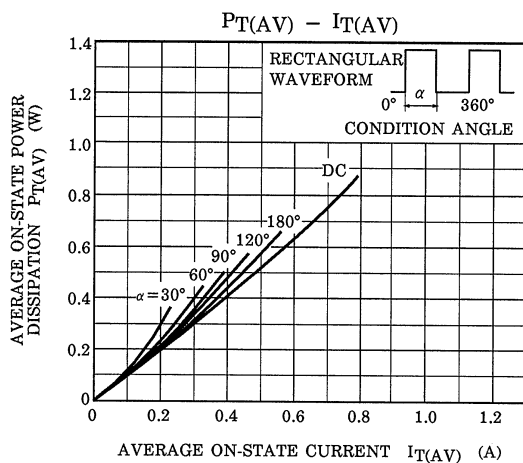
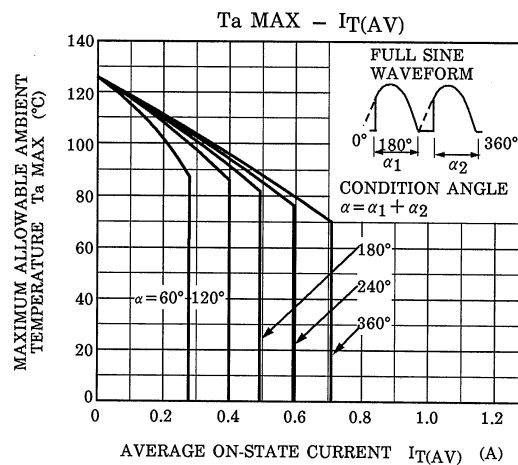
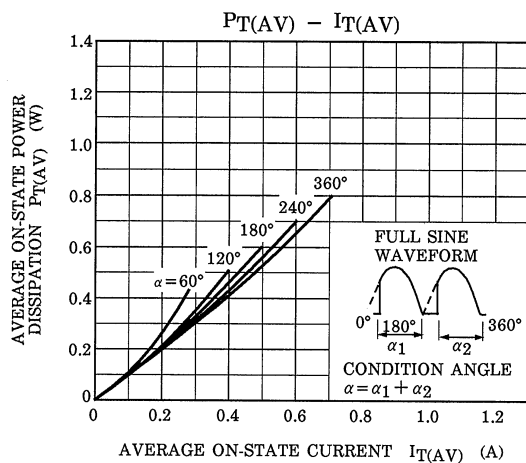
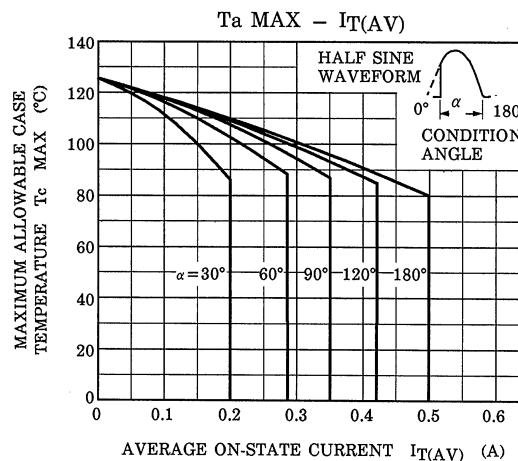
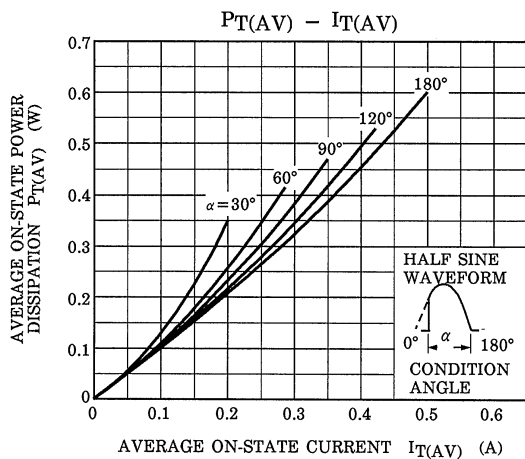
**MARKING**

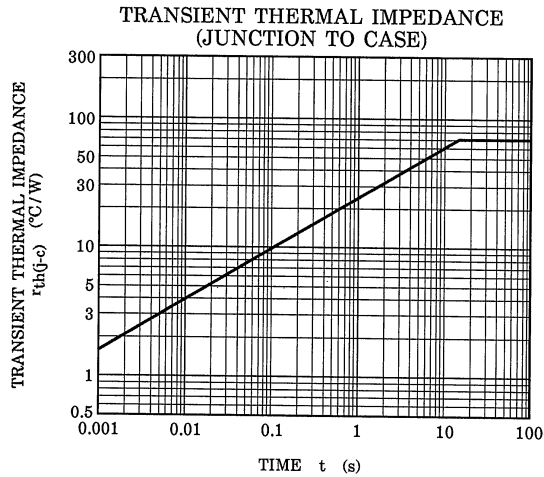
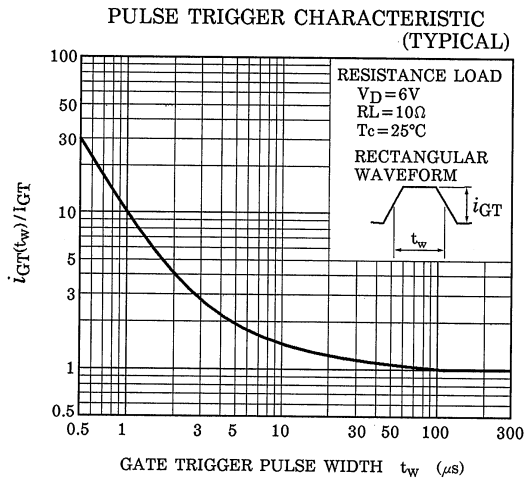
ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Repetitive Peak Off-State Current and Repetitive Peak Reverse Current	I_{DRM} I_{RRM}	$V_{DRM} = V_{RRM} = \text{Rated}$	—	—	10	μA
Peak On-State Voltage	V_{TM}	$I_{TM} = 1\text{A}$	—	—	1.5	V
Gate Trigger Voltage	V_{GT}	$V_D = 6\text{V}$, $R_L = 100\Omega$ $R_{GK} = 1\text{k}\Omega$	—	—	0.8	V
Gate Trigger Current	I_{GT}		—	—	200	μA
Holding Current	I_H	$I_{TM} = 500\text{mA}$, $V_D = 6\text{V}$ $R_{GK} = 1\text{k}\Omega$	—	—	6	mA
Critical Rate of Rise of Off-State Voltage	dV / dt	$V_{DRM} = \text{Rated}$, $R_{GK} = 1\text{k}\Omega$ Exponential Rise	—	200	—	V / μs
Gate Turn-On Time	t_{gt}	$V_D = \text{Rated}$, $i_G = 5\text{mA}$ $R_{GK} = 1\text{k}\Omega$	—	—	1.5	μs
Thermal Resistance	$R_{th(j-a)}$	Junction to Ambient	—	—	70	$^{\circ}\text{C} / \text{W}$

Note: Thermal Resistance Test Condition
Use 0.6×30×30mm Alumina Plate







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