

US6K4

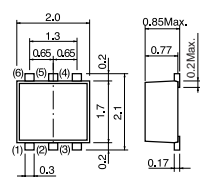
Silicon N-channel MOSFET

- 1) Two Nch MOSFETs are put in TUMT6 package.
- 2) High-speed switching, Low On-resistance.
- 3) 1.8V drive.

Switching

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
US6K4		○

TUMT6



Abbreviated symbol : K04

(1) Tr1 Source
(2) Tr1 Gate
(3) Tr2 Drain
(4) Tr2 Source
(5) Tr2 Gate
(6) Tr1 Drain

<It is the same ratings for the Tr1 and Tr2>

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DS}	20	V
Gate-source voltage		V_{GS}	± 10	V
Drain current	Continuous	I_D	± 1.5	A
	Pulsed	I_{DP}^{*1}	± 3.0	A
Source current (Body diode)	Continuous	I_S	0.6	A
	Pulsed	I_{SP}^{*1}	2.4	A
Total power dissipation		P_D^{*2}	1.0	W / TOTAL
			0.7	W / ELEMENT
Channel temperature		T_{ch}	150	$^{\circ}\text{C}$
Range of storage temperature		T_{stg}	-55 to +150	$^{\circ}\text{C}$

*1 $P_w \leq 10\mu s$, Duty cycle $\leq 1\%$
*2 Mounted on a ceramic board

Parameter	Symbol	Limits	Unit
Channel to ambient	Rth(ch-a) *	125	°C/W / TOTAL
		179	°C/W / ELEMENT

* Mounted on a ceramic board

Transistors

●Electrical characteristics (Ta=25°C)

<It is the same characteristics for the Tr1 and Tr2>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	—	—	±10	μA	$V_{GS}=\pm 10V$, $V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	20	—	—	V	$I_D=1mA$, $V_{GS}=0V$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS}=20V$, $V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	0.3	—	1.0	V	$V_{DS}=10V$, $I_D=1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	—	130	180	mΩ	$I_D=1.5A$, $V_{GS}=4.5V$
		—	170	240	mΩ	$I_D=1.5A$, $V_{GS}=2.5V$
		—	220	310	mΩ	$I_D=0.8A$, $V_{GS}=1.8V$
Forward transfer admittance	$ Y_{fs} $ *	1.6	—	—	S	$V_{DS}=10V$, $I_D=1.5A$
Input capacitance	C_{iss}	—	110	—	pF	$V_{DS}=10V$
Output capacitance	C_{oss}	—	18	—	pF	$V_{GS}=0V$
Reverse transfer capacitance	C_{rss}	—	15	—	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}$ *	—	5	—	ns	$I_D=1.0A$
Rise time	t_r *	—	5	—	ns	$V_{DD}\div 10V$
Turn-off delay time	$t_{d(off)}$ *	—	20	—	ns	$V_{GS}=4.5V$
Fall time	t_f *	—	3	—	ns	$R_L=10\Omega$
Total gate charge	Q_g *	—	1.8	2.5	nC	$V_{DD}\div 10V$
Gate-source charge	Q_{gs} *	—	0.3	—	nC	$V_{GS}=4.5V$
Gate-drain charge	Q_{gd} *	—	0.3	—	nC	$I_D=1.5A$

*Pulsed

●Body diode characteristics (Source-drain) (Ta=25°C)

<It is the same characteristics for the Tr1 and Tr2>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD}	—	—	1.2	V	$I_S=0.6A$, $V_{GS}=0V$

Transistors

●Electrical characteristics curves

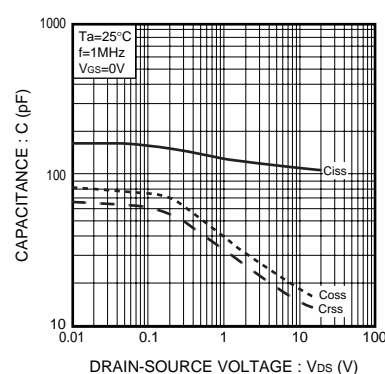


Fig.1 Typical Capacitance vs. Drain-Source Voltage

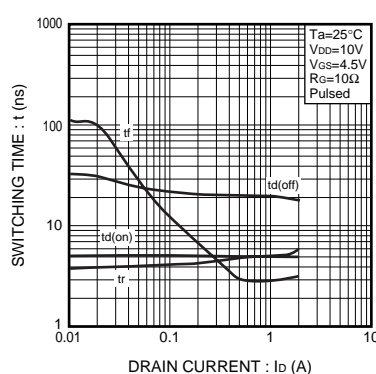


Fig.2 Switching Characteristics

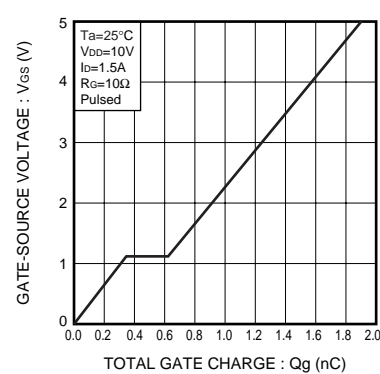


Fig.3 Dynamic Input Characteristics

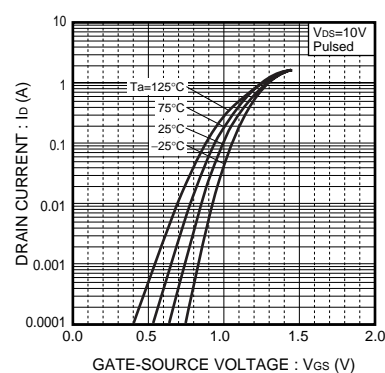


Fig.4 Typical Transfer Characteristics

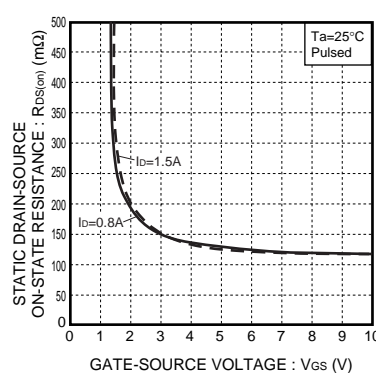


Fig.5 Static Drain-Source On-State Resistance vs. Gate-source Voltage

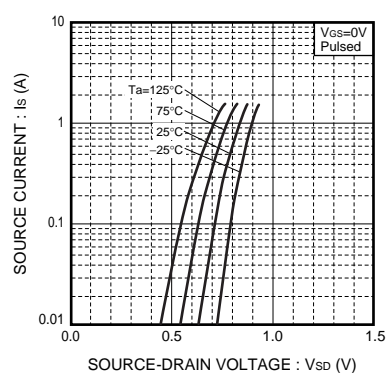


Fig.6 Source Current vs. Source-Drain Voltage

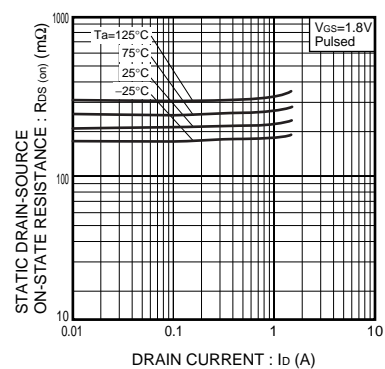


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (I)

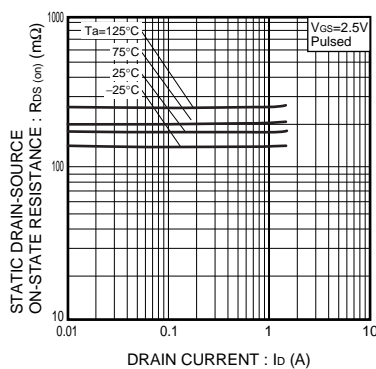


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (II)

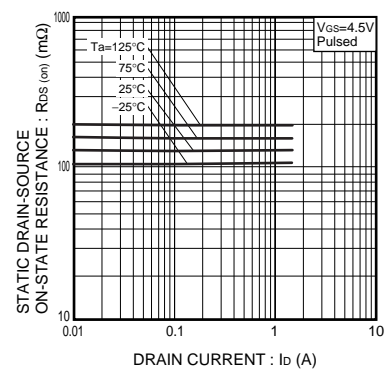


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (III)

●Notice

This product might cause chip aging and breakdown under the large electrified environment.
Please consider to design ESD protection circuit.

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