极景微半导体

US5S105 1.8V, 2.5V, 3.3V Low Skew LVCMOS Clock Buffer

Description

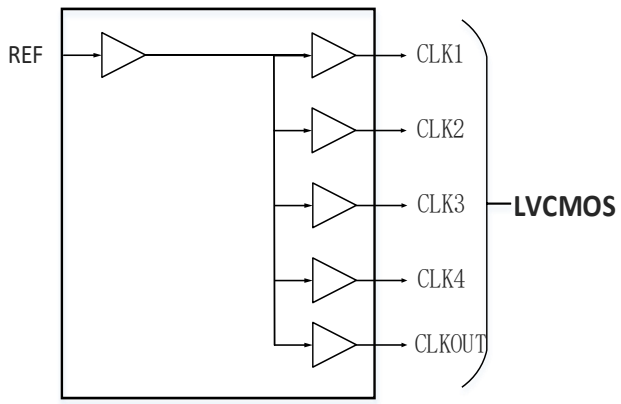
The US5S105 is a low skew, single input to five output, clock buffer. Part of Ultrasilicon’ Clock family, this is a low skew, small clock buffer.

Operates in a 1.8-V, 2.5-V and 3.3-V environment and are characterized for operation from －40° C to 85° C.

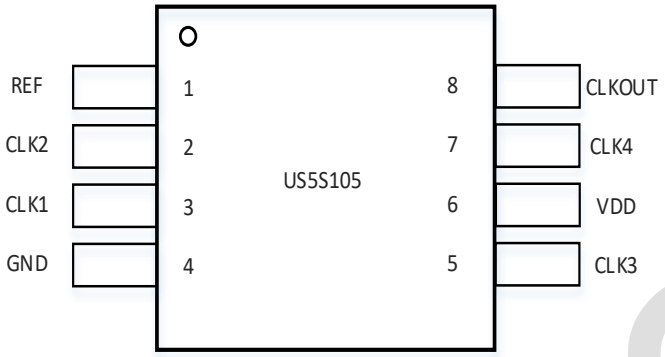
Features

- High-Performance 1:5 LVCMOS Clock Buffer
- Extremely low additive jitter < 25-fs nominal
- Output Skew < 50 ps (Typical)
- Very low propagation delay < 3 ns
- Synchronous Output Enable Is Available
- Outputs Operate up to 250 MHz for 3.3V
- Outputs Operate up to 200 MHz for 2.5V and 1.8V
- Supply voltage: 3.3V, 2.5V or 1.8V
- Industrial Temperature Range:-40°C to 85°C
- Available in 8-Pin SOP Package
- Pin-to-Pin Compatible to the CY2305

Block Diagram



Pin Assignmen



Pin Descriptions and Function Table

Pin Number	Pin Name	Pin Type	Pin Description
1	REF	Power	Single-ended clock input with internal 150-kΩ (typical) pulldown resistor to GND. Typically connected to a single-ended clock input.
2	CLK2	Output	LVCMOS Output 2,Typically connected to a receiver. Unused outputs can be left floating.
3	CLK1	Output	LVCMOS Output 1,Typically connected to a receiver. Unused outputs can be left floating.
4	GND	Power	Ground
5	CLK3	Input	LVCMOS Output 3,Typically connected to a receiver. Unused outputs can be left floating.
6	VDD	Output	Connect to +1.8V, +2.5V, +3.3V .
7	CLK4	Output	LVCMOS Output 4,Typically connected to a receiver. Unused outputs can be left floating.
8	CLKOUT	Input	LVCMOS CLKOUT.

Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied.

Item	Rating
V_{DD} : Supply voltage	0.5V to 3.6V
V_{CLKIN} : Input voltage (CLKIN)	
V_{Yn} : Output pins (Yn)	-0.5V to V_{DD} + 0.3 V
I_{IN} : Input current	-20mA to 20mA
I_O : Continuous output current	-50mA to 50mA
T_{STG} :Storage Temperature	-65°C to 150°C

ESD Ratings

		Max	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017	±4000	V
	Machine model (MM), JEDEC Std. JESD22-A115-C	±200	
	Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±750	

Latch up

		Max	Unit
Latch up	I-test, JEDEC STD JESD78E	±200	mA
	V-test, JEDEC STD JESD78E	4.6	V

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient air temperature	-40		85	°C
T_J	Junction temperature			125	°C
V_{DD}	Power supply for Core and input Buffer blocks	3.3-5% 2.5-5% 1-5%	3.3 2.5	3.3+5% 2.5+5%	V

DC Electrical Characteristics

VDD=1.8V ±5% , Ambient temperature 0 to +70°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		1.71		1.89	V
Input High Voltage, ICLK	VIH	Note 1	0.7*VDD			V
Input Low Voltage, ICLK	VIL	Note 1			0.3*VDD	V
Input High Voltage, OE	VIH		2		VDD	V
Input Low Voltage, OE	VIL				0.4	V
Output High Voltage	VOH	IOH = -45 mA	2.4			V
Output Low Voltage	VOL	IOL = 45 mA			0.8	V
Operating Supply Current	IDD	No load, 135 MHz		50		mA
Short Circuit Current	IOS			±80		mA

VDD=2.5V ±5%, Ambient temperature 0 to +70°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		2.375		2.625	V
Input High Voltage, ICLK	VIH	Note 1	0.7*VDD			V
Input Low Voltage, ICLK	VIL	Note 1			0.3*VDD	V
Input High Voltage, OE	VIH		2		VDD	V
Input Low Voltage, OE	VIL				0.4	V
Output High Voltage	VOH	IOH = -16 mA	2			V
Output Low Voltage	VOL	IOL = 16 mA			0.5	V
Operating Supply Current	IDD	No load, 135 MHz		25		mA
Short Circuit Current	IOS			±28		±28

VDD=3.3V ±5% , Ambient temperature 0 to +70°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.15		3.45	V
Input High Voltage, ICLK	VIH	Note 1	0.7*VDD			V
Input Low Voltage, ICLK	VIL	Note 1			0.3*VDD	V
Input High Voltage, OE	VIH		2		VDD	V
Input Low Voltage, OE	VIL				0.4	V
Output High Voltage	VOH	IOH = -25 mA	2.4			V
Output Low Voltage	VOL	IOL = 25 mA			0.8	V
Operating Supply Current	IDD	No load, 135 MHz		35		mA
Short Circuit Current	IOS			±50		mA

Notes: 1. Nominal switching threshold is VDD/2

AC Electrical Characteristics

VDD = 1.8V ±5%, Ambient Temperature 0 to +70° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t_{OR}	0.8 to 2.0V, C_L=15pF			1.5	ns
Output Fall Time	t_{OF}	2.0 to 0.8V, C_L=15pF			1.5	ns
Propagation Delay	Note 1			3		ns
Output to output skew	Note 2	Rising edges at VDD/2			50	ps

VDD = 2.5V ±5%, Ambient Temperature 0 to +70° C, unless stated otherwise

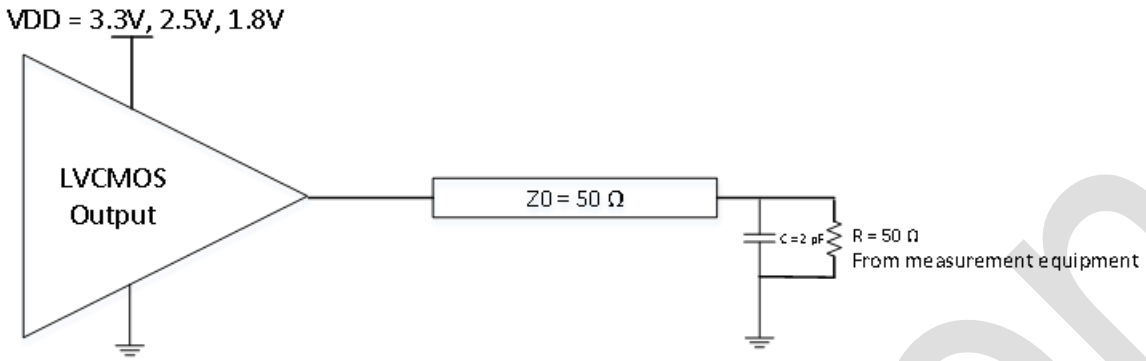
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t_{OR}	0.8 to 2.0V, C_L=15pF			1.5	ns
Output Fall Time	t_{OF}	2.0 to 0.8V, C_L=15pF			1.5	ns
Propagation Delay	Note 1			3		ns
Output to output skew	Note 2	Rising edges at VDD/2		0	50	ps

VDD = 3.3V ±5%, Ambient Temperature 0 to +70° C, unless stated otherwise

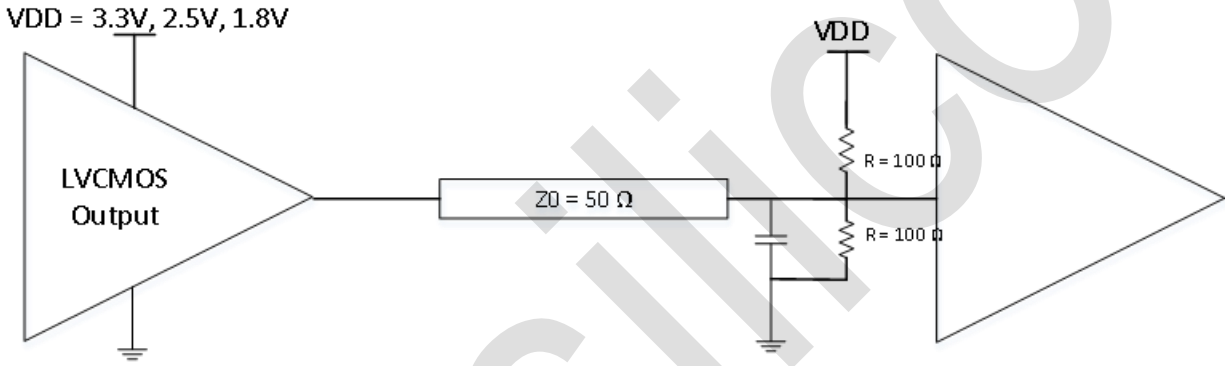
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		250	MHz
Output Rise Time	t_{OR}	0.8 to 2.0V, C_L=15pF			0.7	ns
Output Fall Time	t_{OF}	2.0 to 0.8V, C_L=15pF			0.7	ns
Output Fall Time	Note 1			2.5		ns
Output to output skew	Note 2	Rising edges at VDD/2		0	50	ps

Notes: 1. With rail to rail input clock
2. Between any 2 outputs with equal loading.
3. Duty cycle on outputs will match incoming clock duty cycle. Consult ICS for tight duty cycle clock generators.

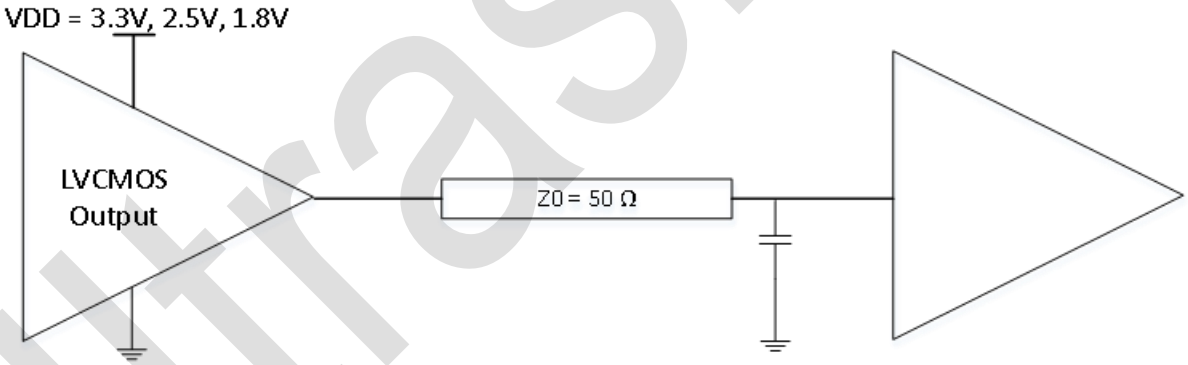
Parameter Measurement Information



Test Load Circuit

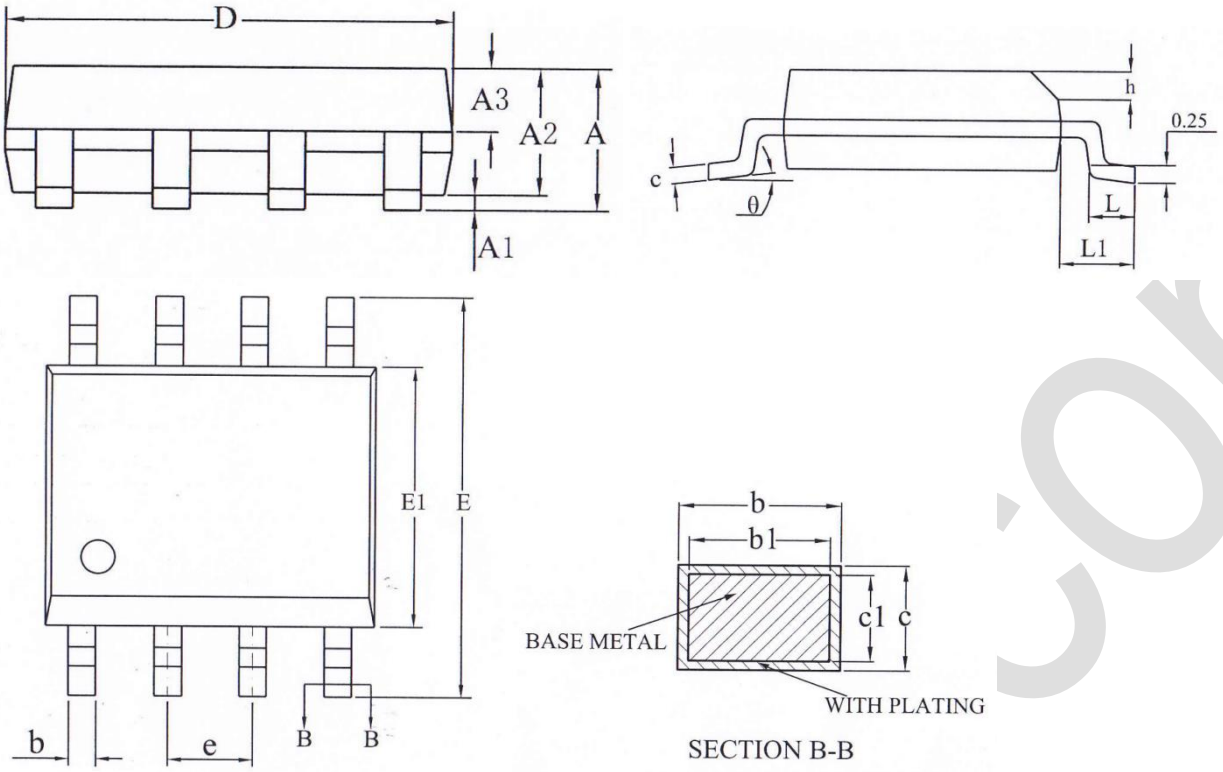


Application Load Witch 50-Ω Termination



Application Load With Termination

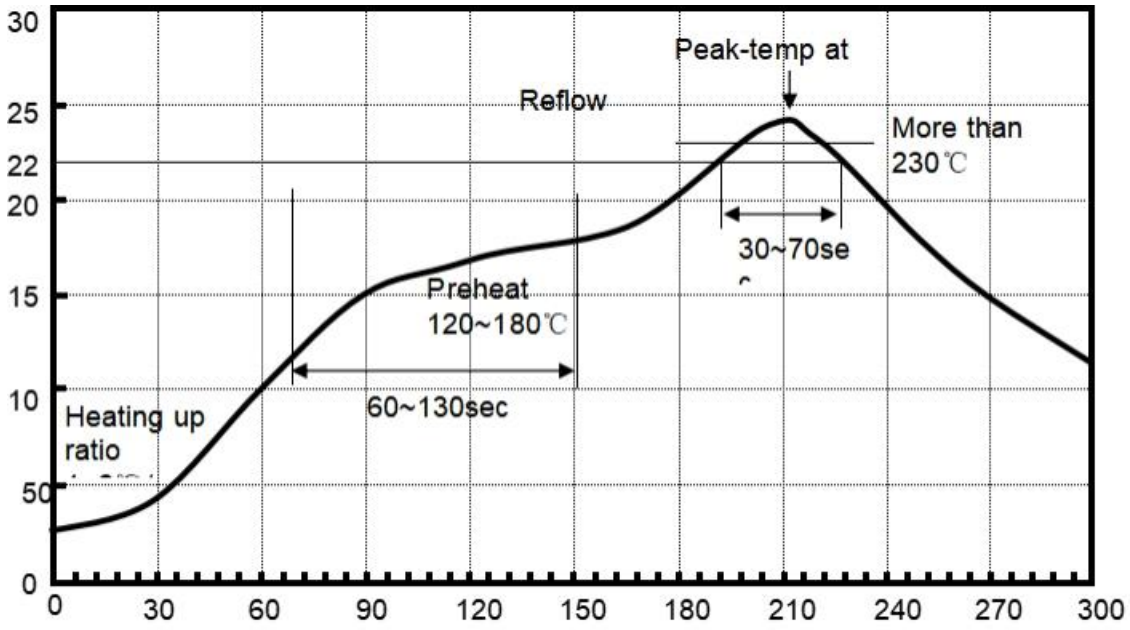
Package Outline and Package Dimensions (8 pin SOP)



Package dimensions are kept current with JEDEC Publication No. 95

Symbol	Millimeters		
	Min	Nom	Max
A	-	-	1.75
A1	0.10	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 Basic		
h	0.25	-	0.50
L	0.50	-	0.80
θ	0°	-	8°

Reflow profile



Recommended Temperature Sn95.5Ag4.0Cu0.5