



UPSR1103

Advance

CMOS IC

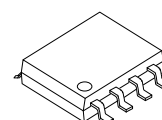
HIGH PRECISION CC/CV PRIMARY SIDE SWITCHING REGULATOR

■ DESCRIPTION

The UTC **UPSR1103** is a primary control unit for switch mode charger and adapter applications. The controlled variable is transferred by an auxiliary winding from the secondary to the primary side. The device integrates PWM controller to enhance the performance of discontinuous conduction mode (DCM) flyback converters.

The UTC **UPSR1103** operates in primary-side sensing and regulation. Opto-coupler and TL431 could be eliminated. It also provides off-time modulation to linearly decrease PWM frequency under light-load conditions so that low standby power can be achieved.

The UTC **UPSR1103** achieves high precision CV/CC regulation and high power efficiency. It offers comprehensive protection coverage with auto-recovery features including Cycle-by-cycle current limiting, VDD over voltage protection, VDD clamp, OTP, leading edge blanking, VDD under voltage lockout, etc.



SOP-8

■ FEATURES

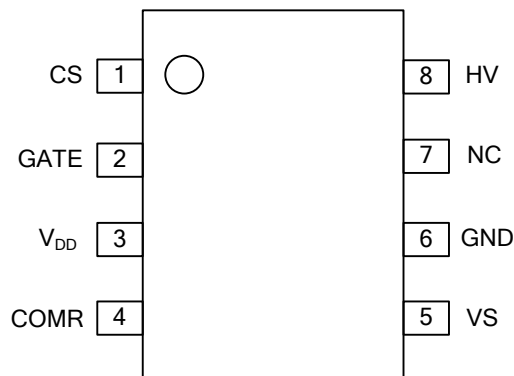
- * High voltage startup
- * $\pm 5\%$ constant voltage regulation at universal AC input
- * High precision constant current regulation at universal AC input
- * Primary side control without TL431 and opto-coupler
- * Programmable CV and CC regulation
- * Programmable cable compensation in CV mode
- * Flyback topology in DCM operation
- * Frequency hopping to reduce system EMI
- * Driver MOSFET switch
- * Built-in leading edge blanking
- * Built-in primary winding inductance compensation
- * Gate output maximum voltage clamped at 15V
- * Cycle-by-cycle current limiting
- * Over voltage protection
- * V_{DD} under-voltage lockout

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UPSR1103L-S08-T	UPSR1103G-S08-T	SOP-8	Tube

UPSR1103L-S08-T	(1)Packing Type (2)Package Type (3)Halogen Free	(1) T: Tube (2) S08: SOP-8 (3) L: Lead Free, G: Halogen Free
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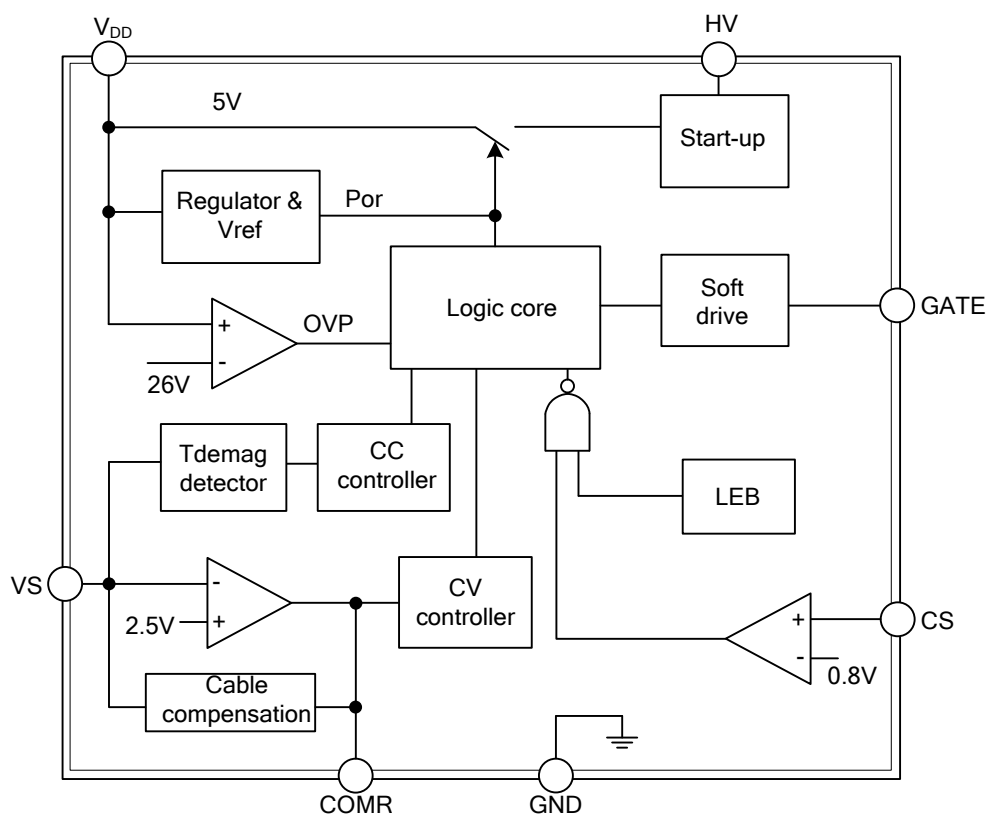
PIN CONFIGURATION



PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	CS	Current sense input.
2	GATE	Gate drive for power MOSFET.
3	VDD	Power supply.
4	COMR	Cable compensation.
5	VS	The voltage feedback from the auxiliary winding.
6	GND	Ground
7	NC	No connect
8	HV	High-voltage startup.

BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
HV Pin Input Voltage	V_{HV}	500	V
Supply Voltage	V_{DD}	30	V
Voltage at VS, CS, COMR to GND		-0.3~7.0	V
Power Dissipation ($T_A < 50^\circ\text{C}$)	P_D	660	mW
Operating Ambient Temperature	T_A	-40~+105	$^\circ\text{C}$
Operating Junction Temperature	T_J	-40~+150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55~+150	$^\circ\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	150	$^\circ\text{C/W}$
Junction to Case	θ_{JC}	39	$^\circ\text{C/W}$

■ ELECTRICAL CHARACTERISTICS ($V_{DD}=15\text{V}$, $T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY SECTION						
Turn-on Threshold Voltage	$V_{TH(ON)}$		13.5	14.5	15.5	V
Turn-off Threshold Voltage	$V_{TH(OFF)}$		8.5	9	9.5	V
VDD OVP Protection	V_{DD_OVP}			26		V
Operating Current	I_{DD-OP}			1.6	2	mA
Green-Mode Operating Current	$I_{DD-GREEN}$			1.3		mA
HV START-UP SECTION						
Minimum Startup Voltage on HV Pin	V_{HV-MIN}				50	V
Supply Current Drawn from Pin HV	I_{HV}	$V_{DC}=100\text{V}$		0.6		mA
Leakage Current after Startup	I_{HV-LC}	$HV=500\text{V}$, $V_{DD}=V_{DD-OFF}+1\text{V}$		0.5		μA
OSCILLATOR SECTION						
Maximum Frequency	f_{OSC}		47	50	53	kHz
Minimum Frequency at CCM	$f_{OSC-CM-MIN}$			13		kHz
Minimum Frequency at No-load	$f_{OSC-N-MIN}$			370		Hz
Frequency Hopping Range	$\Delta f/freq$		± 1.5	± 2.0	± 2.5	kHz
Frequency Hopping Period	t_{FHR}			3		ms
Frequency Variation vs. V_{DD} Deviation	f_{DV}	$V_{DD}=10\sim 25\text{V}$		1	2	%
Frequency Variation vs. Temperature Deviation	f_{DT}	$T_A=-40^\circ\text{C}\sim +105^\circ\text{C}$			15	%
VOLTAGE SENSE SECTION						
Reference Voltage for EA	V_{VR}		2.475	2.500	2.525	V
Reference Voltage for CCM	V_{VR_CCM}			0.5		V
Max. Cable Compensation Current	I_{CABLE_MAX}			45		μA
CURRENT SSENSE SECTION						
Current Sense Threshold Voltage	V_{CS}			800		mV
OCP Propagation Delay	t_{D_OC}			90	200	nS
Leading Edge Blank Time	t_{LEB}			400		nS
Soft Start Time	t_{SS}			10		mS

■ ELECTRICAL CHARACTERISTICS(Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GATE DRIVE SECTION						
Output Voltage Low	V_{OL}	$V_{DD}=15V, I_{O_sink}=20mA$			1.5	V
Output Voltage High	V_{OH}	$V_{DD}=15V, I_{O_source}=20mA$	5			V
Rising Time	t_R	$C_L=1nF$		200	250	nS
Falling Time	t_F	$C_L=1nF$		60	100	nS
Output Clamp Voltage	V_{CLAMP}	$V_{DD}=25V$		15	18	V
OTP SECTION						
Threshold Temperature of OTP (Note)	T_{OTP}			+140		°C

Note: When the over-temperature protection is activated, the power system enters auto restart mode and output is disabled.

■ OPERATION DESCRIPTION

The UTC **UPSR1103** is a primary control unit for switch mode charger and adapter applications. It operates in primary-side sensing and regulation. Opto-coupler and TL431 could be eliminated. Proprietary built-in CV and CC control can achieve high precision CV/CC performance. The device integrates PWM controller to enhance the performance of discontinuous conduction mode (DCM) flyback converters.

High-Voltage Startup control

The HV pin of UTC **UPSR1103** is connected to the line input through a resistor (100K is recommended). During startup, the internal startup circuit in UTC **UPSR1103** is enabled. Meanwhile, line input supplies a constant current to charge the hold-up capacitor through the resistor. When the VDD voltage reaches $V_{TH(ON)}$, the internal startup circuit is disabled and the IC turns on.

Operating Current

The operating current of UTC **UPSR1103** is as low as 1.6mA. Good efficiency and very low standby power can be achieved.

Constant Voltage Operation

The output voltage is defined by the transmission ratio between the secondary and auxiliary winding. The UTC **UPSR1103** captures the auxiliary winding feedback voltage at VS pin and operates in constant-voltage (CV) mode to regulate the output voltage. The auxiliary voltage reflects the output voltage is given by:

$$V_{AUX} = \frac{N_A}{N_S} \times (V_O + \Delta V) \quad (1)$$

Where ΔV indicates the drop voltage of the output diode.

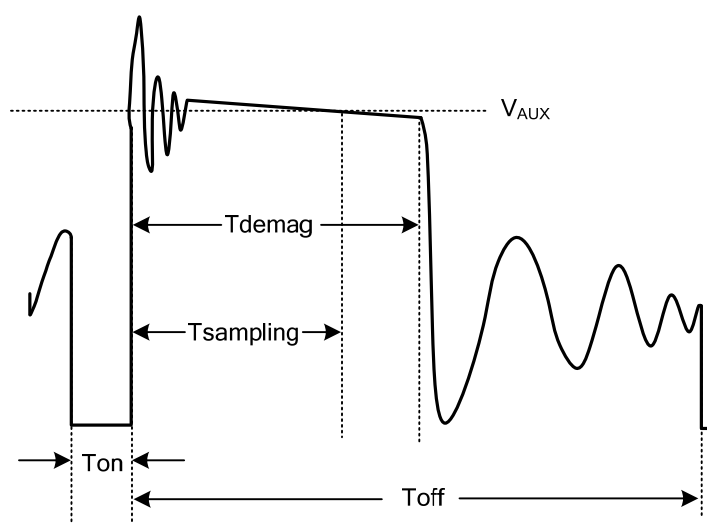


Figure2. Auxiliary voltage waveform

Via a resistor divider connected between the auxiliary winding and VS, the V_{AUX} is sampled at the $T_{sampling}$ end and it is hold until the next sampling. The sampled voltage is compared with 2.5V reference voltage and the error is amplified. The error amplifier output reflects the load condition and controls the T_{off} time and the I_{pk} to regulate the output voltage, thus constant output voltage can be achieved.

Constant Current Operation

When the sampled voltage is below 2.5V reference voltage and the error amplifier output reaches its maximum, thus UTC **UPSR1103** operates in constant-current (CC) mode. The CC point and maximum output power can be externally adjusted by external current sense resistor R_{cs} . The larger R_{cs} , the smaller CC point is, and the smaller output power becomes.

■ OPERATION DESCRIPTION(Cont.)

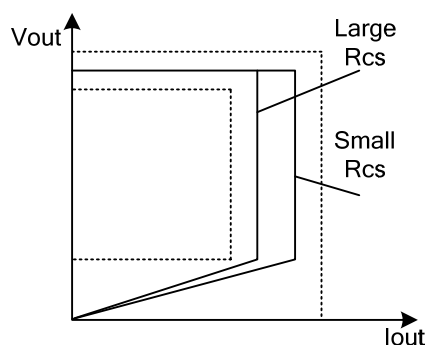


Figure3. Adjustable output power by changing Rcs

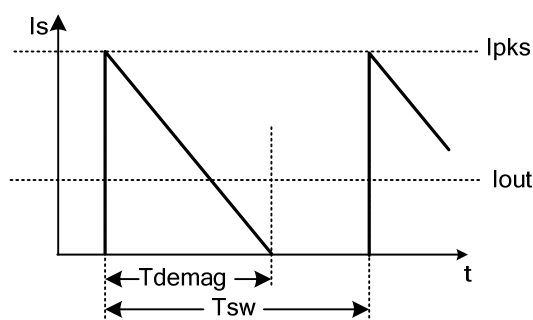


Figure4. Secondary current waveform

In CC operation, the CC loop control function of UTC **UPSR1103** will keep a fixed proportion between secondary inductance de-magnetization time (T_{demag}) and switching cycle time (T_{sw}). The fixed proportion is

$$\frac{T_{demag}}{T_{sw}} = \frac{1}{2} \quad (2)$$

Thus the output current is given by:

$$I_{out} = \frac{1}{2} \times \frac{N_p}{N_s} \times I_{pk} \times \frac{T_{demag}}{T_{sw}} = \frac{1}{4} \times \frac{N_p}{N_s} \times I_{pk} \quad (3)$$

Programmable Cable Drop Compensation

UTC **UPSR1103** has a built-in cable voltage drop compensation to achieve good load regulation. An offset voltage is generated at VS pin by an internal current flowing into the resistor divider. The current is inversely proportional to the voltage of COMR pin. As a result, it is inversely proportional to the output load current. The voltage drop across the cable is compensated by this offset voltage at VS pin. It can also be programmed by adjusting the resistance of the divider to compensate the drop for various cable lines used.

Current Sensing and Leading Edge Blanking

Cycle-by-cycle current limiting is offered in UTC **UPSR1103**. The switch current is detected by a sense resistor into the CS pin. When the power switch is turned on, a turn-on spike will occur on this resistor. A 500ns leading-edge blanking is built in to avoid false-termination of the switching pulse so that the external RC filtering is no longer needed.

■ OPERATION DESCRIPTION(Cont.)

Gate Output

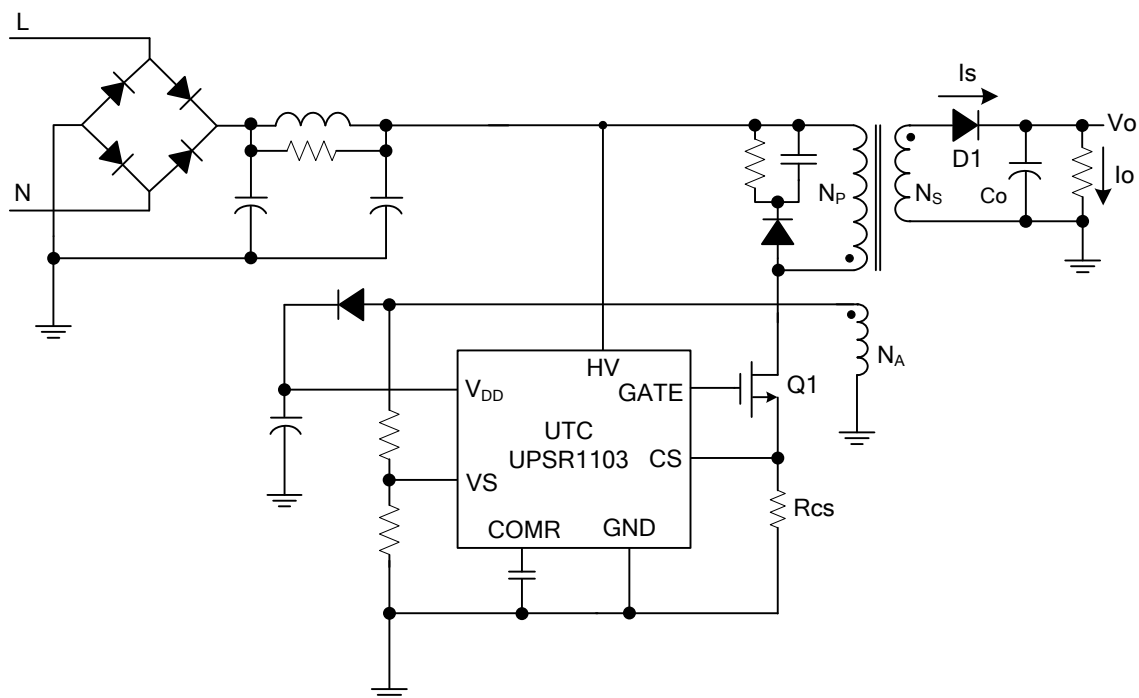
The UTC **UPSR1103** output stage is a fast totem-pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped at 15V to protect power MOSFET transistors against undesired over-voltage gate signals.

Protection Control

Good power supply system reliability is achieved with its comprehensive protection features including VDD over-voltage protection, VDD Clamp, GATE Clamp, Power on soft start, Cycle-by-cycle current limiting, short circuit protection, leading edge blanking, OTP and UVLO, etc.

VDD is supplied by transformer auxiliary winding output. The output of UTC **UPSR1103** is shutdown when VDD drops below $V_{TH(OFF)}$ and the power converter enters power on start-up sequence thereafter.

■ TYPICAL APPLICATION CIRCUIT



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