DATA SHEET

RENESAS

MOS INTEGRATED CIRCUIT

Phase-out/Discontinued

μPD9993

PCM SOUND GENERATOR AND MP3/AAC DECODER LSI (WITH REAL-TIME SURROUND) FOR MOBILE PHONES

DESCRIPTION

The μPD9993 is a PCM sound generator and MP3/AAC decoder LSI that includes an on-chip wide real-time surround function for mobile phones.

FEATURES

- PCM sound generation method provides realistic sound reproduction
- Built-in digital signal processor for MP3/AAC decoder
- Built-in real-time wide surround function
  (for all sources including PCM sound generators, MP3/AAC sources, and audio serial input)
- Up to 68 tones (= 64 polyphonic tones + 4 ADPCM) can be played at the same time, so an abundant variety of tunes can be generated and played
- Supports ADPCM playback. Simultaneous playback with MIDI is also enabled
- Includes a high-performance D/A converter with 16-bit resolution
- Supports five sampling frequency modes: 8 kHz, 16 kHz, 32 kHz, 44.1 kHz, and 48 kHz (ASI and MP3/AAC decoder)
- Provides audio serial I/O interface (16 bits). The serial data input frequency is variable between 32 fs and 64 fs (during slave mode). Supported formats are right-justified, left-justified, and IIS.
- Includes function for mixing MIDI/ADPCM/MP3/AAC signals and audio serial input signals (only fs = 32 kHz sampling is supported).
- Supports 8-bit parallel interface. The host CPU is connected via an 8-bit parallel interface when PS = 0.
- Supports SPI. The host CPU is connected via a 3-wire or a 4-wire serial peripheral interface (SPI) when PS = 1.
- Supports three outputs modes (single end MONO, differential MONO, and STEREO)
- Includes output control functions for vibrator and LED
- Built-in PLL, so various types of input clocks can be supported
- Supports two I/O power supply voltages: 1.8 to 3 V (supports only digital pins)
- Power supply voltages:
  - DV_{DD}: 1.425 to 1.575 V
  - EV_{DD}: 1.71 to 3.3 V
  - AV_{DD}: 2.7 to 3.3 V
  - AV_{DD}_P: 2.7 to 3.3 V
- 85-pin tape FBGA package (6 × 6 mm body size, 0.5 mm ball pitch)

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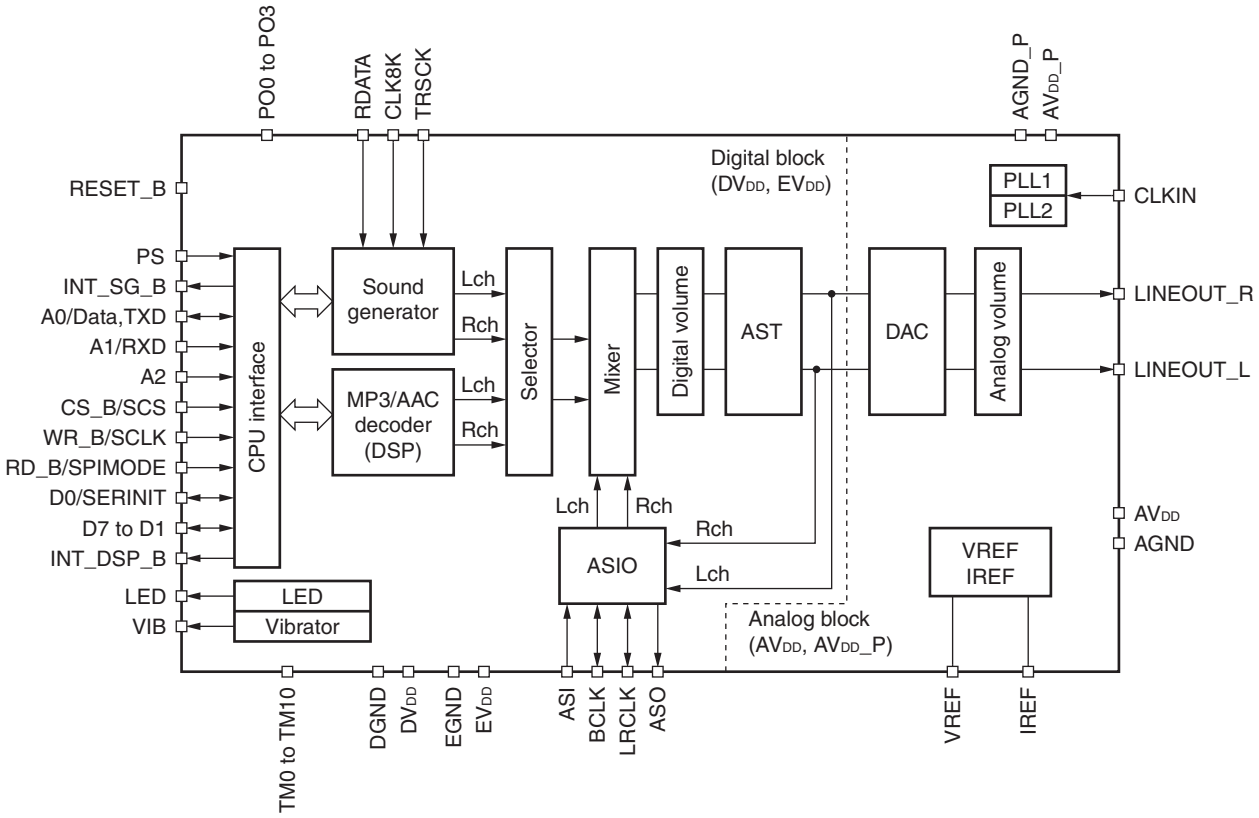
The mark ★ shows major revised points.

ORDERING INFORMATION

Part number	Package
μPD9993F9-BA3	85-pin tape FBGA (6 × 6)

★ BLOCK DIAGRAM

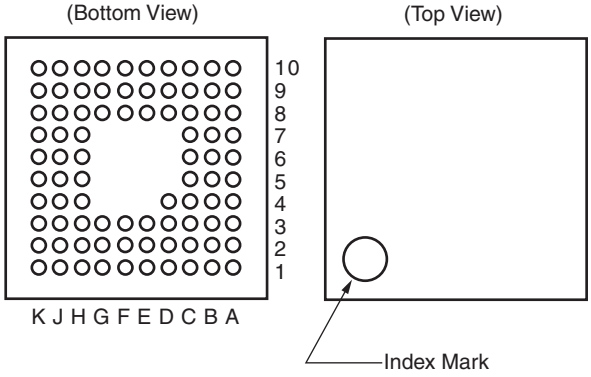


Remark AST: Adaptive Surround™ Technology and DiMAGIC Virtualizer X

PIN CONFIGURATION

- 85-pin tape FBGA (6 × 6)

  μPD9993F9-BA3



Pin No.	Pin Name
1A	Shorted with 1K Pin
1B	N.C
1C	LINEOUT_L
1D	AGND
1E	AV_{DD}
1F	LINEOUT_R
1G	AGND
1H	AGND_P
1J	N.C
1K	Shorted with 1A Pin
2A	N.C
2B	N.C
2C	TM0
2D	IREF
2E	VREF
2F	TM1
2G	AV_{DD}_P
2H	CLKIN
2J	N.C
2K	N.C
3A	TM3

Pin No.	Pin Name
3B	TM2
3C	N.C
3D	N.C
3E	N.C
3F	N.C
3G	N.C
3H	N.C
3J	PO1
3K	PO0
4A	RDATA
4B	TM4
4C	DV_{DD}
4D	N.C
4H	A2
4J	PO3
4K	PO2
5A	TRSCK
5B	CLK8K
5C	DGND
5H	TM5
5J	A1 / RXD

Pin No.	Pin Name
5K	DGND
6A	EGND
6B	PS
6C	TM9
6H	TM10
6J	CS_B / SCS
6K	A0 / Data, TXD
7A	ASI
7B	ASO
7C	TM6
7H	TM7
7J	RD_B / SPIMODE
7K	WR_B / SCLK
8A	LRCLK
8B	BCLK
8C	DV_{DD}
8D	TM8
8E	DGND
8F	INT_DSP_B
8G	N.C
8H	N.C

Pin No.	Pin Name
8J	D1
8K	D0 / SERINIT
9A	DV_{DD}
9B	N.C
9C	EV_{DD}
9D	VIB
9E	RESET_B
9F	D7
9G	D5
9H	D3
9J	N.C
9K	DV_{DD}
10A	Shorted with 10K Pin
10B	N.C
10C	LED
10D	DV_{DD}
10E	INT_SG_B
10F	D6
10G	D4
10H	D2
10J	DGND
10K	Shorted with 10A Pin

Caution Leave the N.C pins open.

PIN NAME

A0, A1, A2:	Address
ASI:	Audio serial data input
ASO:	Audio serial data output
AV_{DD}:	Power supply for analog block
AV_{DD}_P:	Power supply for PLL
AGND:	Ground for analog block
AGND_P:	Ground for PLL
BCLK:	Bit clock input/output
CS_B:	Chip select
CLK8K:	Sync clock input for RDATA
CLKIN:	Clock input
D0 to D7:	Data bus
DV_{DD}:	Power supply for digital block
DGND:	Ground for digital block
EV_{DD}:	Power supply for I/O pins
EGND:	Ground for I/O pins
INT_SG_B:	Interruption from PCM sound generator
INT_DSP_B:	Interruption from DSP (MP3/AAC decoder)
IREF:	Current reference for DAC
LED:	LED control output
LINEOUT_L:	Line out (left channel)
LINEOUT_R:	Line out (right channel)
LRCLK:	Left right clock input/output
N.C:	Non-connection
PO0 to PO3:	Peripheral output
PS:	Parallel/serial I/F select
RD_B:	Read
RDATA:	Record data
RESET_B:	Reset
TM0 to TM2 and TM5 to TM9:	Test mode input
TM3,TM4, TM10:	Test mode output
TRSCK:	Clock input for RDATA
VIB:	Vibrator control output
VREF:	Voltage reference for DAC
WR_B:	Write

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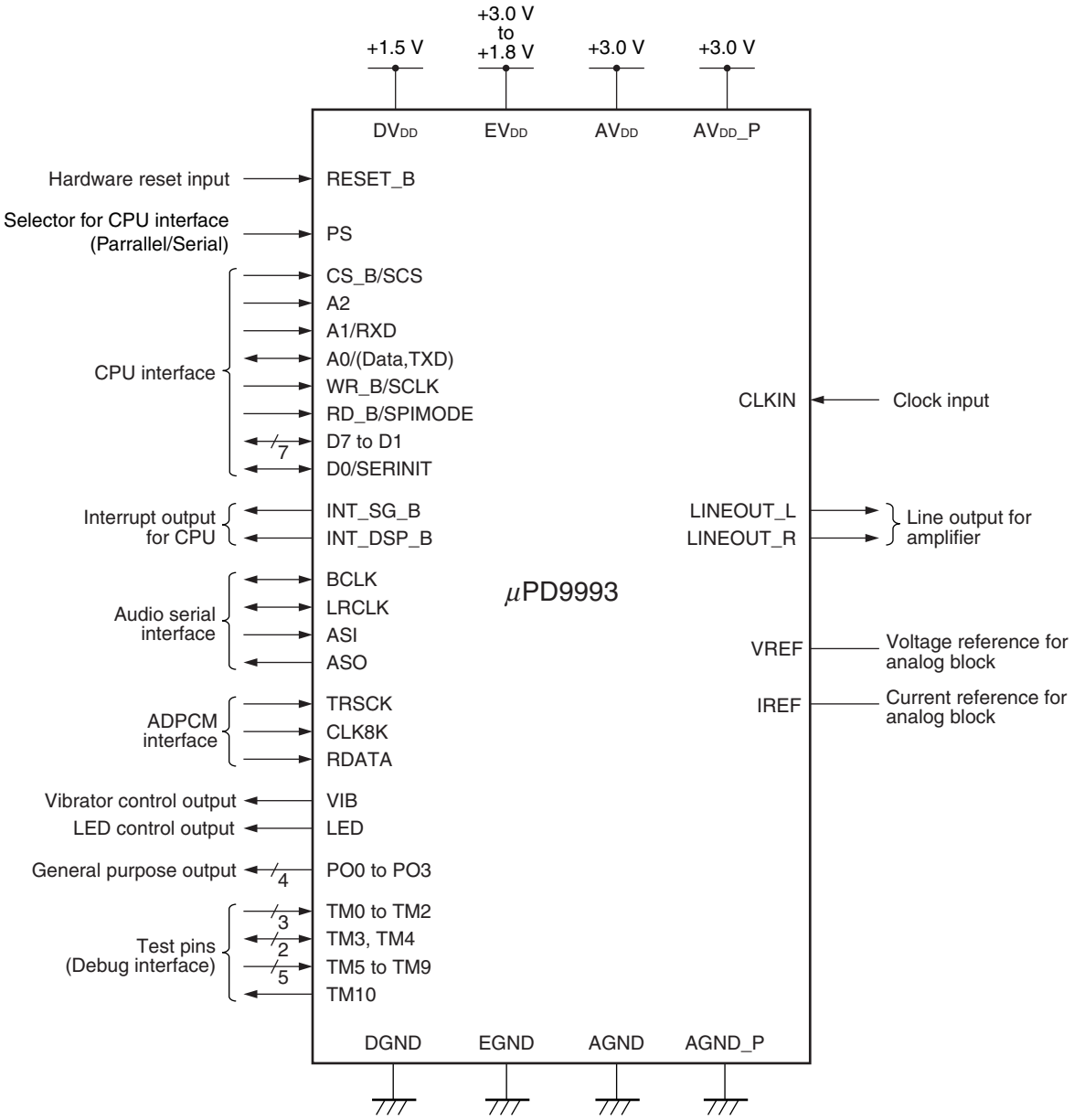
1. PIN FUNCTIONS

1.1 Pin Configuration



1.2 Explanation of Pin Functions

(1) Power supply pins

Pin Name	Pin No.	I/O	Function
DV_{DD}	9A, 9K, 10D, 4C, 8C	–	Power supply (1.425 V to 1.575 V) for digital block Be sure to connect a 0.1 μF capacitor between this pin and DGND.
DGND	5K, 10J, 5C, 8E	–	Ground for digital block
EV_{DD}	9C	–	Power supply (1.71 V to 3.3 V) for I/O Be sure to connect a 0.1 μF capacitor between this pin and EGND.
EGND	6A	–	Ground for I/O
AV_{DD}	1E	–	Power supply (2.7 V to 3.3 V) for analog Be sure to connect a 0.1 μF capacitor between this pin and AGND.
AGND	1D, 1G	–	Ground for analog block
AV_{DD}_P	2G	–	Power supply (2.7 V to 3.3 V) for PLL Be sure to connect a 0.1 μF capacitor between this pin and AGND-P.
AGND_P	1H	–	Ground for PLL block
VREF	2E	–	Reference voltage for analog block Be sure to connect a 0.22 μF capacitor between this pin and AGND.
IREF	2D	–	Reference current for analog block Be sure to connect a 56 kΩ resistor between this pin and AGND.

(2) Clock and system control pins

Pin Name	Serial No.	I/O	Function
CLKIN	2H	Input	Clock input This is the reference clock input that is used to generate the internal master clock. Be sure to input using capacitive coupling (1000 pF).
RESET_B	9E	Input	Hardware reset input signal This resets the μPD9993. Registers are initialized to their initial values after a reset.

(3) Host interface pins **(1/2)**

Pin Name	Pin No.	I/O	Function
A0 / (Data ,TXD)	6K	I/O	1. Parallel I/F mode (when PS = 0) Host interface address A0 signal input This input pin indicates the internal register address or data during host CPU access. 1: When transferring data 0: When setting address of internal register to be accessed
			2. Serial I/F mode (when PS = 1) • Bidirectional TX/RX serial data input/output (when PS = 1 and RD_B = 0) In this case, this pin is used as 3-wire SPI mode • TX serial data output (when PS = 1 and RD_B = 1) In this case, this pin is used as 4-wire SPI mode
A1 / RXD	5J	Input	1. Parallel I/F mode (when PS = 0) Host interface address A1 signal input This input pin selects the access destination register during host CPU access. A1 = 0 and A2 = 0 : Chip control register A1 = 0 and A2 = 1 : DSP for MP3/AAC decoder A1 = 1 and A2 = 0 : PCM sound generator A1 = 1 and A2 = 1 : Prohibited
			2. Serial I/F mode (when PS = 1) RX serial data input (when PS = 1 and RD_B = 1) In this case, this pin is used as 4-wire SPI mode
A2	4H	Input	1. Parallel I/F mode (when PS = 0) Host interface address A2 signal input This input pin selects the access destination register during host CPU access. A1 = 0 and A2 = 0 : Chip control register A1 = 0 and A2 = 1 : DSP for MP3/AAC decoder A1 = 1 and A2 = 0 : PCM sound generator A1 = 1 and A2 = 1 : Prohibited Connect this pin (A2) to GND, when not used.
CS_B/ SCS	6J	Input	1. Parallel I/F mode (when PS = 0) Chip select input for parallel I/F This is the input pin for the host interface select signal. This pin is set as active (low) while the host CPU accesses a host interface register.
			2. Serial I/F mode (when PS = 1) Chip select input for serial I/F
RD_B/ SPIMODE	7J	Input	1. Parallel I/F mode (when PS = 0) Host read input This pin is set as active (low) while the host CPU reads a host interface register. Do not set this pin and the WR_B pin as active at the same time.
			2. Serial I/F mode (when PS = 1) 3-wire/4-wire SPI mode select 1: 4-wire SPI mode 0: 3-wire SPI mode

(3) Host interface pins **(2/2)**

Pin Name	Pin No.	I/O	Function
WR_B/ SCLK	7K	Input	1. Parallel I/F mode (when PS = 0) Host write input This pin is set as active (low) while the host CPU writes to a host interface register. Do not set this pin and the RD_B pin as active at the same time.
			2. Serial I/F mode (when PS = 1) Clock for serial I/F
D0/ SERINIT	8K	I/O	1. Parallel I/F mode (when PS = 0) Bit 0 for 8-bit host data bus When the host CPU accesses the μPD9993, address and data I/O is performed. When the CS_B signal is inactive (high), this pin is set to high impedance.
			2. Serial I/F mode (when PS = 1) Initialization signal for serial I/F
D1 to D7	8J, 10H, 9H, 10G, 9G, 10F, 9F	I/O	1. Parallel I/F mode (when PS = 0) Bits 7-0 for 8-bit host data bus When the host CPU accesses the μPD9993, address and data I/O is performed. When the CS_B signal is inactive (high), this bus is set to high impedance.
			2. Serial I/F mode (when PS = 1) This bus is always set to high impedance. Connect these pins to GND.
INT_SG_B	10E	Output	Interrupt request from PCM sound generator This signal requests interrupt from the μPD9993 to the host CPU. This is used when requesting data transfer or internal status notification.
INT_DSP_B	8F	output	Interrupt request from DSP (MP3/AAC decoder) This signal request interrupt from the μPD9993 to the host CPU. This is used when requesting data transfer or internal status notification.
PS	6B	Input	Parallel/serial I/F mode setting 1: Serial I/F mode 0: Parallel I/F mode This pin has an internal pull-down resister (50 kΩ)

(4) Exterior LED, Vibrator control output pins

Pin Name	Pin No.	I/O	Function
LED	10C	Output	External LED control output This is the port output pin. Settings are entered by writing values to the port setting register from the host CPU. Leave this pin open when not used.
VIB	9D	Output	External vibrator control output This is the port output pin. Settings are entered by writing values to the port setting register from the host CPU. Leave this pin open when not used.

(5) Audio serial interface pins

Pin Name	Pin No.	I/O	Function
BCLK	8B	I/O	Bit synchronization clock I/O for audio serial This pin is used to input or output a bit synchronization clock for audio serial. Connect this pin to GND when not used.
LRCLK	8A	I/O	Audio serial frame synchronization clock I/O This pin is used to input or output a frame sync signal for serial transfers. Connect this pin to GND when not used.
ASO	7B	Output	Audio serial data output The audio serial data frame size is set via registers. During master mode, either 64 bits or 32 bits can be selected. During slave mode, selections can be made in 2-bit steps within a range from 32 to 64 bits. Leave this pin open when not used.
ASI	7A	Input	Audio serial data input The audio serial data frame size is set via registers. During master mode, either 64 bits or 32 bits can be selected. During slave mode, selections can be made in 2-bit steps within a range from 32 to 64 bits. Leave this pin open when not used. Pull-down is performed internally.

(6) ADPCM interface pins

Pin Name	Pin No.	I/O	Function
TRSCK	5A	Input	Serial clock input for ADPCM recording Pull-down is performed internally. Leave this pin open when not used.
CLK8K	5B	Input	Synchronization clock input for ADPCM recording Pull-down is performed internally. Leave this pin open when not used.
RDATA	4A	Input	Data input for ADPCM recording Pull-down is performed internally. Leave this pin open when not used.

(7) DAC, line out output pins

Pin Name	Pin No.	I/O	Function
LINEOUT_L	1C	Output	SOUND GENERATOR line out (L-ch) output This pin outputs the left-channel analog signal for line out function.
LINEOUT_R	1F	Output	SOUND GENERATOR line out (R-ch) output This pin outputs the right-channel analog signal for line out function.

(8) General-purpose external output pins

Pin Name	Pin No.	I/O	Function
PO0 to PO3	3K, 3J, 4K, 4J	Output	General-purpose external output pins These pins can be used to output control signals to peripheral devices.

(9) Test pins

Pin Name	Pin No.	I/O	Function
TM0 to TM2	2C, 2F, 3B	Input	Input for test Leave open or connect to GND. Pull-down is performed internally.
TM3, TM4	3A, 4B	I/O	I/O for test Leave open.
TM5, TM6	5H, 7C	Input	Input for test Leave open or connect to EV_{DD}. Pull-up is performed internally.
TM7 to TM9	7H, 8D, 6C	Input	Input for test Leave open or connect to GND.
TM10	6H	Output	Output for test Leave open.

(10) Others

Pin Name	Pin No.	I/O	Function
N.C	1B, 1J, 2A, 2B, 2J, 2K, 3C, 3D, 3E, 3F, 3G, 3H, 4D, 8G, 8H, 9B, 9J, 10B	–	Reserved pin for compatibility with future products. Leave this pin open.

1.3 Connection of Unused Pins

It is recommended to connect the unused pins as shown in the table below.

Pin Name	I/O	Recommended Connection
ASI	Input	Leave open or connect to GND.
A1	Input	Connect to GND.
A2	Input	Connect to GND.
TRSCK	Input	Leave open or connect to GND.
CLK8K	Input	Leave open or connect to GND.
RDATA	Input	Leave open or connect to GND.
TM0 to TM2	Input	Leave open or connect to GND.
TM5, TM6	Input	Leave open or connect to EV_{DD}.
TM7 to TM9	Input	Leave open or connect to GND.
D1 to D7	I/O	Connect to GND when SPI mode is selected (PS = 1).
LRCLK	I/O	Connect to GND.
BCLK	I/O	Connect to GND.
TM3, TM4	I/O	Leave open.
PO0 to PO3	Output	Leave open.
ASO	Output	Leave open.
VIB	Output	Leave open.
LED	Output	Leave open.
INT_DSP_B	Output	Leave open.
TM10	Output	Leave open.

Caution Leave the N.C pins open.

1.4 Initial State of Pins

Pin Name	I/O	During Reset	After Reset
VIB	Output	Low-level output	Low-level output
LED	Output	Low-level output	Low-level output
INT_SG_B	Output	High-level output	High-level output
INT_DSP_B	Output	High-level output	High-level output
ASO	Output	Hi-Z	Hi-Z
BCLK	I/O	Hi-Z	Input
LRCLK	I/O	Hi-Z	Input
TM3, TM4	I/O	Hi-Z	Low-level output
PO0 to PO3	Output	Low-level output	Low-level output
D7 to D0	I/O	Hi-Z	Input
TM10	Output	Hi-Z	Hi-Z

1.5 Pin Status

The μPD9993's pin status table is shown below.

(1/2)

Pin No.	I/O	Analog/ Digital	Pin Name	Internal Pull-Down/ Pull-Up	Standby Status		Reset Status (RESET_B = Low)		After Reset Status
					Control signal	Pin Status	Control signal	Pin Status	
2F	Input		TM1	Pull-Down	None	Input	None	Input	Input
2C	Input	Digital	TM0	Pull-Down	None	Input	None	Input	Input
1C	Output	Analog	LINEOUT_L	–	STDAC	Hi-Z	STDAC	Hi-Z	Hi-Z
1D	–	Analog	AGND	–	–	–	–	–	–
2D	Output	Analog	IREF	–	**Note 1**	Hi-Z	Note 1	Hi-Z	Hi-Z
2E	Output	Analog	VREF	–	**Note 1**	Hi-Z	Note 1	Hi-Z	Hi-Z
1E	–	Analog	AV_{DD}	–	–	–	–	–	–
1F	Output	Analog	LINEOUT_R	–	STDAC	Hi-Z	STDAC	Hi-Z	Hi-Z
1G	–	Analog	AGND	–	–	–	–	–	–
1H	–	Analog	AGND_P	–	–	–	–	–	–
2H	Input	Analog	CLKIN	–	STPLL1,2	Hi-Z	STPLL1,2	Hi-Z	Hi-Z
2G	–	Analog	AV_{DD}_P	–	–	–	–	–	–
3K	I/O	Digital	PO0	–	None	**Note 2**	RESET_B	Low output	Low output
3J	I/O	Digital	PO1	–	None	**Note 2**	RESET_B	Low output	Low output
4K	I/O	Digital	PO2	–	None	**Note 2**	RESET_B	Low output	Low output
4J	I/O	Digital	PO3	–	None	**Note 2**	RESET_B	Low output	Low output
5K	–	Digital	DGND	–	–	–	–	–	–
4H	Input	Digital	A2	–	None	Input	None	Input	Input
5J	Input	Digital	A1	–	None	Input	None	Input	Input
6K	I/O	Digital	A0	–	None	Input	None	Input	Input
9k	–	Digital	DV_{DD}	–	–	–	–	–	–
6J	Input	Digital	CS_B	–	None	Input	None	Input	Input
7K	Input	Digital	WR_B	–	None	Input	None	Input	Input
7J	Input	Digital	RD_B	–	None	Input	None	Input	Input
8K	I/O	Digital	D0	–	None	Input	RESET_B	Hi-Z	Input
8J	I/O	Digital	D1	–	None	Input	RESET_B	Hi-Z	Input
10H	I/O	Digital	D2	–	None	Input	RESET_B	Hi-Z	Input
9H	I/O	Digital	D3	–	None	Input	RESET_B	Hi-Z	Input
10G	I/O	Digital	D4	–	None	Input	RESET_B	Hi-Z	Input
9G	I/O	Digital	D5	–	None	Input	RESET_B	Hi-Z	Input
10F	I/O	Digital	D6	–	None	Input	RESET_B	Hi-Z	Input
9F	I/O	Digital	D7	–	None	Input	RESET_B	Hi-Z	Input
10J	–	Digital	DGND	–	–	–	–	–	–
10E	Output	Digital	INT_SG_B	–	None	Output	RESET_B	High	High output
8F	Output	Digital	INT_DSP_B	–	None	Output	RESET_B	High	High output
9E	Input	Digital	RESET_B	–	None	Input	None	Input	Input

Notes 1. STDAC, STPLL1 and STPLL2

2. Differs according to register setting.

(2/2)

Pin No.	I/O	Analog/ Digital	Pin Name	Internal Pull-Down/ Pull-Up	Standby Status		Reset Status (RESET_B = Low)		After Reset Status
					Control signal	Pin Status	Control signal	Pin Status	
10D	–	Digital	DV_{DD}	–	–	–	–	–	–
4C/8C	–	Digital	DV_{DD}	–	–	–	–	–	–
5C/9E	–	Digital	DGND	–	–	–	–	–	–
9D	Output	Digital	VIB	–	None	**Note 1**	RESET_B	Low output	Low output
10C	Output	Digital	LED	–	None	**Note 1**	RESET_B	Low output	Low output
9C	–	Digital	EV_{DD}	–	–	–	–	–	–
8A	I/O	Digital	LRCLK	–	STASI, STASO	**Note 2**	RESET_B	Hi-Z	Input
8B	I/O	Digital	BCLK	–	STASI, STASO	**Note 2**	RESET_B	Hi-Z	Input
7A	Input	Digital	ASI	Pull-Down	STASI, STASO	**Note 2**	None	Input	Input
7B	Output	Digital	ASO	–	STASI, STASO	**Note 2**	RESET_B	Hi-Z	Hi-Z
6A	–	Digital	EGND	–	–	–	–	–	–
9A	–	Digital	DV_{DD}	–	–	–	–	–	–
6B	Input	Digital	PS	Pull-Down	None	Input	None	Input	Input
5A	Input	Digital	TRSCK	Pull-Down	None	Input	None	Input	Input
5B	Input	Digital	CLK8K	Pull-Down	None	Input	None	Input	Input
4A	Input	Digital	RDATA	Pull-Down	None	Input	None	Input	Input
4B	I/O	Digital	TM4	–	STDIG	Low output	RESET_B	Hi-Z	Low output
3A	I/O	Digital	TM3	–	STDIG	Low output	RESET_B	Hi-Z	Low output
3B	Input	Digital	TM2	Pulll-Down	None	Input	None	Input	Input
5H	Input	Digital	TM5	Pull-up	None	Input	None	Input	Input
7C	Input	Digital	TM6	Pull-Down	None	Input	None	Input	Input
7H	Input	Digital	TM7	Pull-Down	None	Input	None	Input	Input
8D	Input	Digital	TM8	Pull-Down	None	Input	None	Input	Input
6C	Input	Digital	TM9	Pull-Down	None	Input	None	Input	Input
6H	Output	Digital	TM10	Pull-Up	None	Hi-Z	RESET_B	Hi-Z	Hi-Z

Notes 1. Differs according to register setting.

2. For description of the status of the LRCLK, BCLK, ASI, and ASO pins during standby mode, see Table 1-1.

Table 1-1. Pin Status in ASIO Block

Pin No.	I/O	Analog/ Digital	Pin Name	MS = 0 (Slave)				MS = 1 (Master)			
				[STASI, STASO]				[STASI, STASO]			
				[0, 0]	[0, 1]	[1, 0]	[1, 1]	[0, 0]	[0, 1]	[1, 0]	[1, 1]
8A	I/O	Digital	LRCLK	Input[Note]	Input	Input	Input	Fixed to low	Output	Output	Output
8B	I/O	Digital	BCLK	Input[Note]	Input	Input	Input	Fixed to low	Output	Output	Output
7A	Input	Digital	ASI	Invalid	Invalid	Input	Input	Invalid	Invalid	Input	Input
7B	Output	Digital	ASO	Hi-Z	Output	Hi-Z	Output	Hi-Z	Output	Hi-Z	Output

Note Fixed to low level internally

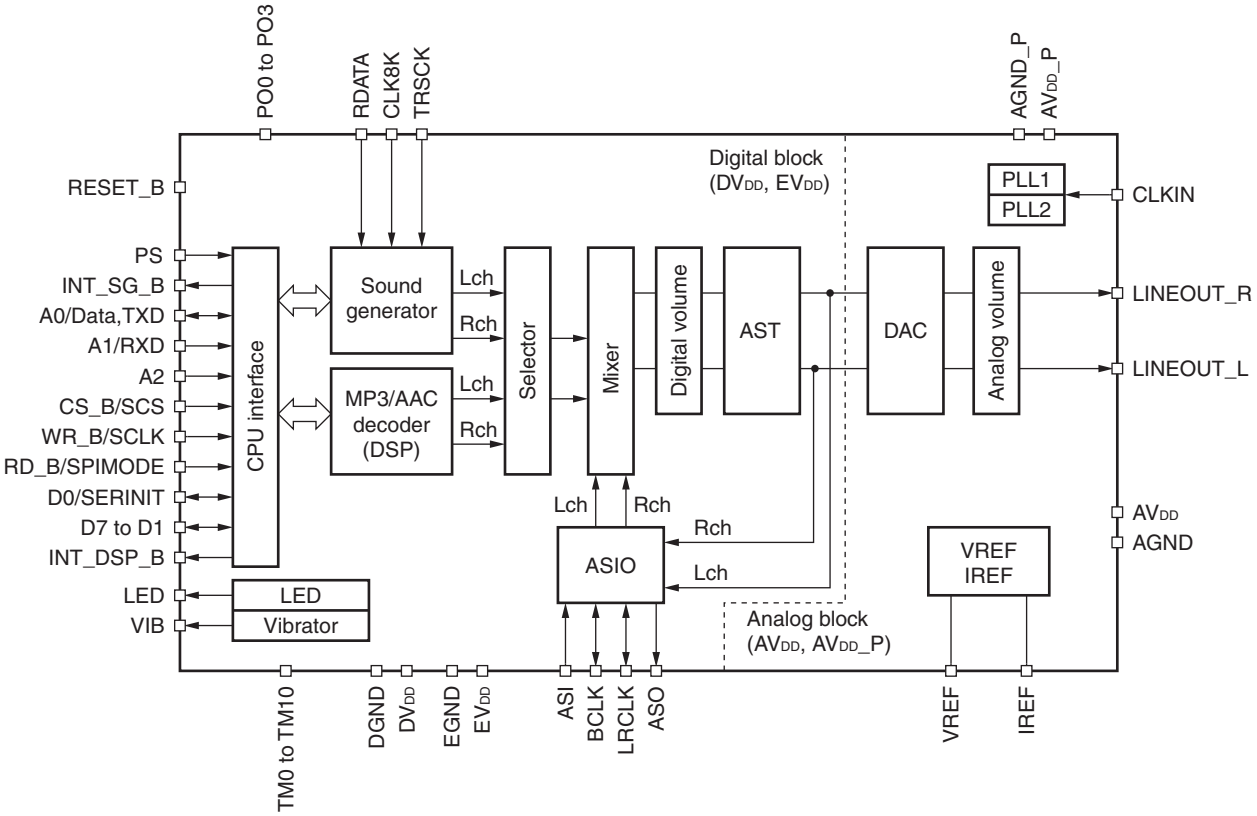
Remarks 1. MS is bit D2 in the SLASI register (08H).

2. STASI and STASO are bits D4 and D3 in the STNBY register (00H).

2. GENERAL DESCRIPTION

★ 2.1 Block Diagram

Figure 2-1. Block Diagram



(1) PLL1, PLL2 (CLKIN pin)

Clock input in the range from 2.688 to 26 MHz is supported.

In this block, when a clock with a frequency in this range is input, it is multiplied by the PLL to generate the fixed frequency clock that is required internally. PLL1 generates the clock signals required by all blocks except for the sound generator block and MP3/AAC decoder block, and PLL2 generates the clock signal for the sound generator block and MP3/AAC decoder block. After activation, normal operation begins after at least 5 ms have elapsed.

(2) CPU interface

This connects to the host CPU via an 8-bit parallel interface or 3/4-wire serial peripheral interface (SPI).

(3) Vibrator, LED control output port

This is an output port for the LED and vibrator.

(4) PCM sound generator block

A PCM sound generator for generation of up to 64 simultaneous tones is on chip, along with a sequencer. The sampling frequency is 32 kHz. The playback function for ADPCM is also on chip. The sampling frequency options are 8 kHz × 4 channels, 16 kHz × 2 channels, and 32 kHz × 1 channel.

(5) Digital signal processor block for decoding MP3/AAC

The μPD9993 has a high-performance digital signal processor for decoding MP3/AAC. For decoding, firmware needs to be downloaded from external memory.

Only the MP3/AAC decoder or PCM sound generator (MIDI/ADPCM) can be selected. Therefore both cannot operate at the same time. Selection of the MP3/AAC decoder and PCM sound generator is performed by setting command register.

(6) Audio serial I/O interface

This is an I/O interface for external audio data.

Five sampling frequency modes are supported: 8 kHz, 16 kHz, 32 kHz, 44.1 kHz, and 48 kHz (Initial value is 32 kHz).

The serial data input frequency is variable.

(7) Selector/mixer

This block is used to switch among or mix the sound generator (or the MP3/AAC decoder) and audio serial input.

(8) AST (surround)

This block performs real-time surround processing.

(9) DAC

This block converts digital signals to analog signals.

This DAC (D/A converter) is a high-performance stereo DAC with 16-bit resolution.

(10) General-purpose output ports (PO0-PO3)

The PO0-PO3 ports can be directly controlled by the host CPU. It is also possible to use these ports as additional LED ports.

(11) Soft Volume & Mute

A Digital Soft Volume & Mute function is built in. It is possible to change the digital volume gradually.

3. HOST CPU INTERFACE

Two I/F modes are available: parallel I/F mode, and serial I/F mode. The access methods from the host CPU interface are described below.

3.1 Parallel I/F Mode

The parallel I/F mode is entered by setting the PS pin to low level.

3.1.1 Write access

During write access, data is written to the μPD9993 from the system. The write access timing is shown in Figures 3-1 and 3-2.

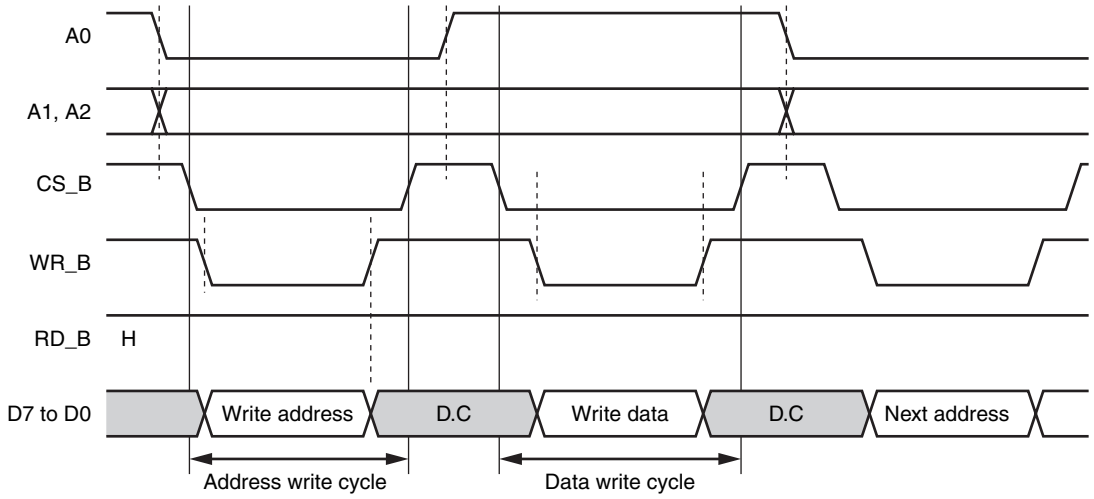
- A0 is used to distinguish between address write cycles and data write cycles.
- A1 and A2 are used to distinguish between register access for the sound generator, MP3/AAC decoder (DSP), and chip control register. The combinations of A1 and A2 are as follows.

  A1 = 0 and A2 = 0: Chip control register
  A1 = 0 and A2 = 1: DSP for MP3/AAC decoder
  A1 = 1 and A2 = 0: PCM sound generator
  A1 = 1 and A2 = 1: Prohibited

- In the address write cycle, the data write address is assigned to bits D7 to D0.
- Operation is based on detection of the rising edge of WR_B by the system clock.

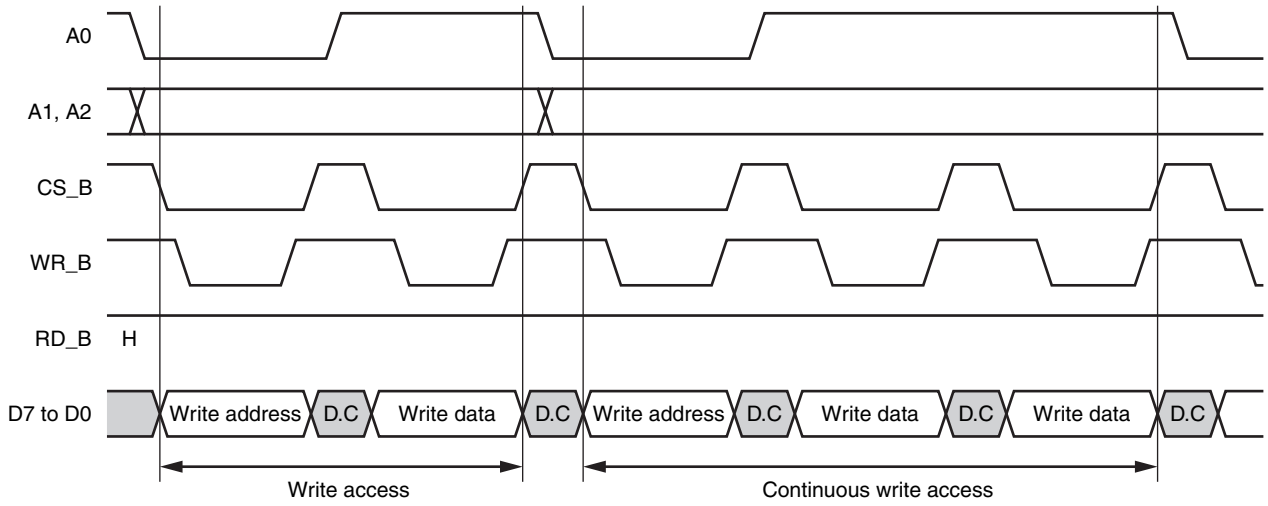
Caution Be sure to fix the RD_B pin to high level during address write cycles and data write cycles.

Figure 3-1. Write Access (Single Access)



Remark Set the CS_B pin to low level during the write period (WR_B = Low).
D.C: Don't care

Figure 3-2. Write Access (Continuous Access)



Remark Set the CS_B pin to low level during the write period (WR_B = Low).
D.C: Don't care

Continuous write access must be used in case of FIFO access, firmware download, HIO access, and AST RAM access.

The write access mode is selected by the written address. The transmit direction is also specified in "Write data" in the above figure.

3.1.2 Read access

During read access, data is read from the system by the μPD9993. The read access timing is shown below.

- A0 is used to distinguish between address write cycles and data read cycles.
- A1 and A2 are used to between among register access for the sound generator, MP3/AAC decoder (DSP), and chip control register. The combinations of A1 and A2 are as follows.

  A1 = 0 and A2 = 0 : Chip control register
  A1 = 0 and A2 = 1 : DSP for MP3/AAC decoder
  A1 = 1 and A2 = 0 : PCM sound generator
  A1 = 1 and A2 = 1 : Prohibited

- Operation is based on detection of the rising edge of WR_B and RD_B by the system clock.
- In the address write cycle, the data write address is assigned to bits D7 to D0.

Figure 3-3. Read Access (Single Access)

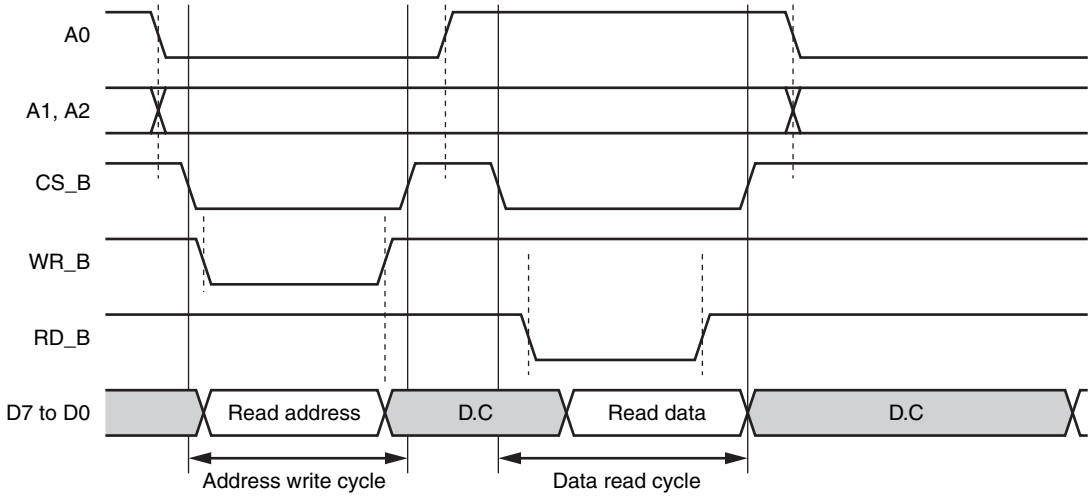
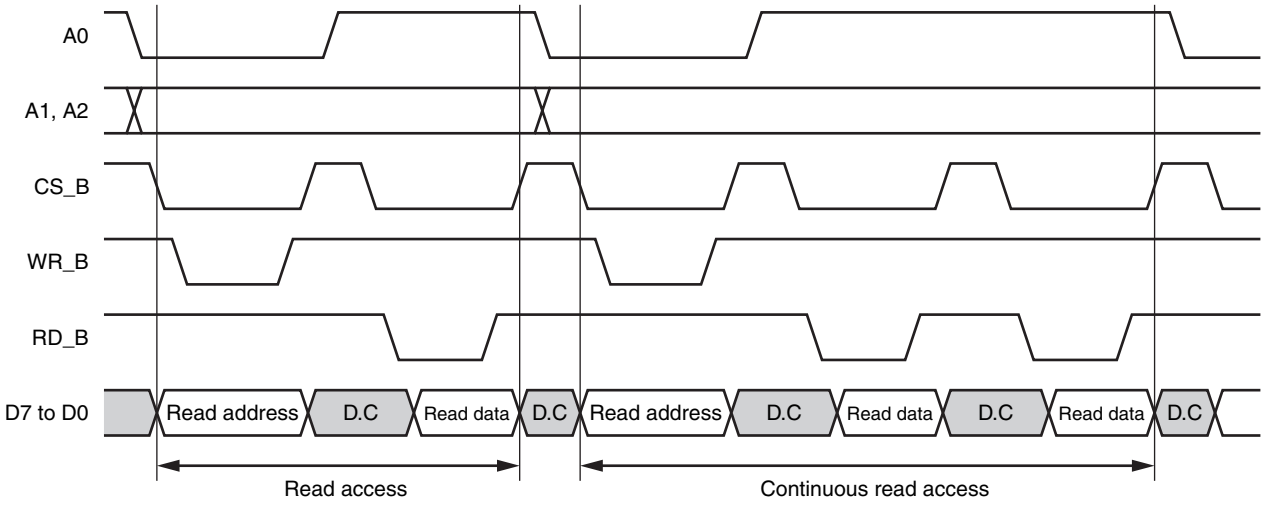
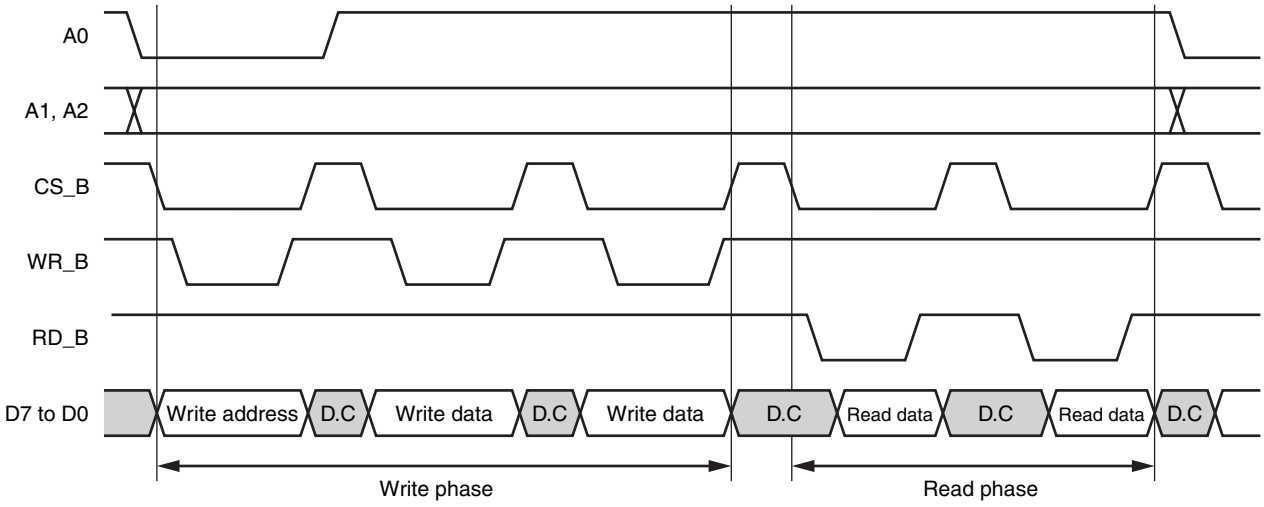


Figure 3-4. Read Access (Continuous Access for FIFOs)



Remark Set the CS_B pin to low level during the read period (RD_B) = Low).
D.C: Don't care

Figure 3-5. Read Access (Continuous Access for Firmware, HIO and AST RAM)



Continuous write access must be used in case of FIFO access, firmware download, HIO access, and AST RAM access.

The write access mode is selected by the written address. The transmit direction is also specified in "Write data" in the above figure.

3.2 Serial I/F Mode

The Serial I/F mode is entered by setting the PS pin to high level. In this mode, there are two communication methods: 3-wire SPI mode and 4-wire SPI mode. The SPIMODE (RD_B) pin is used to switch the SPI mode.

(1) Pin functions

Pin Name	Function	I/O
PS	Select of host CPU interface mode (0: Parallel, 1: Serial)	I
SPIMODE(RD_B)	Select of SPI mode (0: 3-wire SPI mode, 1: 4-wire SPI mode)	I
SCLK (WR_B)	Serial data clock	I
SCS (CS_B)	Chip select signal from host CPU	I
Data, TXD (A0)	Serial TX/RX data from/to host CPU When SPIMODE (RD_B) = 0, this pin is bidirectional. When SPIMODE (RD_B) = 1, this pin is the TXD output.	I/O
RXD (A1)	Serial RX data from host CPU When RD_B = 1, this pin is the RXD input.	I
SERINIT(D0)	Initialization signal for serial I/F When SCS (CS_B) = 1, the serial I/F is asynchronously initialized when SERINIT (D0) = 1. (The initializing condition is SCS = 1 and SERINIT = 1.)	I

Remark ( ) means the pin name in parallel I/F mode.

To use serial interface mode, the PS pin must be high level.

When the SCS pin is high level, the Data, TXD pin will go into a high-impedance state.

★ The SCS pin must be high level after completion of read operation.

(2) Format of serial host CPU interface

Read/Write Control	1 bit	(High: Write access, Low: Read access)
Address	7 bits	
Data	8 bits	
Total	16 bits	

(a) Register area

This melody LSI has 3 bank registers (sound generator, DSP for MP3/AAC decoder, and chip control). Switching of these registers is performed by writing a value to a specific address (4FH: Bank register).

(b) Access format

- Normal write access
- Normal read access
- Continuous access (1)
- Continuous access (2) for sound generator's FIFOs
- Continuous access (3) for firmware download, HIO access, and AST RAM access

The access format is selected by the written address. See **7. REGISTERS** for details.

3.2.1 Access format in 3-wire SPI mode

Figure 3-6. Format of Host CPU Access (Period of Read/Write Access)

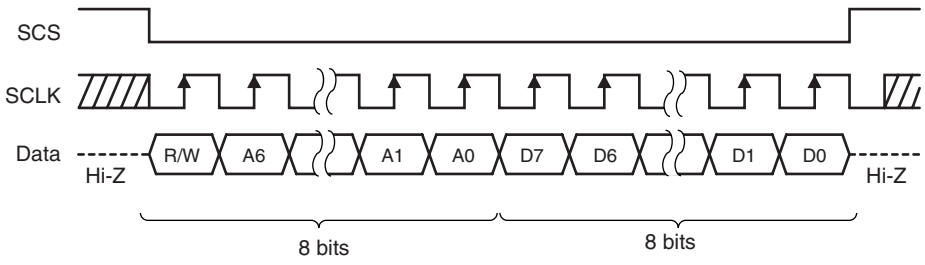
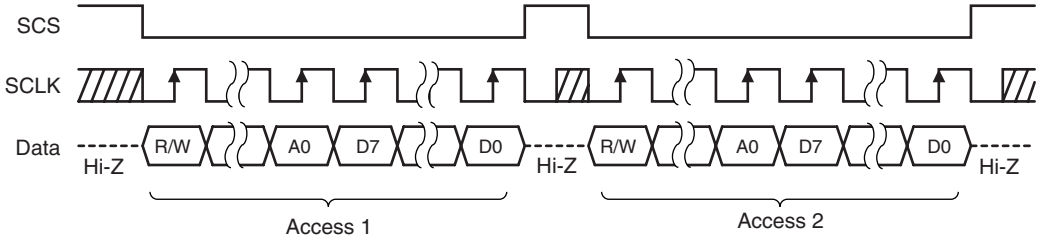
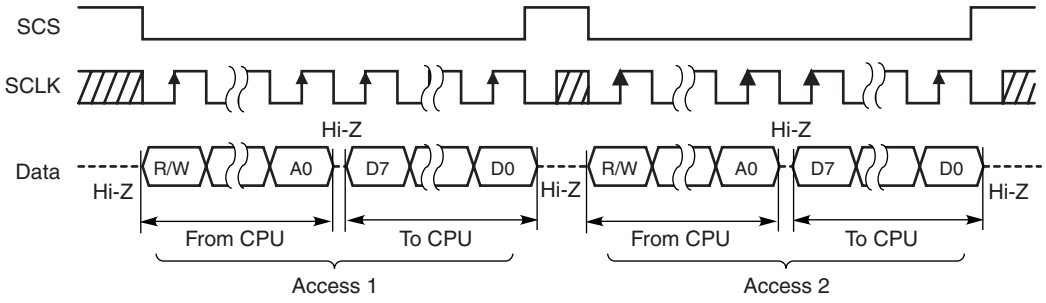


Figure 3-7. Format of Host CPU Access - Continuous Access (1)

(a) Write access



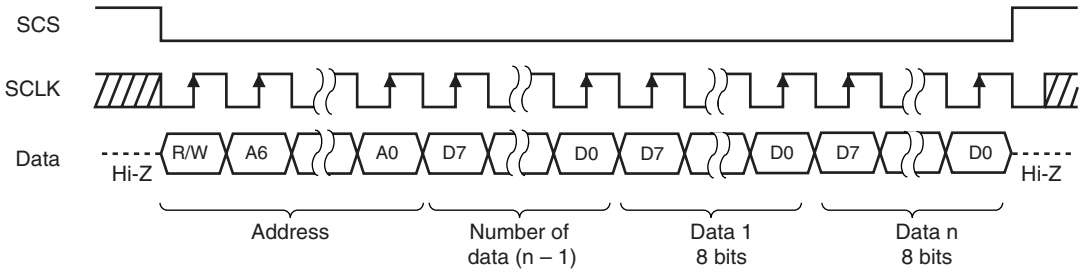
(b) Read access



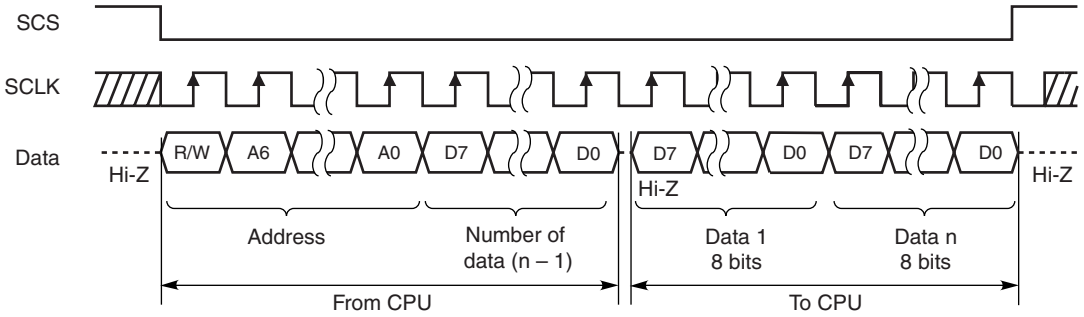
Remark The above formats are used except when accessing FIFOs in the sound generator block, and during firmware download, HIO access, and AST RAM access.

Figure 3-8. Format of Host CPU Access - Continuous Access (2)
for FIFOs in Sound Generator Block

(a) Write access



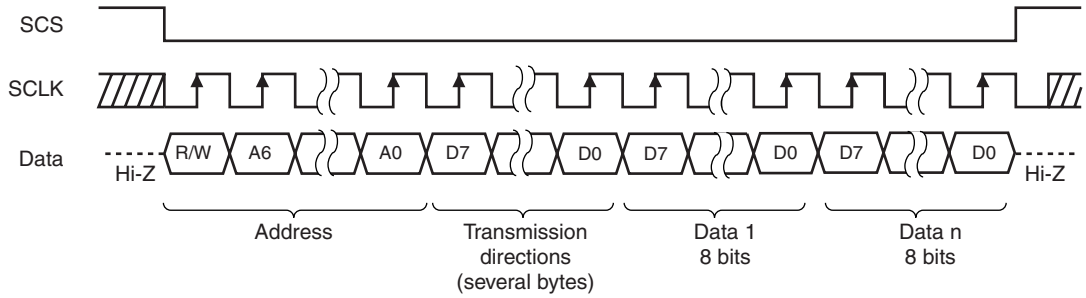
(b) Read access



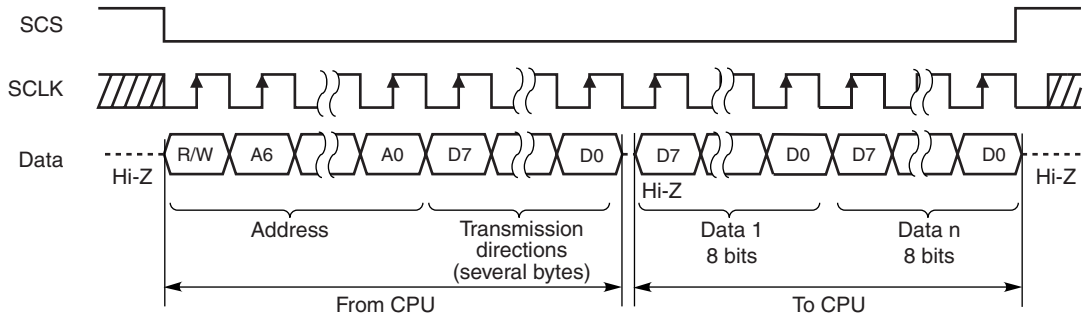
Remark The above formats are only used to access FIFOs in the sound generator block.

Figure 3-9. Format of Host CPU Access - Continuous Access (3)
for Firmware Download, HIO Access, and AST RAM Access

(a) Write access



(b) Read access



Remark The above formats are only used for access firmware download, HIO access, and AST RAM access.

3.2.2 Access format in 4-wire SPI mode

Figure 3-10. Format of Host CPU Access (A period of read/write access)

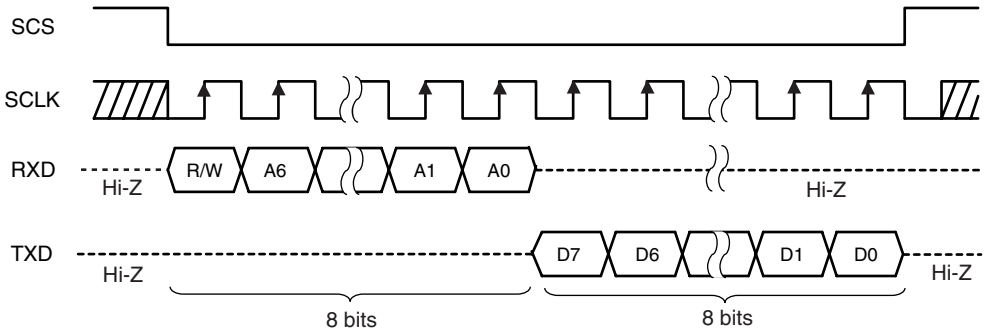
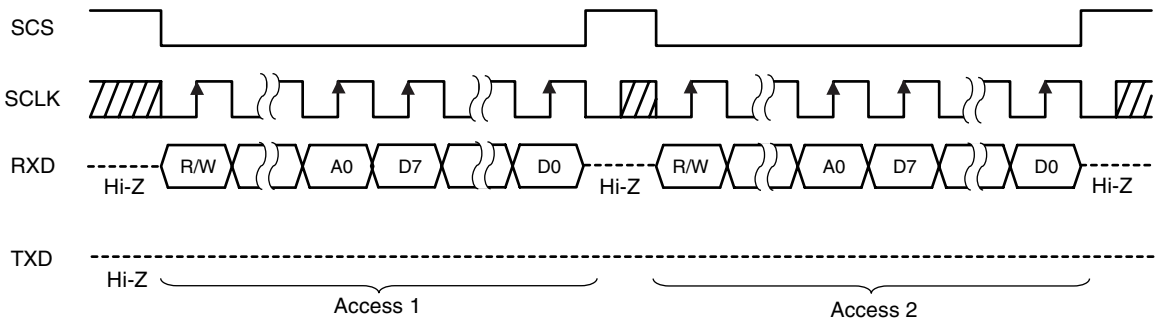
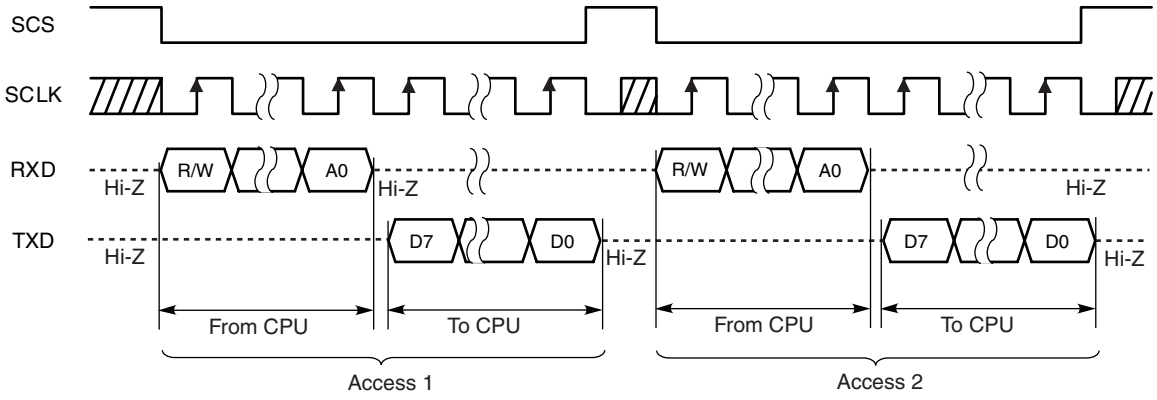


Figure 3-11. Format of Host CPU Access - Continuous Access (1)

(a) Write access



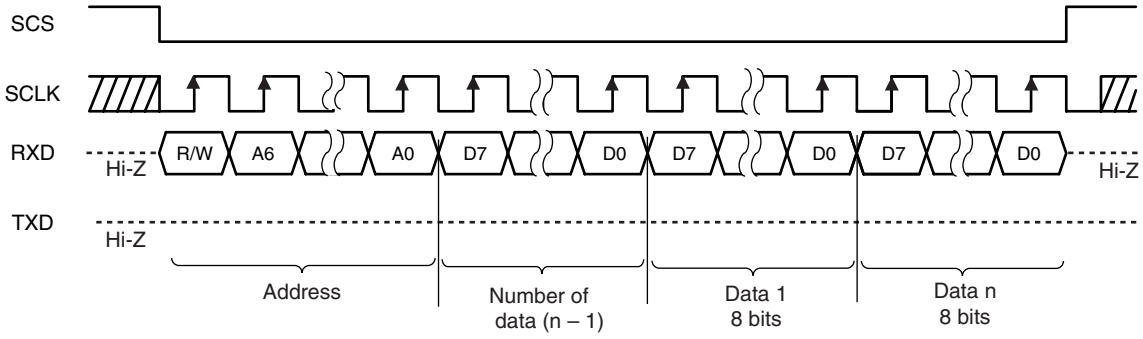
(b) Read access



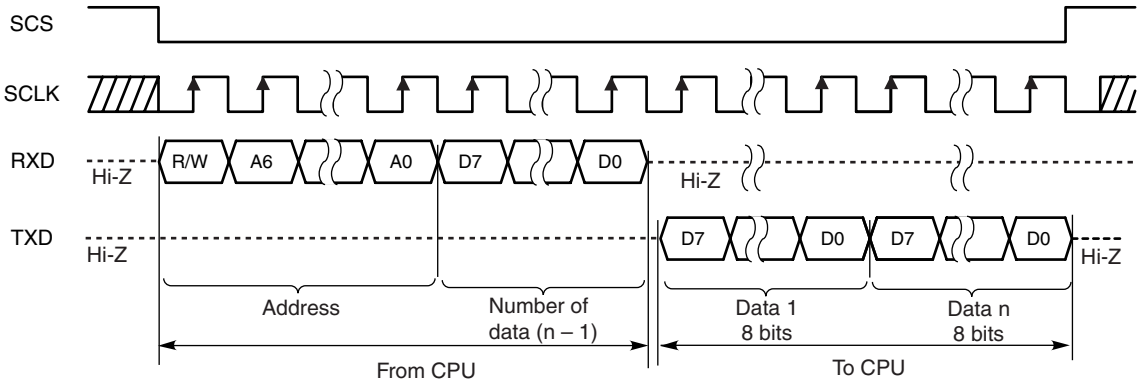
Remark The above formats are used except when accessing FIFOs in the sound generator, and during firmware download, HIO access, and AST RAM access.

Figure 3-12. Format of Host CPU Access - Continuous Access (2)
for FIFOs in Sound Generator Block and AST RAM

(a) Write access



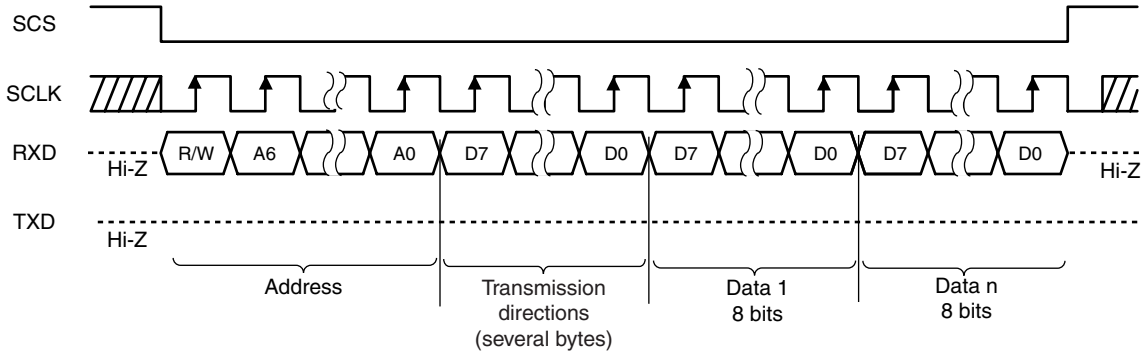
(b) Read access



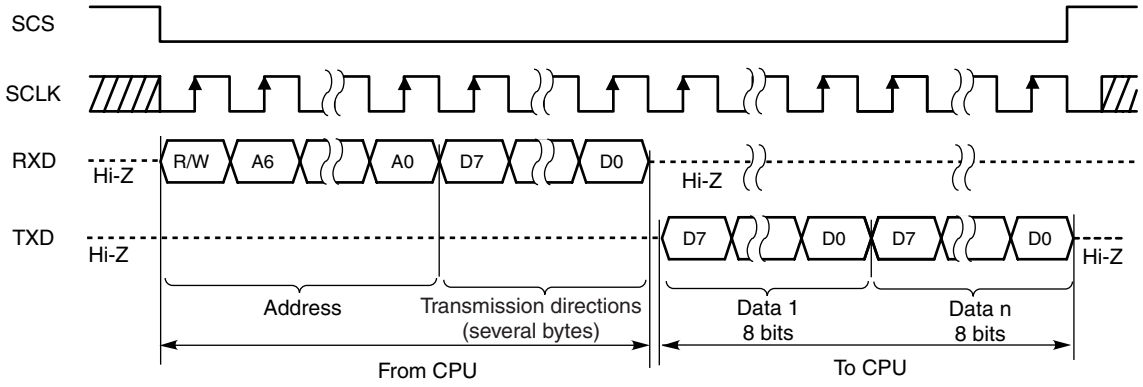
Remark The above formats are only used to access FIFOs in the sound generator block access.

Figure 3-13. Format of Host CPU Access - Continuous Access (3)
for Firmware Download, HIO Access, and AST RAM Access

(a) Write access



(b) Read access



Remark The above formats are only used for access Firmware download, HIO access, and AST RAM access.

3.2.3 Initialization signal for serial I/F

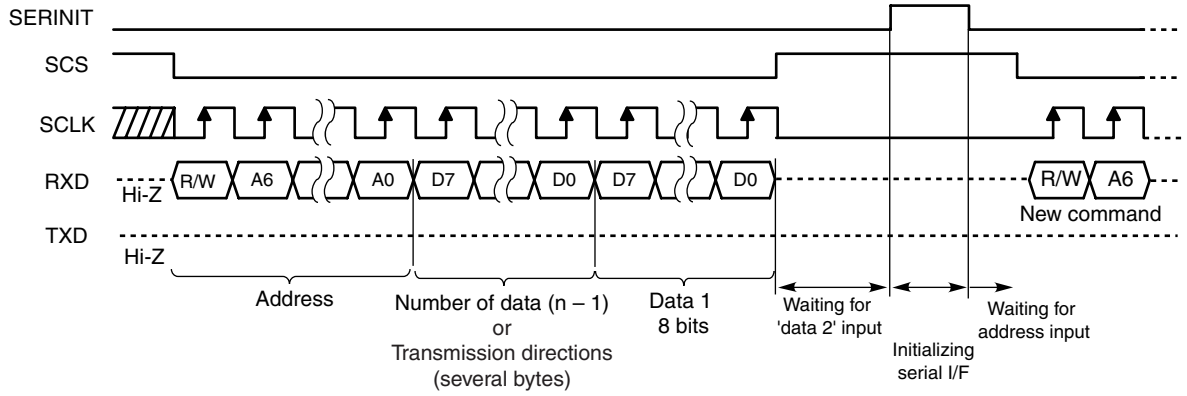
The SERINIT (D0) pin is an initialization signal for the serial I/F and is used for compulsory initialization of the serial I/F during write/read continuous access. (Therefore, this pin is normally used at low level if compulsory initialization is unnecessary.)

The compulsory initialization operates only the serial I/F and is asynchronously performed by SCS = 1 and SERINIT = 0. On the other hand the registers in the sound generator and chip control are not initialized. Therefore the serial I/F waits for a new address to be input after initialization.

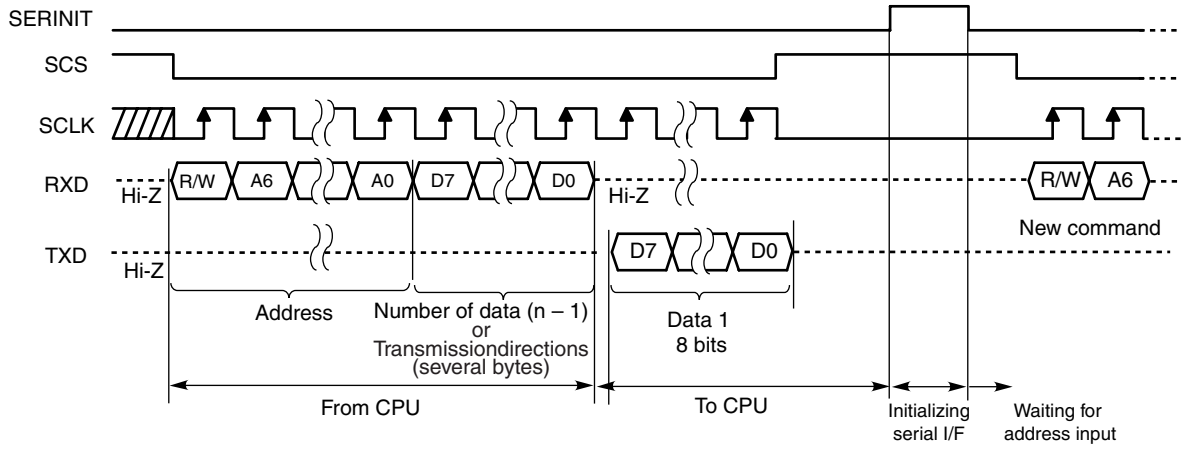
An example of this initialization signal is shown below.

Figure 3-14. Canceling Continuous Access Using SERINIT (D0) Pin

(a) Write access



(b) Read access



Remark The initialization conditions in 3/4-wire mode are the same.

4. AUDIO SERIAL INTERFACE

When LRCLK = 0 in the SLASI register (08H), L-ch data is assigned during the high-level period of LRCLK and R-ch data is assigned during the low-level period of LRCLK. For IIS format, this is reversed, in which case LRCLK = 1 should be set.

Within each of these periods, the format can be switched among right-justified, left-justified, and IIS format. Selection of master mode or slave mode is also enabled. The number of data bits per frame can be set via the BFS[4:0] bits in the SFSL register (07H). The serial input/output timing is shown in Figures 4-1 to 4-3.

Figure 4-1. Right-Justified Format

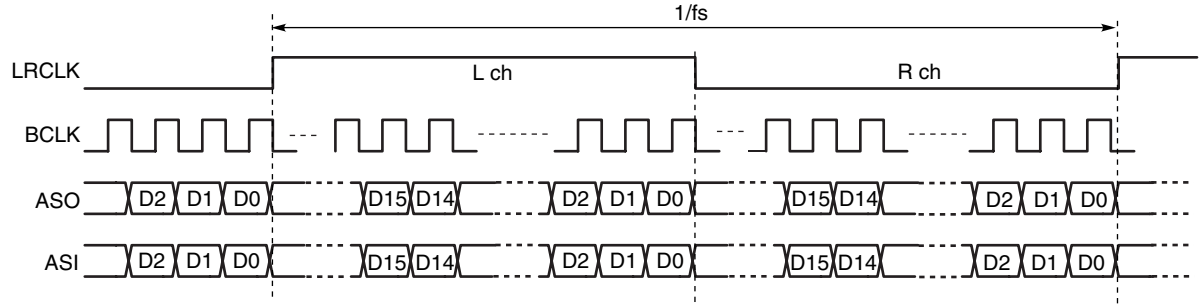


Figure 4-2. Left-Justified Format

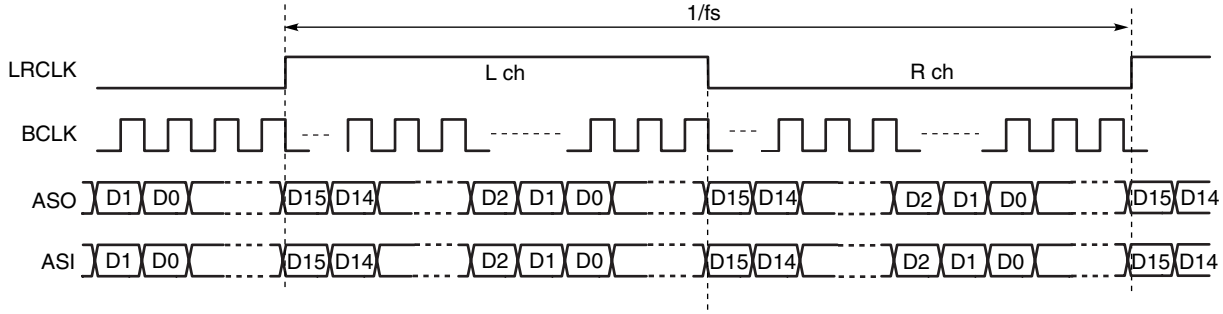
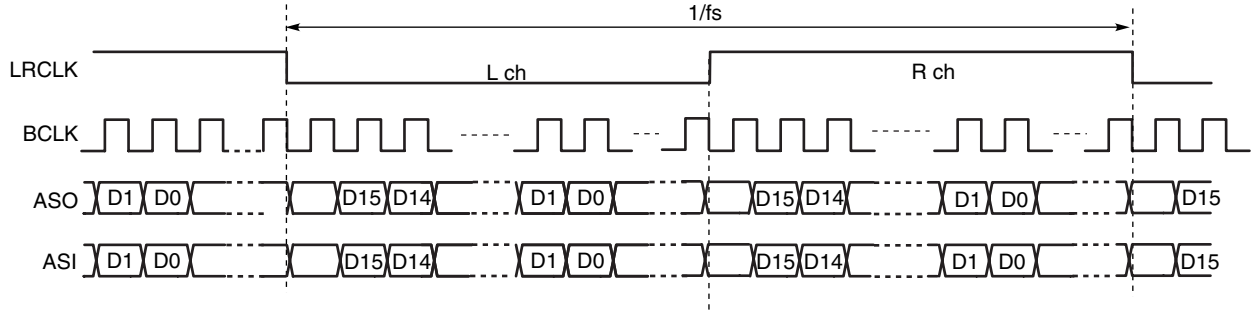


Figure 4-3. IIS Format



Remarks 1. The IIS format is left-justified with one empty bit and sets L-ch to low level and R-ch to high level. Do not specify other settings when selecting IIS mode (ASIM = 1 in SLASI register (08H)). When selecting LR mode (ASIM = 0 in SLASI register (08H)), left or right justification can be selected in combination with normal or reversed left-right format.

2. The number of data bits per frame can be set via the BFS[4:0] bits in the SFSL register (07H).
In master mode, either 64 bits or 32 bits can be selected. In slave mode, any value between 32 bits and 64 bits can be selected in two-bit increments.
After a reset is cleared, the default frame configuration setting is 64 bits in total (32 bits for L-ch and 32 bits for R-ch).

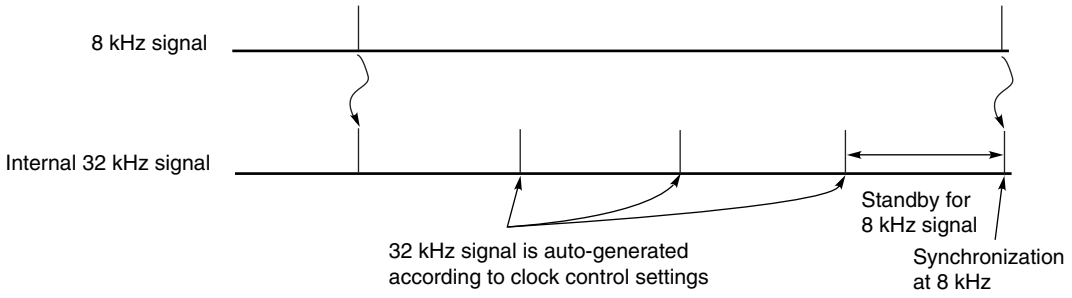
5. ADPCM INPUT INTERFACE

5.1 CLK8K

This is the input pin for the clock signal used for external 8 kHz synchronization when ADPCM recording. During playback, this clock signal is generated based on a 32 kHz signal generated in the μPD9993, and during recording this signal is generated based on an 8 kHz clock signal input from an external source.

Caution If an 8 kHz synchronization clock signal is not being input from an external source during recording, the recorded data cannot be saved.

Figure 5-1. Synchronization During ADPCM Recording



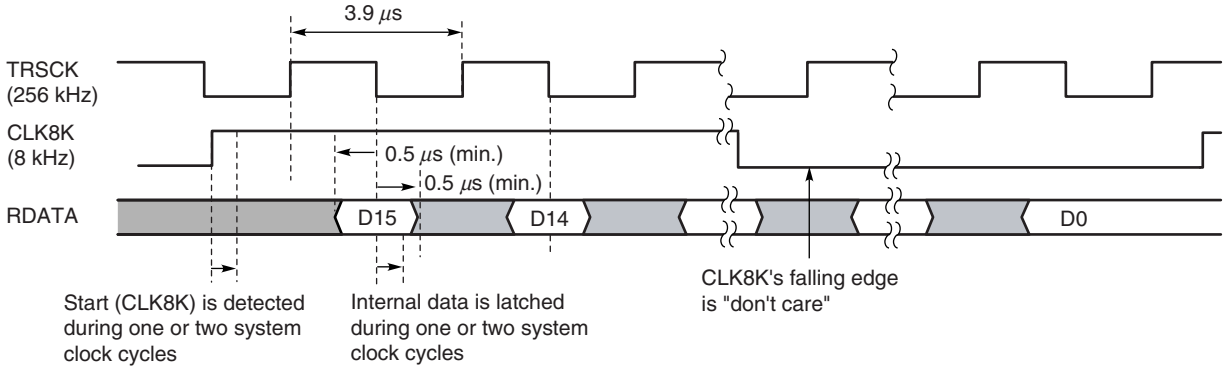
5.2 TRSCK and RDATA

The ADPCM input interface is an external synchronous serial interface used for input and output of linear PCM data or μ-law PCM data.

5.2.1 Serial recording interface

The timing of the external synchronous serial interface is shown below.

Figure 5-2. Timing of External Synchronous Serial Interface



Transfer of ADPCM recorded data is performed in synchronization with an external 8 kHz sync signal and an external serial clock. Latching of data is performed at the falling edge of the serial clock and data is latched MSB first in 16-bit segments. In the case of 16-bit linear PCM data (two's complement format), all 16 bits are valid, but in the case of μ-law 8-bit PCM data, the higher 8 bits are ignored and only the lower 8 bits contain valid data.

Caution Input to the CLK8K pin is detected only at the rising edge.

6. MP3/AAC DECODER

Only the MP3/AAC decoder or PCM sound generator (MIDI/ADPCM) can be selected. Therefore both cannot operate at the same time.

Selection of the MP3/AAC decoder and PCM sound generator is performed by setting a command register.

6.1 Interface

The μPD9993 can use the host CPU interface (parallel) or the SPI interface (serial) to send firmware and data streams. Interface selection is performed by using the PS pin, which is a mode setting pin for setting the parallel and serial interfaces (See **1. PIN FUNCTIONS** for details).

6.2 Firmware

The μPD9993 has a digital signal processor (DSP) for decoding MP3/AAC data streams. The DSP needs a firmware for decoding. Decoding is performed by downloading either the MP3 or AAC firmware from the external memory.

6.2.1 Procedure for downloading firmware for MP3/AAC decoder

This section indicates the procedure for downloading the MP3/AAC decoder's firmware.

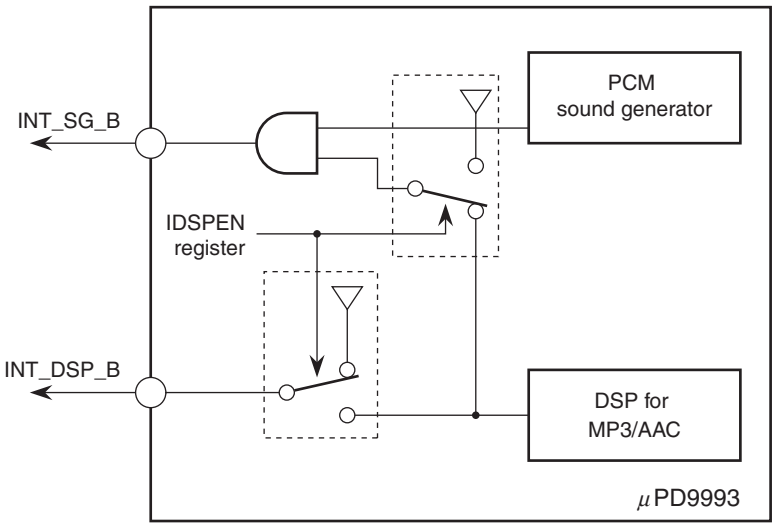
6.3 Interrupts

The μPD9993 has two interrupt signal pins (INT_SG_B and INT_DSP_B). INT_SG_B is an interrupt signal from the PCM sound generator and INT_DSP_B is an interrupt signal from the DSP (MP3/AAC decoder).

The PCM sound generator and the DSP for the MP3 or AAC decoder do not operate at the same time. Therefore only one interrupt signal pin can be used at time.

In this case, INT_SG_B can be used as the interrupt signal from both PCM sound generator and DSP (MP3/AAC decoder), and the INT_DSP_B is left open. This control is performed by command registers.

Figure 6-1. Interrupt signal pins (INT_SG_B, INT_DSP_B)



7. REGISTERS

The μPD9993 has three register areas as follows.

- Registers for PCM sound generator
- Registers for chip control
- Registers for DSP (MP3/AAC decoder)

The registers for chip control and the DSP are described below.

Caution Information on sound generator (SG) registers will be disclosed only to parties that have signed an NDA (non disclosure agreement).

7.1 Parallel I/F Mode

In parallel I/F mode, the register area is switched by the combination of the A1 and A2 pins.

- A1 = 0 and A2 = 0 : Chip control register
- A1 = 0 and A2 = 1 : DSP for MP3/AAC decoder
- A1 = 1 and A2 = 0 : PCM sound generator

Remark A1 = 1 and A2 = 1 : Prohibited

The register map when the PS pin is low level is as follows.

7.1.1 Register map for chip control

Table 7-1. List of Control Registers (1/2)

Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Control Description	Register Name
00H	W/R	STDIG	STPLL2	STPLL1	STASI	STASO	STSYNTH	STDAC	STDSP	00H	LSI standby setting	STNBY
01H	W/R	MCLK1A[7:0]								40H	Master clock setting 1	MCLK1A
02H	W/R	MCLK1B[7:0]								79H	Master clock setting 1	MCLK1B
03H	W/R	0	0	0	MCLK2A[4:0]					05H	Master clock setting 2	MCLK2A
04H	W/R	MCLK2B[7:0]								3FH	Master clock setting 2	MCLK2B
05H	W/R	0	0	0	MIX	0	0	SLSORCE[1:0]		00H	Source selection and mixing settings	SLSORCE
06H	W/R	0	0	0	DVXSL	0	0	ENSRD[1:0]		00H	Surround control	ENSRD
07H	W/R	BFS[4:0]					FS[2:0]			00H	Sampling frequency setting and ASIO BCLK setting	SLFS
08H	W/R	0	0	0	0	SLR	MS	ASIM	LRCLK	00H	ASI format setting	SLASI
09H	W/R	0	0	0	DAULGA[4:0]					02H	Digital volume (L)	DAULGA
0AH	W/R	0	0	0	DAURGA[4:0]					02H	Digital volume (R)	DAURGA
0BH	W/R	0	0	0	AAULGA[4:0]					1FH	Analog volume (L)	AAULGA
0CH	W/R	0	0	0	AAURGA[4:0]					1FH	Analog volume (R)	AAURGA
0DH	W/R	0	0	0	0	0	0	VIB	LED	00H	LED, VIB port output setting	VIB
0EH	W/R	0	0	0	0	POUT3	POUT2	POUT1	POUT0	00H	General-purpose port output setting	POUT
0FH	W/R	0	0	0	0	0	0	SVOL[1:0]		00H	Digital Soft Volume setting	SVOL

Remark Don't access an unspecified address (address area is from 00H to 7FH).

Table 7-1. List of Control Registers (2/2)

Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Control Description	Register Name
10H	W/R	0	0	0	0	0	0	MONO[1:0]		00H	Mono setting	MONO
2FH	R	0	0	0	0	0	0	IDSP	ISG	00H	INT source	INTSRC
3FH	R	PVER[3:0]				MVER[3:0]				3×H[Note]	Product discernment and LSI version	VER
50H	W/R	SRDCOF[7:0]								Undefined	Surround coefficient	SRDCOF
59H	W	GSRDW[7:0]								Undefined	Surround coefficient G1	GSRDW
5BH	W	DLSRDW[7:0]								Undefined	Surround coefficient D1	DLSRDW
64H	R	GSRDR[7:0]								30H	Surround coefficient G1	GSRDR
66H	R	DLSRDR[7:0]								20H	Surround coefficient D1	DLSRDR

Note Differs according to the LSI version for MVER[3:0]. PVER[3:0] is fixed to 3H.

Remarks 1. Don't access an unspecified address (address area is from 00H to 7FH).

2. The interrupt source register (2FH) exists in all register areas.

7.1.2 Register map for DSP (MP3/AAC decoder)

Table 7-2. List of Control Registers

Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Control Description	Register Name
00H	W/R	0	0	0	0	0	0	0	HRST	00H	DSP command reset	HRST
02H	W/R	0	0	0	0	0	0	0	HIORSTB	01H	HIO reset	HIORSTB
04H	W/R	0	0	0	0	0	0	0	DRSTB	01H	DSP latch reset	DRSTB
10H	W/R	0	0	0	0	0	0	0	CLKE	00H	DSP clock enable	CLKE
20H	W/R	0	0	0	0	0	0	0	MWDNEN	00H	Firmware download enable	MWDNEN
22H	W/R	Extended register for Firmware stream download								00H	Firmware stream download	MWDN
2FH	R	0	0	0	0	0	0	IDSP	ISG	00H	INT source	INTSRC
30H	R	0	0	0	0	0	0	ISMLD	ISRES	00H	INT factor for DSP	INTFC
32H	W/R	0	0	0	0	0	0	IMLD	IMRES	00H	Mask of INT factor for DSP	IMASK
40H	W/R	Extended register for HIO access								00H	HIO access register	
42H	R	0	0	HRER	HWER	HSER	HLER	HREF	HWEF	01H	HIO status register	HST1
50H	W/R	0	0	0	0	0	0	0	WUP	00H	Wakeup control	WUP
60H	W/R	0	0	0	0	0	0	0	LRMASK	00H	Mask of INT request for PCM	LRMASK
70H	W/R	0	0	0	0	0	0	0	IDSPEN	00H	INT_DSP_B enable	IDSPEN

Remarks 1. Don't access an unspecified address (address area is from 00H to 7FH).

2. The interrupt source register (2FH) exists in all register areas.

7.2 Serial I/F Mode

In serial I/F mode, the register area is switched by the bank register setting (address 4FH).

- BANK = 00B: PCM sound generator register bank
- BANK = 01B: Chip control register bank
- BANK = 10B: DSP register bank

The register map for chip control is performed when the PS pin is high level is as follows.

7.2.1 Sound generator bank

This register map applies when the bank register is 00H.

Table 7-3. List of Sound Generator Bank Registers

Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Control Description	Register Name
00H : 2EH	Registers for sound generator											
2FH	R	0	0	0	0	0	0	IDSP	ISG	00H	INT source	INTSRC
30H : 4E	Registers for sound generator											
4FH	W/R	0	0	0	0	0	0	BANK[1:0]		01H	BANK register	BANK
50H : 7FH	Registers for sound generator											

Remark The bank register (4FH) and interrupt source register (2FH) exist in all bank areas.

7.2.2 Chip control bank

The register map applies when the bank register is 01H.

Table 7-4. List of Chip Control Bank Registers (1/2)

Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Control Description	Register Name
00H	W/R	STDIG	STPLL2	STPLL1	STASI	STASO	STSYNTH	STDAC	STDSP	00H	LSI standby setting	STNBY
01H	W/R	MCLK1A[7:0]								40H	Master clock setting 1	MCLK1A
02H	W/R	MCLK1B[7:0]								79H	Master clock setting 1	MCLK1B
03H	W/R	0	0	0	MCLK2A[4:0]					05H	Master clock setting 2	MCLK2A
04H	W/R	MCLK2B[7:0]								3FH	Master clock setting 2	MCLK2B
05H	W/R	0	0	0	MIX	0	0	SLSORCE[1:0]		00H	Source selection and mixing settings	SLSORCE
06H	W/R	0	0	0	DVXSL	0	0	ENSRD[1:0]		00H	Surround control	ENSRD
07H	W/R	BFS[4:0]					FS[2:0]			00H	Sampling frequency setting and ASIO BCLK setting	SLFS
08H	W/R	0	0	0	0	SLR	MS	ASIM	LRCLK	00H	ASI format setting	SLASI
09H	W/R	0	0	0	DAULGA[4:0]					02H	Digital volume (L)	DAULGA
0AH	W/R	0	0	0	DAURGA[4:0]					02H	Digital volume (R)	DAURGA
0BH	W/R	0	0	0	AAULGA[4:0]					1FH	Analog volume (L)	AAULGA
0CH	W/R	0	0	0	AAURGA[4:0]					1FH	Analog volume (R)	AAURGA
0DH	W/R	0	0	0	0	0	0	VIB	LED	00H	LED, VIB port output setting	VIB
0EH	W/R	0	0	0	0	POUT3	POUT2	POUT1	POUT0	00H	General-purpose port output setting	POUT
0FH	W/R	0	0	0	0	0	0	SVOL[1:0]		00H	Digital soft volume setting	SVOL
10H	W/R	0	0	0	0	0	0	MONO[1:0]		00H	Mono setting	MONO
2FH	R	0	0	0	0	0	0	IDSP	ISG	00H	INT source	INTSRC
3FH	R	PVER[3:0]				MVER[3:0]				3×H[Note]	Product discernment and LSI version	VER
4FH	W/R	0	0	0	0	0	0	BANK[1:0]		01H	Bank register	BANK
50H	R/W	SRDCOF[7:0]								Undefined	Surround coefficient	SRDCOF
59H	W	GSRDW[7:0]								Undefined	Surround coefficient G1	GSRDW
5BH	W	DLSRDW[7:0]								Undefined	Surround coefficient D1	DLSRDW
64H	R	GSRDR[7:0]								30H	Surround coefficient G1	GSRDR
66H	R	DLSRDR[7:0]								20H	Surround coefficient D1	DLSRDR

Note Differs according to the LSI version for MVER[3:0]. PVER[3:0] is fixed to 3H.

Remarks 1. Don't access an unspecified address (address area is from 00H to 7FH).

2. The bank register (4FH) and interrupt source register (2FH) exist in all bank areas.

7.2.3 DSP bank

This register map applies when the bank register is 02H.

Table 7-5. List of DSP Bank Registers

Address	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Control Description	Register Name
00H	W/R	0	0	0	0	0	0	0	HRST	00H	DSP command reset	HRST
02H	W/R	0	0	0	0	0	0	0	HIORSTB	01H	HIO reset	HIORSTB
04H	W/R	0	0	0	0	0	0	0	DRSTB	01H	DSP latch reset	DRSTB
10H	W/R	0	0	0	0	0	0	0	CLKE	00H	DSP clock enable	CLKE
20H	W/R	0	0	0	0	0	0	0	MWDNEN	00H	Firmware Download Enable	MWDNEN
22H	W/R	Extended register for Firmware stream download								00H	Firmware stream download	MWDN
2FH	R	0	0	0	0	0	0	IDSP	ISG	00H	INT source	INTSRC
30H	R	0	0	0	0	0	0	ISMLD	ISRES	00H	INT factor for DSP	INTFC
32H	W/R	0	0	0	0		0	IMLD	IMRES	00H	Mask of INT factor for DSP	IMASK
40H	W/R	Extended register for HIO access								00H	HIO access register	HIO
42H	R	0	0	HRER	HWER	HSER	HLER	HREF	HWEF	01H	HIO status register	HST1
4FH	W/R	0	0	0	0	0	0	BANK		01H	Bank register	BANK
50H	W/R	0	0	0	0	0	0	0	WUP	00H	Wakeup control	WUP
60H	W/R	0	0	0	0	0	0	0	LRMASK	00H	Mask of INT request for PCM	LRMASK
70H	W/R	0	0	0	0	0	0	0	IDSPEN	00H	INT_DSP_B enable	IDSPEN

Remarks 1. Don't access an unspecified address (address area is from 00H to 7FH).

2. The bank register (4FH) and interrupt source register (2FH) exist in all bank areas.

7.3 Detailed Description of DSP (DSP Bank) Registers

7.3.1 Command reset of DSP (HRST)

This register performs command reset for only the DSP.

Address: 00H, register name: HRST, block: DSP, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	HRST

(1) HRST

Data	Mode	Initial Value	Description
0	Reset	0	Reset
1	Active		Normal operation

Remark This register is initialized by the RESET_B pin.

7.3.2 Command reset of HIO (HIORSTB)

This register performs command reset for only the internal DSP interface (HIO).

Address: 02H, register name: HIORSTB, block: DSP, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0		HIORSTB

(1) HIORSTB

Data	Mode	Initial Value	Description
0	Reset	1	Reset
1	Active		Normal operation

7.3.3 Command reset of DSP latch (DRSTB)

This register performs command reset for only the internal DSP output block.

Address: 04H, register name: DRSTB, block: DSP, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	DRSTB

(1) DRSTB

Data	Mode	Initial Value	Description
0	Reset	1	Reset
1	Active		Normal operation

7.3.4 Clock signal control register for DSP block (CLKE)

This register controls the clock signal for the DSP block.

Address: 10H, register name: CLKE, block: DSP, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	CLKE

(1) CLKE

Data	Mode	Initial Value	Description
0	Stop (Disable)	0	CLOCK for DSP is not supplied.
1	Active (Enable)		Normal operation

7.3.5 Firmware download enable register (MWDNEN)

This register enables firmware downloading.

Address: 20H, register name: MWDNEN, block: DSP, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	MWDNEN

(1) MWDNEN

Data	Mode	Initial Value	Description
0	Disable	0	Disables firmware downloading. (Write protect)
1	Enable		Enables firmware downloading.

7.3.6 INT source register (INTSRC)

This register distinguishes the interrupt source between the PCM sound generator and DSP (MP3/AAC decoder).

Address: 2FH, register name: INTSRC, block: other, access: R

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	IDSP	ISG

(1) IDSP/ISG

Data	Mode	Initial Value	Description
ISG	S.G.	0	Interrupt of PCM sound generator.
IDSP	DSP	0	Interrupt of DSP (MP3/AAC decoder).

7.3.7 INT factor for DSP (INTFC)

This register is used to read interrupt factors.

Address: 30H, register name: INTFC, block: DSP, access: R

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	ISMLD	ISRES

(1) ISMLD

Data	Mode	Initial Value	Description
0		0	–
1			Firmware download or stream download completed.

Remark This factor is initialized by reading from the host CPU.

(2) ISRES

Data	Mode	Initial Value	Description
0		0	–
1			Exists a response from DSP

Remark This factor is initialized by reading from the host CPU.

7.3.8 Mask of INT factor for DSP (IMASK)

This register masks interrupt factors.

Address: 32H, register name: IMASK, block: DSP, access: R/W

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	IMLD	IMRES

(1) IMLD

Data	Mode	Initial Value	Description
0	Mask	0	INT factor from DSP masked
1	No mask		No mask.

(2) IMRES

Data	Mode	Initial Value	Description
0	Mask	0	Response from DSP masked
1	No mask		No mask.

7.3.9 HIO status register (HIO1)

This is the status register for the internal DSP interface (HIO).

Address: 42H, register name: HIO1, block: DSP, access: R/W

D7	D6	D5	D4	D3	D2	D1	D0
0	0	HRER	HWER	HSER	HLER	HREF	HWEF

(1) HRER (Error flag of host read)

Data	Mode	Initial Value	Description
0		0	–
1	Error occurred		A host read error occurred.

Caution This register is set to "1" when the host CPU reads HDT and HREF = 0.
Once it is set to "1", this register will not change until the DSP writes "0" to it.

(2) HWER (Error flag of host write)

Data	Mode	Initial Value	Description
0		0	–
1	Error occurred		A host write error occurred.

Caution This register is set to "1" when the host CPU writes to HDT and HWEF = 0.
Once it is set to "1", this register will not change until the DSP writes "0" to it.

(3) HSER (Error flag of HDT store)

Data	Mode	Initial Value	Description
0		0	–
1	Error occurred		An HDT store error occurred

Caution This register is set to "1" when the DSP stores data in HDT and HREF = 1.
Once it is set to "1", this register will not change until the DSP writes "0" to it.

(4) HLER (Error flag of HDT load)

Data	Mode	Initial Value	Description
0		0	–
1			An HDT load error occurred

Caution This register is set to "1" when the DSP loads data from HDT and HWEF = 1.
Once it is set to "1", this register will not change until the DSP writes "0" to it.

(5) HREF (Enabling flag of Host read)

Data	Mode	Initial Value	Description
0	Disable	0	Disables reading from host CPU.
1	Enable		Enables reading from host CPU.

Caution This register is set to "1" when the DSP stores data in HDT.

(6) HWEF (Enabling flag of Host write)

Data	Mode	Initial Value	Description
0	Disable	1	Disables write from Host CPU.
1	Enable		Enables write from Host CPU.

Caution This register is set to "1" when the DSP loads data from HDT.

7.3.10 Wakeup control (WUP)

This register controls to wakeup of the DSP block.

Address: 50H, register name: WUP, block: DSP, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	WUP

(1) WUP

Data	Mode	Initial Value	Description
0	No operation	0	Negate DSP wakeup signal.
1	Active		Activate DSP wakeup signal.

Caution To wakeup DSP, write "1" to this register first, then rewrite "0" to this register.

7.3.11 Mask of PCM INT factor (LRMASK)

This register is used to mask interrupt factors.

Address: 60H, register name: LRMASK, block: DSP, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	LRMASK

(1) LRMASK

Data	Mode	Initial Value	Description
0	Mask	0	PCM INT request for internal DSP output block masked.
1	No mask		No mask

Caution LRMASK must be set to "1" in the mixing mode (MIX register of chip control bank is set to "1").

7.3.12 INT_DSP_B enable (IDSPEN)

This register enables the INT_DSP_B pin.

Address: 70H, register name: IDSPEN, block: DSP, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	IDSPEN

(1) IDSPEN

Data	Mode	Initial Value	Description
0	Disable	0	High-level output. Interrupts of DSP are output from INT_SG_B pin.
1	Enable		Enables the output of interrupt signal from DSP.

7.3.13 Bank register (BANK)

This register is used to switch the sound generator register bank, chip control register bank, and DSP register bank in serial I/F mode.

This register is available in serial I/F mode only (it is only valid when PS = 1).

Address: 4FH, register name: BANK, CPU interface, access: R/W, initial value: 01H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	BANK	

(1) BANK

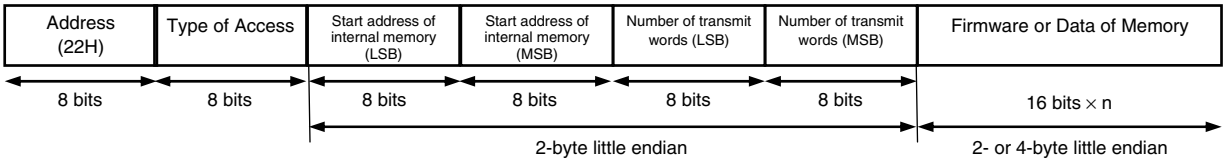
Data	Mode	Initial Value	Description
BANK		01H	Bank register for switching among sound generator register bank, DSP register bank, and chip control register bank.

When BANK = 00B, the sound generator register bank is selected.
When BANK = 01B, the chip control register bank is selected.
When BANK = 10B, the DSP register bank is selected.

Bank register can be accessed from all register banks.

7.3.14 Extended register for firmware stream download (address 22H)

This address is used to download firmware and data streams.



(1) Address

Address 22H of the DSP registers (BANK) is specified in this area.

In serial I/F mode (PS = 1), the R/W control signal is as the MSB bit ("1": Write, "0": Read).

(2) Type of access

The contents specified in this area are as follows.

D7	D6	D5	D4	D3	D2	D1	D0
R/W	Type of access	Undefined			Direction		

Bit	Function	Description
7	R/W	0: Read mode 1: Write mode
6	Type of access	0: Single access 1: Incremental access
5 to 3	Undefined	
2 to 0	Direction	000: Selection of reset control address 001: Selection of IMEM area 010: Selection of XMEM area 011: Selection of YMEM area 1xx: Selection of DSP stream buffer

(3) Start address of internal memory

The start address of the internal memory is specified in this area. Read and write access is started from this address.

(4) Number of transmit words

The number of transmit words is specified in this area when incremental access is specified in "(2) Type of access" (D6 = 1). In the case of single access, this area must be set to 0000H.

In this area, 1 word is defined as 16 bits. Therefore,

IMEM: 2 words (32 bits)

XMEM: 1 word (16 bits)

YMEM: 1 word (16 bits)

For example, when the number of transmit data words is 1024, the setting value of this area must be 0400H.

(5) Firmware or Data of memory

In the case of write access, this area defines the firmware for writing to memory.

IMEM: 1 word = 4 bytes (little endian)

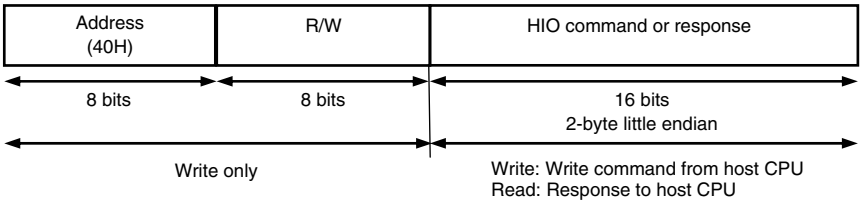
XMEM: 1 word = 2 bytes (little endian)

YMEM: 1 word = 2 bytes (little endian)

In the case of read access, the transmit data of the internal DSP memory is defined in this area.

7.3.15 Extended register for HIO access (address 40H)

This address is for access of the internal DSP interface (HIO).



(1) Address

Address 40H of the DSP registers (BANK) is specified in this area.

In serial I/F mode (PS = 1), the R/W control signal is specified as the MSB bit. ("1": Write, "0": Read)

(2) R/W

The contents allocated to this area are as follows.

D7	D6	D5	D4	D3	D2	D1	D0
Undefined							R/W

Bit	Function	Description
7 to 1	Undefined	
0	R/W	0: Read response 1: Write command

(3) HIO command or response area

The HIO command or response area is specified in this area.

Write access: Command from host CPU to DSP (2 bytes, little endian)

Read access: Response from the DSP (2 bytes, little endian)

7.4 Description of Chip Control (Chip Control Bank) Registers

7.4.1 Standby setting (STNBY)

This register sets standby mode.

Address: 00H, register name: STNBY, block: General, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
STDIG	STPLL2	STPLL1	STASI	STASO	STSYNTH	STDAC	STDSP

(1) STDIG

Data	Mode	Initial Value	Description
0	Standby	0	Standby for digital block except command registers
1	ON		Normal operation

Remark The digital blocks except command registers, sound generator, and DSP (MP3/AAC decode) will be initialized and will stop internal clocks when this register is set to "0". Initialization of the command registers is performed by the RESET_B pin and initialization of sound generator and DSP is performed by command of each register bank.

(2) STPLL2

Data	Mode	Initial Value	Description
0	Standby	0	Standby for PLL2
1	ON		Normal operation

Remark During PLL2 standby mode (power down), the PLL2 output clock is stopped.

(3) STPLL1

Data	Mode	Initial Value	Description
0	Standby	0	Standby for PLL1
1	ON		Normal operation

Remark In PLL1 standby mode (power down), the PLL1 output clock is stopped.

(4) STASI

Data	Mode	Initial Value	Description
0	Standby	0	Standby for audio serial interface input (ASI)
1	ON		Normal operation

(5) STASO

Data	Mode	Initial Value	Description
0	Standby	0	Standby for audio serial interface output (ASO)
1	ON		Normal operation

Caution The LRCLK pin and the BCLK pin are set to standby when both the STASI and the STASO bits are set to standby. For details, see Table 1-1. Pin Status in ASIO Block.

(6) STSYNTH

Data	Mode	Initial Value	Description
0	Standby	0	Standby for sound generator block (Synthesizer)
1	ON		Normal operation

Remark Internal clock for sound generator stops when this register is set to "0".

(7) STDAC

Data	Mode	Initial Value	Description
0	Standby	0	Standby for DAC block[Note]
1	ON		Normal operation

Note This standby signal is effective for the DAC analog block and the analog volume block.

(8) STDSP

Data	Mode	Initial Value	Description
0	Standby	0	Standby for DSP (MP3/AAC decoder) block
1	ON		Normal operation

Remark Internal clock for DSP (MP3/AAC decoder) stops when this register is set to "0".

7.4.2 Master clock setting (MCLK1A, MCLK1B, MCLK2A, MCLK2B)

These registers set frequencies of master clock 1 and master clock 2.

Address: 01H, register name: MCLK1A, block: PLL1, access: R/W, initial value: 40H

D7	D6	D5	D4	D3	D2	D1	D0
MCLK1A[7:0]							

Address: 02H, register name: MCLK1B, block: PLL1, access: R/W, initial value: 79H

D7	D6	D5	D4	D3	D2	D1	D0
MCLK1B[7:0]							

Address: 03H, register name: MCLK2A, block: PLL2, access: R/W, initial value: 05H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	MCLK2A[4:0]				

Address: 04H, register name: MCLK2B, block: PLL2, access: R/W, initial value: 3FH

D7	D6	D5	D4	D3	D2	D1	D0
MCLK2B[7:0]							

(1) MCLK1A [7:0]

Data	Mode	Initial Value	Description
MCLK1A[7:0]		40H	Sets PLL1, used to generate the audio master clock.

(2) MCLK1B [7:0]

Data	Mode	Initial Value	Description
MCLK1B[7:0]		79H	Sets PLL1, used to generate the audio master clock.

(3) MCLK2A [4:0]

Data	Mode	Initial Value	Description
MCLK2A[4:0]		05H	Sets PLL2, used to generate the sound generator and MP3/AAC master clock.

(4) MCLK2B [7:0]

Data	Mode	Initial Value	Description
MCLK2B[7:0]		3FH	Sets PLL2, used to generate the sound generator and MP3/AAC master clock.

Master clock setting examples are shown below.

(a) Audio master clock setting

The MCLK1A and the MCLK1B set the clock frequency supplied to all blocks except the sound generator and DSP block. Be sure to set the MCLK1A and MCLK1B registers according to the input clock frequency and sampling frequency. The input clock signal is first divided by the value in the MCLK1A register and is then multiplied by the value in the MCLK1B register.

CLKIN Input Frequency [MHz]	MCLK1A[6:0]		MCLK1B[7:0]		Sampling Frequency fs [kHz]
	Dec	HEX	Dec	HEX	
2.688	20	14	168	A8	44.1
5.376	40	28	168	A8	44.1
12.000	76	4C	143	8F	44.1
12.600	77	4D	138	8A	44.1
13.000 Note	76	4C	132	84	44.1
14.400	125	7D	196	C4	44.1
16.128	120	78	168	A8	44.1
26.000	152	98	132	84	44.1
2.688	14	0E	128	80	48.0
5.376	28	1C	128	80	48.0
12.000	62	3E	127	7F	48.0
12.600	81	51	158	9E	48.0
13.000 Note	64	40	121	79	48.0
14.400	75	4B	128	80	48.0
16.128	84	54	128	80	48.0
26.000	128	80	121	79	48.0
2.688	14	0E	128	80	32.0
5.376	28	1C	128	80	32.0
12.000	62	3E	127	7F	32.0
12.600	81	51	158	9E	32.0
13.000 Note	64	40	121	79	32.0
14.400	75	4B	128	80	32.0
16.128	84	54	128	80	32.0
26.000	128	80	121	79	32.0
2.688	14	0E	128	80	8.0
5.376	28	1C	128	80	8.0
12.000	62	3E	127	7F	8.0
12.600	81	51	158	9E	8.0
13.000 Note	64	40	121	79	8.0
14.400	75	4B	128	80	8.0
16.128	84	54	128	80	8.0
26.000	128	80	121	79	8.0
2.688	14	0E	128	80	16.0
5.376	28	1C	128	80	16.0
12.000	62	3E	127	7F	16.0
12.600	81	51	158	9E	16.0
13.000 Note	64	40	121	79	16.0
14.400	75	4B	128	80	16.0
16.128	84	54	128	80	16.0
26.000	128	80	121	79	16.0

Note Default setting

(b) Sound generator & MP3/AAC decoder master clock setting

The MCLK2A and the MCLK2B set the frequencies of the clock to be supplied to the sound generator and DSP (MP3/AAC decoder) block. Be sure to set values in the MCLK2A and MCLK2B registers according to the input clock frequency. The input clock signal is first divided by the value set to the MCLK2A register and is then multiplied by the value set to the MCLK2B register.

CLKIN Input Frequency [MHz]	MCLK2A[4:0]		MCLK2B[7:0]		Sampling Frequency fs [kHz]	Master Clock Frequency for SG [MHz]	Master Clock Frequency for DSP [MHz]
	Dec	HEX	Dec	HEX			
2.688	1	01	62	3E	32.0	55.55200	83.32800
5.376	2	02	62	3E	32.0	55.55200	83.32800
12.000	5	05	69	45	32.0	55.20000	82.80000
12.600	5	05	66	42	32.0	55.44000	83.16000
13.000 Note	5	05	63	3F	32.0	54.60000	81.90000
14.400	6	06	69	45	32.0	55.20000	82.80000
16.128	6	06	62	3E	32.0	55.55200	83.32800
26.000	10	0A	63	3F	32.0	54.60000	81.90000

Note Default setting

7.4.3 Switching/mixing of surround block input source (SLSORCE)

This register selects the input of surround block. Mixing with sound generator or DSP (MP3/AAC decoder) and the audio serial interface is also possible.

Address: 05H, register name: SLSORCE, block: Selector, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	MIX	0	0	SLSORCE[1:0]	

(1) SLSORCE [1:0]

Data	Mode	Initial Value	Description
00B	SYNTH	00B	Select sound generator
01B	ASI		Select audio serial interface (ASI)
10B	DSP		Select DSP (MP3/AAC Decoder)
11B	-		Prohibited

Caution When ASI is selected by the SLSORCE register, the output signal is only the ASI signal. In this case, the MIX register setting is ignored.

(2) MIX

Data	Mode	Initial Value	Description
0	Path selection	0	Only one path is used. The path is selected by the SLSORCE register.
1	Mixing		The ASI signal is mixed with the S.G. or DSP signal.

Cautions 1. When ASI is selected by SLSORCE register, the output signal is only the ASI signal. In this case, the MIX register setting is ignored.

2. The mixing mode is supported only when ASIO and the sound generator, or ASIO and the DSP output have the same sampling frequency.
In the case of mixing ASI with the sound generator, the supported sampling frequency is only 32 kHz.
In case of mixing ASI with the DSP(MP3/AAC), both have to be set to the same sampling frequency. Moreover, the LRMASK register (mask of PCM INT factor for DSP existing DSP Bank) must be set to "1".

3. If the sum of the ASI signal and output signal of the sound generator or DSP exceeds the full scale, the output signal will be clipped.

4. When setting the MIX bit to 1 while ASIO is in slave mode (MS bit of SLASI register = 1 (08H)), be sure to set the STASI bit of the standby register (00H) to 1 and input BCLK and LRCLK.
When stopping the ASI input while MIX = 1, retain the settings of MS = 1, MIX = 1, and STASI = 1 or set MIX = 0 and SLSORCE = 00H or 10H.
See 10.4 Table 10-1. Relationship between Setting Modes and Internal Operations (Relationship with Synchronization Clock) for details.

7.4.4 Surround control (ENSRD)

This switches the surround function on and off.

Address: 06H, register name: ENSRD, block: AST, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	DVXSL	0	0	ENSRD[1:0]	

(1) ENSRD [1:0]

Data	Mode	Initial Value	Description
00B	OFF	00B	Surround processing is not performed. Reading or writing of the surround coefficient is enabled.
01B	SPK		The coefficients for speaker is used to perform surround processing.
10B	HP		The coefficients for headphone is used to perform surround processing.
11B	–		Setting prohibited

Caution Reading or writing the surround coefficient is enabled only when ENSRD [1:0] = 00B. In this case, set STPLL2 to "1" and wait 5 ms before reading or writing the coefficient.

(2) DVXSL

Data	Mode	Initial Value	Description
0	AST	0	Adaptive surround
1	DVX		DVX

Caution It is necessary to set exclusive coefficients for each function.

7.4.5 Sampling frequency setting for AST block, ASIO, DAC, and BCLK switching for ASIO (SLFS)

This sets the sampling rate of AST block, ASIO, and DAC. It also sets the frequency of BCLK.

Address: 07H, register name: SLFS, block: ASIO, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
BFS[4:0]					FS[2:0]		

(1) FS[2:0]

Data	Mode	Initial Value	Description
000B	32 kHz	000B	Sets AST, ASIO, and DAC sampling rate as 32 kHz.
001B	44.1 kHz		Sets AST, ASIO, and DAC sampling rate as 44.1 kHz.
010B	48 kHz		Sets AST, ASIO, and DAC sampling rate as 48 kHz.
100B	8 kHz		Sets AST, ASIO, and DAC sampling rate as 8 kHz.
101B	16 kHz		Sets AST, ASIO, and DAC sampling rate as 16 kHz.

Caution Be sure to set this in tandem with the master clock setting (set for each sampling frequency). Do not set any data that is not shown above.

(2) BFS[4:0]

Data	Mode	Initial Value	Description
00H	64 fs	00H	Sets 64 fs as BCLK frequency (can be set during master mode).
01H	62 fs		Sets 62 fs as BCLK frequency.
02H	60 fs		Sets 60 fs as BCLK frequency.
03H	58 fs		Sets 58 fs as BCLK frequency.
04H	56 fs		Sets 56 fs as BCLK frequency.
05H	54 fs		Sets 54 fs as BCLK frequency.
06H	52 fs		Sets 52 fs as BCLK frequency.
07H	50 fs		Sets 50 fs as BCLK frequency.
08H	48 fs		Sets 48 fs as BCLK frequency.
09H	46 fs		Sets 46 fs as BCLK frequency.
0AH	44 fs		Sets 44 fs as BCLK frequency.
0BH	42 fs		Sets 42 fs as BCLK frequency.
0CH	40 fs		Sets 40 fs as BCLK frequency.
0DH	38 fs		Sets 38 fs as BCLK frequency.
0EH	36 fs		Sets 36 fs as BCLK frequency.
0FH	34 fs		Sets 34 fs as BCLK frequency.
10H	32 fs		Sets 32 fs as BCLK frequency (can be set during master mode).

Caution In master mode (MS = 1), only 64 fs (00H) or 32 fs (10H) can be set. If any other value is set, 64 fs (the initial value) will be selected.

In slave mode (MS = 0), any sampling frequency from 32 fs to 64 fs can be set in 2 fs increments.

7.4.6 ASIO mode setting (SLASI)

This specifies the ASIO setting as shown below.

Address: 08H, register name: SLASI, block: ASIO, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	SLR	MS	ASIM	LRCLK

(1) SLR

Data	Mode	Initial Value	Description
0	SR	0	Right-justified format
1	SL		Left-justified format

(2) MS

Data	Mode	Initial Value	Description
0	SLAVE	0	Slave mode
1	MASTER		Master mode

Caution In slave mode, external clock input is required. For a description of the pin status of the ASIO block during various modes, see 1.5 Pin Status.

(3) ASIM

Data	Mode	Initial Value	Description
0	LR	0	LR mode
1	IIS		IIS mode (In this case, the SLR bit is a “don’t care” bit).

(4) LRCLK

Data	Mode	Initial Value	Description
0	LCH	0	When LRCLK is at high level, this specifies L channel data.
1	RCH		When LRCLK is at high level, this specifies R channel data.

Caution Be sure to set LRCLK = 1 when IIS mode is selected.

7.4.7 Digital volume (L) setting (DAULGA)

This sets the L channel digital gain.

Address: 09H, register name: DAULGA, block: Digital Volume, access: R/W, initial value: 02H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	DAULGA[4:0]				

(1) DAULGA[4:0]

Data	Mode	Initial Value	Description
DAULGA[4:0]		02H	Sets digital gain (L-ch)

7.4.8 Digital volume (R) Setting (DAURGA)

This sets the R channel digital gain.

Address: 0AH, register name: DAURGA, block: Digital Volume, access: R/W, initial value: 02H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	DAURGA[4:0]				

(1) DAURGA[4:0]

Data	Mode	Initial Value	Description
DAURGA[4:0]		02H	Sets digital gain (R-ch)

Table 7-6. Digital Volume (5-Bit Non-Linear)

Gain	DAULGA[4:0]/ DAURGA[4:0]
+12 dB	00H
+6 dB	01H
±0 dB	02H (Initial value)
–3 dB	03H
–6 dB	04H
–9 dB	05H
–12 dB	06H
–15 dB	07H
–18 dB	08H
–21 dB	09H
–24 dB	0AH
–27 dB	0BH

Gain	DAULGA[4:0]/ DAURGA[4:0]
–30 dB	0CH
–33 dB	0DH
–36 dB	0EH
–39 dB	0FH
–42 dB	10H
–45 dB	11H
–48 dB	12H
–51 dB	13H
–54 dB	14H
–57 dB	15H
–60 dB	16H
Mute	17H

7.4.9 Analog volume (L-ch) Setting (AAULGA)

This sets the L channel analog gain.

Address: 0BH, register name: AAULGA, block: Analog Volume, access: R/W, initial value: 1FH

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	AAULGA[4:0]				

(1) AAULGA[4:0]

Data	Mode	Initial Value	Description
AAULGA[4:0]		1FH	Sets analog gain (L-ch)

7.4.10 Analog volume (R-ch) setting (AAURGA)

This sets the R channel analog gain.

Address: 0CH, register name: AAURGA, block: Analog Volume, access: R/W, initial value: 1FH

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	AAURGA[4:0]				

(1) AAURGA[4:0]

Data	Mode	Initial Value	Description
AAURGA[4:0]		1FH	Sets analog gain (R-ch)

Table 7-7. Analog Volume (5-Bit Linear)

Gain	AAULGA[4:0] / AAURGA[4:0]
±0 dB	00H
–1.5 dB	01H
–3 dB	02H
–4.5 dB	03H
–6 dB	04H
–7.5 dB	05H
–9 dB	06H
–10.5 dB	07H
–12 dB	08H
–13.5 dB	09H
–15 dB	0AH
–16.5 dB	0BH
–18 dB	0CH
–19.5 dB	0DH
–21 dB	0EH
–22.5 dB	0FH

Gain	AAULGA[4:0] / AAURGA[4:0]
–24 dB	10H
–25.5 dB	11H
–27 dB	12H
–28.5 dB	13H
–30 dB	14H
–31.5 dB	15H
–33 dB	16H
–34.5 dB	17H
–36 dB	18H
–37.5 dB	19H
–39 dB	1AH
–40.5 dB	1BH
–42 dB	1CH
–43.5 dB	1DH
–45 dB	1EH
Mute	1FH (Initial value)

7.4.11 VIB and LED settings (VIB)

This register is used to control the output port for the vibrator and LED.

Address: 0DH, register name: VIB, block: Analog volume, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	VIB	LED

(1) LED

Data	Mode	Initial Value	Description
0	OFF	0	Low-level output from LED pin
1	ON		High-level output from LED pin

(2) VIB

Data	Mode	Initial Value	Description
0	OFF	0	Low-level output from VIB pin
1	ON		High-level output from VIB pin

Caution For both LED and VIB, the register value is output to the pins.

7.4.12 Setting of general-purpose output pins (POUT)

This sets the output level for the general-purpose output pins (pins PO0 to PO3). It is also possible to use these pins for additional LED ports.

Address: 0EH, register name: POUT, block: PO, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	POUT3	POUT2	POUT1	POUT0

(1) POUT0 to POUT3

Data	Mode	Initial Value	Description
0	LOW	0	Low-level output from corresponding pins PO0 to PO3.
1	HIGH		High-level output from corresponding pins PO0 to PO3.

7.4.13 Soft volume setting (SVOL)

This register specifies the time of the digital volume change

Address: 0FH, register name: SVOL, block: Digital volume, access: R/W, initial value: 00H

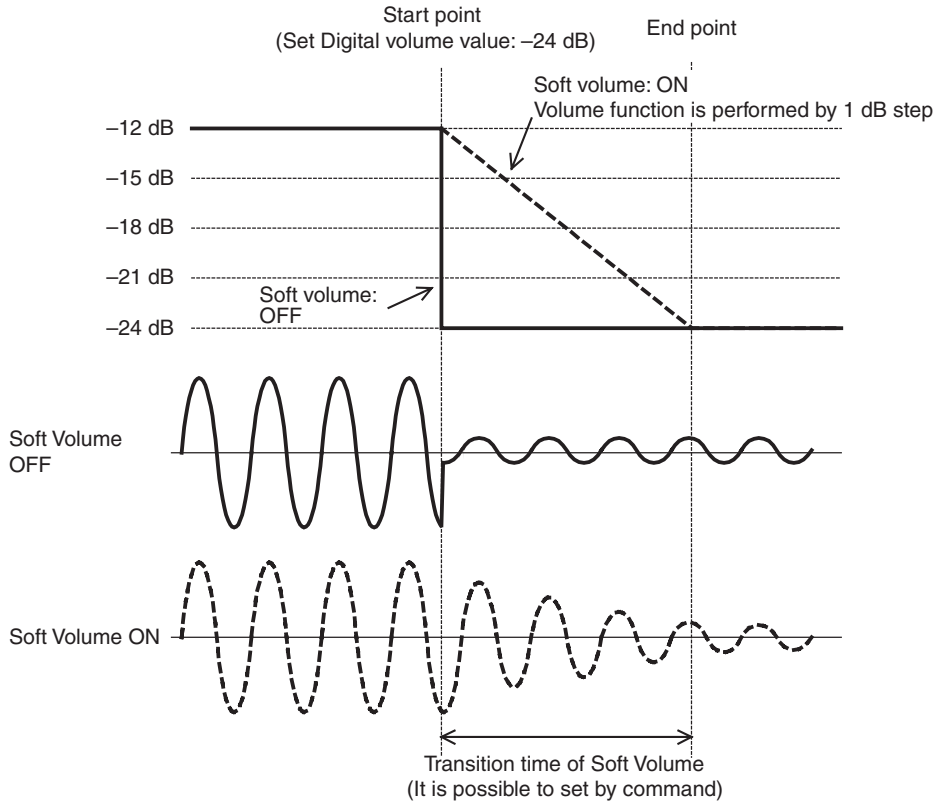
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	SVOL[1:0]	

(1) SVOL[1:0]

Data	Mode	Initial Value	Description
00B	8ms	00B	The digital volume changes at a speed of 0 dB to mute in 8 ms.
01B	16ms		The digital volume changes at a speed of 0 dB to mute in 16 ms.
10B	24ms		The digital volume changes at a speed of 0 dB to mute in 24 ms.
11B	OFF		The soft volume is not used.

Caution Volume level is changed in 1 dB steps.

Figure 7-1. The explanation of Soft volume function



Remark This figure is for example of changing digital volume setting from –12dB to –24 dB.

7.4.14 Mono setting (MONO)

This register is used to change the output signal from stereo to mono. It is possible to control the LINEOUT_L and LINEOUT_R output signal.

Address: 10H, register name: MONO, block: Digital volume, access: R/W, initial value: 00H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	MONO[1:0]	

(1) MONO[1:0]

Data	Mode	Initial Value	Description
00B	OFF	00B	Stereo output
01B	MONO1		Mono output (LINEOUT_L and LINEOUT_R are the same output.)
10B	MONO2		Mono output (LINEOUT_L and LINEOUT_R are differential outputs.) LINEOUT_L is the positive output and LINEOUT_R is the negative output.
11B	–		Setting prohibited

7.4.15 INT source register (INTSRC)

This register is used to distinguish between the PCM sound generator and DSP (MP3/AAC decoder) interrupt sources.

Address: 2FH, register name: INTSRC, block: Other, access: R

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	IDSP	ISG

(1) IDSP/ISG

Data	Mode	Initial Value	Description
ISG	S.G.	0	PCM sound generator interrupt
IDSP	DSP	0	DSP (MP3/AAC decoder) interrupt

7.4.16 LSI version (VER)

This displays the LSI version information.

Address: 3FH, register name: VER, block: Other, access: R, initial value: Differs depending on LSI version

D7	D6	D5	D4	D3	D2	D1	D0
PVER[1:0]				MVER[1:0]			

(1) PVER[3:0]

Data	Mode	Initial Value	Description
PVER[3:0]		3H	Product code

(2) MVER[3:0]

Data	Mode	Initial Value	Description
MVER[3:0]		–	LSI version

7.4.17 Bank register (BANK)

This register is used to switch the sound generator register bank, chip control register bank, and DSP register bank in serial I/F mode.

This register is available in serial I/F mode only (it is only valid when PS = 1).

Address: 4FH, register name: BANK, CPU interface, access: R/W, initial value: 01H

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	BANK	

(1) BANK

Data	Mode	Initial Value	Description
BANK		01H	Bank register for switching between sound generator register bank and chip control register bank

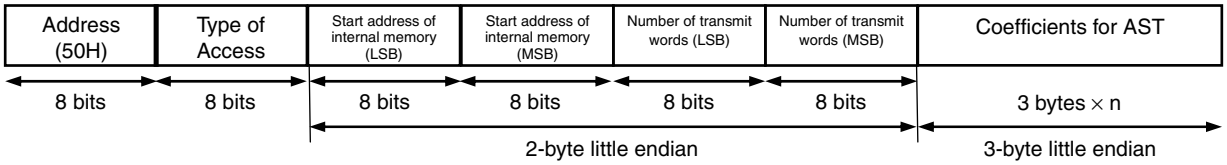
When BANK = 00B, the sound generator register bank is selected.
When BANK = 01B, the chip control register bank is selected.
When BANK = 10B, the DSP register bank is selected.

Bank register can be accessed from all register banks.

Remark Fill the unused bits (D [7:2]) with zero values. "BANK = 10B" is prohibited.

7.4.18 Surround coefficient download register (address 50H)

This register is used to download surround coefficients.



(1) Address

Address 50H of the chip control registers (BANK) is specified to this area.

In serial I/F mode (PS = 1), the R/W control signal is specified as MSB bit. ("1": Write, "0": Read)

(2) Type of access

The contents allocated to this area are as follows.

D7	D6	D5	D4	D3	D2	D1	D0
R/W	Type of access	Undefined					

Bit	Function	Description
7	R/W	0: Read mode 1: Write mode
6	Type of access	0: Single access 1: Incremental access
5 to 0	–	Undefined

(3) Start address of internal memory

The start address of the internal memory is specified to this area. Read and write access is started from this address.

The range of memory addresses is from 0 (000H) to 644 (284H).

(4) Number of transmit words

The number of transmit words (3-byte little endian) is specified to this area when incremental access is specified in "**(2) Type of access**" (D6 = 1). In the case of single access, this area must be set to 0000H.

In this area, the direction is defined by 2-byte (16 bits) little endian as in the above figure.

For example, when the number of transmit data words is 256, the setting value of this area has to be 0100H.

(5) Coefficients for AST

The coefficient data of AST is specified in this area. 1 word is defined by 3-byte little endian.

In the case of write access, this area defines the data transmitted from the host CPU to the internal AST memory.

In the case of read access, this area defines the data read from the internal AST memory.

7.4.19 Surround coefficient common write register for AST (GSRDW, DLSRDW)

These registers are used to write the surround coefficient for AST. They are used for both speaker and headphones.

Address: 59H, register name: GSRDW, block: AST, access: W, initial value: Undefined

D7	D6	D5	D4	D3	D2	D1	D0
GSRDW[7:0]							

Address: 5BH, register name: DLSRDW, block: AST, access: W, initial value: Undefined

D7	D6	D5	D4	D3	D2	D1	D0
DLSRDW[7:0]							

(1) GSRDW[7:0]

Data	Mode	Initial Value	Description
GSRDW[7:0]		Undefined	Surround coefficient setting register G1

(2) DLSRDW[7:0]

Data	Mode	Initial Value	Description
DLSRDW[7:0]		Undefined	Surround coefficient setting register D1

Caution Addresses 59H and 5BH must be written using single (normal) write access.

7.4.20 Surround coefficient common read register for AST (GSRDR, DLSRDR)

These registers are used to read the surround coefficient for AST. They are used for both speaker and headphones.

Address: 64H, register name: GSRDR, block: AST, access: R, initial value: Undefined

D7	D6	D5	D4	D3	D2	D1	D0
GSRDR[7:0]							

Address: 66H, register name: DLSRDR, block: AST, access: R, initial value: Undefined

D7	D6	D5	D4	D3	D2	D1	D0
DLSRDR[7:0]							

(1) GSRDR[7:0]

Data	Mode	Initial Value	Description
GSRDR[7:0]		30H	Surround coefficient setting register G1

(2) DLSRDR[7:0]

Data	Mode	Initial Value	Description
DLSRDR[7:0]		20H	Surround coefficient setting register D1

Caution Addresses 64H and 66H must be written using single (normal) write access.

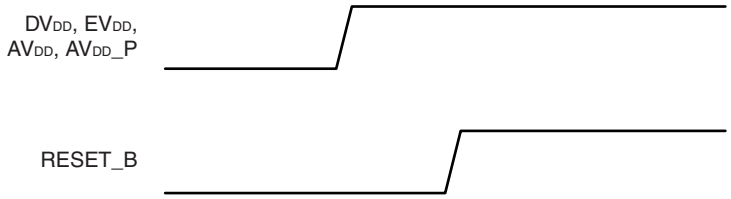
8. POWER STARTUP PROCEDURE

The μPD9993 includes 4 power supply units: the internal digital logic block power supply (DV_{DD}), PLL1/PLL2 power supply (AV_{DD}_P), internal analog circuit power supply (AV_{DD}), and the I/O circuit power supply (EV_{DD}).

8.1 Wakeup Sequence

<1> With the RESET_B pin set to low level, turn on the power supply units (DV_{DD}, AV_{DD}, AV_{DD}_P, and EV_{DD}). It is recommended turning on all four of these units at the same time.
<2> Wait until the power supply voltage reaches the specified voltage value.
<3> Negate the hardware reset.
To negate, set the RESET_B pin to high level.

★



Caution The state of all pins is undefined immediately after power supply startup.
All pins including data bus are undefined states if all the power supplies are turned on during the RESET_B pin is high level. So bus fight may happens.

8.2 Shutdown Sequence

<1> With the RESET_B pin set to low level, turn off the power supply units (DV_{DD}, AV_{DD}, AV_{DD}_P, and EV_{DD}). It is recommended turning off all four of these units at the same time.
<2> After power-down, the status of the RESET_B pin is undefined.

9. POWER SAVING FUNCTION

The μPD9993 includes 2 power saving functions (standby modes). One of them is controlled by command input, and the other is controlled by the power supply.

9.1 Software Power Saving Function (Command-Driven)

The μPD9993 includes a power saving function (standby mode) that is controlled by command input.

This register exists at address 00H of the chip control registers (or chip control register bank).

9.2 Hardware Power Saving Function (by Powering Down Power Supply)

In addition to the software power saving function, a hardware power saving function is available. In such cases, note with caution that all data written to registers and memory will be deleted (be sure to rewrite this data after return to normal operation).

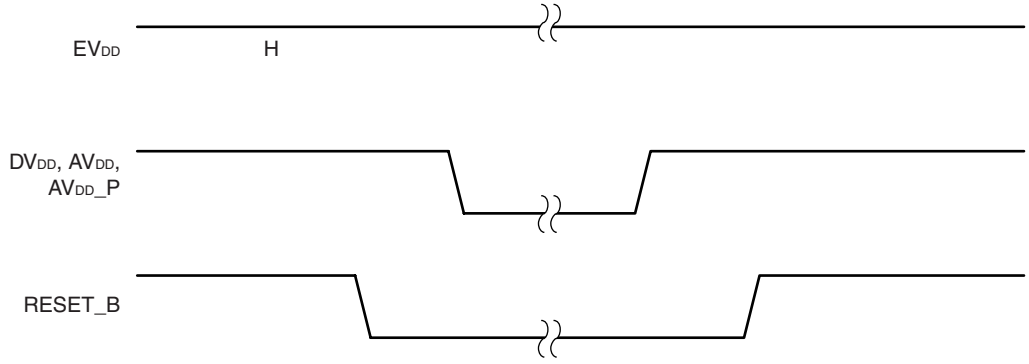
Follow the steps described below when setting hardware power saving.

<1> With the RESET_B pin set to low level, turn off DV_{DD}, AV_{DD}, and AV_{DD}_P.
<2> Continue supplying EV_{DD} since it is used to protect the CPU bus line.
<3> Be sure to fix the RESET_B pin to low level during a hardware power saving operation.

Follow the steps described below to return to normal operation.

<1> With the RESET_B pin set to low level, turn on DV_{DD}, AV_{DD}, and AV_{DD}_P.
<2> Set the RESET_B pin to high level.

★



Caution All pins including data bus may output invalid data if the RESET_B pin is high level during hardware standby, so bus fight may happens.
All pins including data bus may sink current if the EV_{DD} is turned off during hardware standby, so bus fight may happens.

10. SETTING SEQUENCE

In this chapter, 3 steps, 'Switching to SG bank', 'Switching to DSP bank' and 'switching to chip control bank' are required when PS = 1 (serial I/F mode).

- 'Switching to SG bank' means to switch to the sound generator (SG)register area.
- 'Switching to Chip Control Bank' means to switch to the chip control register area.
- 'Switching to DSP Bank' means to switch to the DSP (MP3/AAC decoder) register area.

These step are not required when PS = 0 (parallel I/F mode).

10.1 Power Up

Steps	Items	Target Register, etc.
1	Negate hardware reset	RESET_B pin (from low to high)
2	Set PLL	MCLK1A, MCLK1B, MCLK2A, MCLK2B
3	Set sampling frequency	FS
4	Activate PLLs	STPLL1, STPLL2
5	Start to supply clock to CLKIN	CLKIN pin
6	Activate blocks	STSYNTH, STDIG, STDSP, STASI, STASO, STDAC
7	Internal clock is enabled	After activation standby, normal operation begins after at least 5 ms have elapsed.

10.2 Basic Sequence for Switching Among Operation Modes

Steps	Items	Target Register, etc.
1	Switching to chip control bank (When PS = 1)	BANK
2	Lower analog volume step by step (recommended)	AAULGA, AAURGA
3	Set analog volume to mute	AAULGA, AAURGA
4	Set standby mode	STPLL1, STPLL2, STSYNTH, STDSP, STDIG, STASI, STASO, STDAC
5	Switch SG/DSP/ASI path	SLSORCE, MIX
6	Switching surround on/off setting	ENSRD
7	Set sampling frequency	FS
8	Set ASIO mode	MS, ASIM, LRCLK, SLR
9	Activate PLLs	STPLL1, STPLL2
10	Activates blocks	STSYNTH, STDSP, STDIG, STASI, STASO, STDAC
11	Internal clock is enabled	After activation, normal operation begins after at least 5 ms have elapsed.
12	Cancel mute of analog volume	AAULGA, AAURGA
13	Raise analog volume step by step (recommended)	AAULGA, AAURGA

Remarks 1. In slave mode, LRCLK and BCLK must be supplied.

2. To eliminate any audible change in sound that can occur due to single-frame operation errors in the digital data that is generated while switching, we recommend muting the analog volume to lower it step by step. Also raise the analog volume step by step after mode chenge.
An example of raising and lowering volume step by step is shown below.

Example: Step = 1.5 dB (minimum unit)
Cycle (time per step) for raising or lowering = 200 μs per step

These values are merely an example. Adjustments for each set should be made as determined.

3. The STDIG signal is also used to reset operations such as digital filter operations, so it is required when switching modes.

10.2.1 Mute

Steps	Items	Target Register, etc.
1	Switching to chip control bank (When PS = 1)	BANK
2	Lower analog volume step by step (recommended)	AAULGA, AAURGA
3	Set analog volume to mute	AAULGA, AAURGA

10.2.2 Standby

Steps	Items	Target Register, etc.
1	Switching to chip control bank (When PS = 1)	BANK
2	Lower analog volume step by step (recommended)	AAULGA, AAURGA
3	Set analog volume to mute	AAULGA, AAURGA
4	Set standby mode	STPLL1, STPLL2, STSYNTH, STDSP, STDIG, STASI, STASO, STDAC
5	Activate PLLs	STPLL1, STPLL2
6	Activate blocks	STSYNTH, STDSP, STDIG, STASI, STASO, STDAC
7	Internal clock is enabled	After activation, normal operation begins after at least 5 ms have elapsed.
8	Cancel mute of analog volume	AAULGA, AAURGA
9	Raise analog volume step by step (recommended)	AAULGA, AAURGA

10.2.3 Sampling frequency

Steps	Items	Target Register, etc.
1	Switching to chip control bank (when PS = 1)	BANK
2	Lower analog volume step by step (recommended)	AAULGA, AAURGA
3	Set analog volume to mute	AAULGA, AAURGA
4	Set standby mode	STPLL1, STPLL2, STSYNTH, STDSP, STDIG, STASI, STASO, STDAC
5	Set sampling frequency	FS
6	Activate PLLs	STPLL1, STPLL2
7	Activate blocks	STSYNTH, STDSP, STDIG, STASI, STASO, STDAC
8	Internal clock is enabled	After activation, normal operation begins after at least 5 ms have elapsed.
9	Cancel mute of analog volume	AAULGA, AAURGA
10	Raise analog volume step by step (recommended)	AAULGA, AAURGA

10.2.4 Path switching

Steps	Items	Target Register, etc.
1	Switching chip control bank (When PS = 1)	BANK
2	Lower analog volume step by step (recommended)	AAULGA, AAURGA
3	Set analog volume to mute	AAULGA, AAURGA
4	Switch SG/DSP/ASI path	SLSORCE, MIX
5	Cancel mute of analog volume	AAULGA, AAURGA
6	Raise analog volume step by step (recommended)	AAULGA, AAURGA

Caution Data may be incorrect in one frame.

10.2.5 Surround switching

Steps	Items	Target Register, etc.
1	Switching to chip control bank (when PS = 1)	BANK
2	Lower analog volume step by step (recommended)	AAULGA, AAURGA
3	Set analog volume to mute	AAULGA, AAURGA
4	Switching surround on/off setting	ENSRD
5	Cancel mute of analog volume	AAULGA, AAURGA
6	Raise analog volume step by step (recommended)	AAULGA, AAURGA

Caution Data may be incorrect in one frame.

10.2.6 Set ASIO mode

Steps	Items	Target Register, etc.
1	Switching to chip control bank (when PS = 1)	BANK
2	Lower analog volume step by step (recommended)	AAULGA, AAURGA
3	Set analog volume to mute	AAULGA, AAURGA
4	Set standby mode	STPLL1, STPLL2, STSYNTH, STDSP, STDIG, STASI, STASO, STDAC
5	Set ASIO mode	MS, ASIM, LRCLK, SLR
6	Activate PLLs	STPLL1, STPLL2
7	Activate blocks	STSYNTH, STDSP, STDIG, STASI, STASO, STDAC
8	Internal clock is enabled	After activation, normal operation begins after at least 5 ms have elapsed.
9	Cancel mute of analog volume	AAULGA, AAURGA
10	Raise analog volume step by step (recommended)	AAULGA, AAURGA

Caution Data may be incorrect in one frame.

10.2.7 AST RAM access

The coefficient RAM for AST (AST-RAM) uses PLL2 for the clock signal when coefficients are downloaded from the host CPU. In normal operation, AST uses only PLL1 for the clock signal.

(1) When starting up or during PLL2 standby

Steps	Items	Target Register, etc.
1	Negate hardware reset after supplying power	RESET_B pin (from low to high)
2	Sets surround control register	ENSRD = 00B
3	Activate PLL2	STPLL2 = 1
4	Internal clock is enabled	After activation, normal operation begins after at least 5 ms have elapsed.
5	Start address setting	SRDRA, address of coefficients
6	Data transfer	Data transfer

(2) When PLL2 is already activated

Steps	Items	Target Register, etc.
1	Switching to chip control bank (when PS = 1)	BANK
2	Sets surround control register	ENSRD = 00B
3	Internal clock is enabled	After setting ENSRD = 00B, AST-RAM is ready for writing/reading after at least 400 ns have elapsed.
4	Start address setting	SRDRA, address of coefficients
5	Data transfer	Data transfer

10.3 Setting Sequence Example

10.3.1 Sound generator - DAC output

(1) Power up

Steps	Items	Target Register, etc.
1	Negate hardware reset	RESET_B pin (from low to high)
2	Set PLLs	MCLK1A, MCLK1B, MCLK2A, MCLK2B
3	Set sampling frequency	FS 32 kHz
4	SG/DSP/ASI path switching	SLSORCE = 00B
5	Activate PLLs	STPLL1 = STPLL2 = 1
6	Start to supply clock to CLKIN	CLKIN pin
7	Activate blocks	STDIG = STSYNTH = STDAC = 1
8	Internal clock is enabled	After activation, normal operation begins after at least 5 ms have elapsed.

(2) 'Switching to SG bank' (When PS = 1)

(3) Sound generator setting

(4) Sound generator data transfer

(5) Volume up

Steps	Items	Target Register, etc.
9	Switching to chip control bank (when PS = 1)	BANK
10	Cancel mute of analog volume	AAULGA, AAURGA
11	Raise analog volume step by step (recommended)	AAULGA, AAURGA

10.3.2 Sound generator - ASO output

(1) Power up

Steps	Items	Target Register, etc.
1	Negate hardware reset	RESET_B pin (from low to high)
2	Set PLLs	MCLK1A, MCLK1B, MCLK2A, MCLK2B
3	Set sampling frequency	FS 32 kHz
4	SG/DSP/ASI path switching	SLSORCE = 00B
5	Set ASIO mode	MS, ASIM, LRCLK, SLR MS = 0: Slave mode; external LRCLK and BCLK required. MS = 1: Master mode
6	Activate PLLs	STPLL1 = STPLL2 = 1
7	Start to supply clock to CLKIN	CLKIN pin
8	Activate blocks	STDIG = STSYNTH = STASO = 1
9	Internal clock is enabled.	After activation, normal operation begins after at least 5 ms have elapsed.

(2) 'Switching to SG bank' (when PS = 1)

(3) Sound generator setting

(4) Sound generator data transfer

10.3.3 DSP (MP3/AAC decoder) - DAC output

(1) Power up

Steps	Items	Target Register, etc.
1	Negate hardware reset	RESET_B pin (from low to high)
2	Set PLLs	MCLK1A, MCLK1B, MCLK2A, MCLK2B
3	Set sampling frequency	FS 8 kHz, 16 kHz, 32 kHz, 44.1 kHz, or 48 kHz
4	SG/DSP/ASI path switching	SLSORCE = 10B
5	Activate PLLs	STPLL1 = STPLL2 = 1
6	Start to supply clock to CLKIN	CLKIN pin
7	Activate blocks	STDIG = STDSP = STDAC = 1
8	Internal clock is enabled.	After activation, normal operation begins after at least 5 ms have elapsed.

(2) 'Switching to DSP bank' (when PS = 1)

(3) DSP (MP3/AAC decoder) setting

(4) DSP (MP3/AAC decoder) data transfer

(5) Volume up

Steps	Items	Target Register, etc.
9	Switching to chip control bank (when PS = 1)	BANK
10	Cancel mute of analog volume	AAULGA, AAURGA
11	Raise analog volume step by step (recommended)	AAULGA, AAURGA

10.3.4 DSP (MP3/AAC decoder) - ASO output

(1) Power up

Steps	Items	Target Register, etc.
1	Negate hardware reset	RESET_B pin (from low to high)
2	Set PLLs	MCLK1A, MCLK1B, MCLK2A, MCLK2B
3	Set sampling frequency	FS 8 kHz, 16 kHz, 32 kHz, 44.1 kHz, or 48 kHz
4	SG/DSP/ASI path switching	SLSORCE = 10B
5	Set ASIO mode	MS, ASIM, LRCLK, SLR MS = 0: Slave mode; external LRCLK and BCLK required. MS = 1: Master mode
6	Activate PLLs	STPLL1 = STPLL2 = 1
7	Start to supply clock to CLKIN	CLKIN pin
8	Activate blocks	STDIG = STDSP = STASO = 1
9	Internal clock is enabled	After activation, normal operation begins after at least 5 ms have elapsed.

(2) 'Switching to DSP bank' (when PS = 1)

(3) DSP (MP3/AAC decoder) setting

(4) DSP (MP3/AAC decoder) data transfer

10.3.5 ASI-DAC output

(1) Power up

Steps	Items	Target Register, etc.
1	Negate hardware reset	RESET_B pin (from low to high)
2	Set PLLs	MCLK1A, MCLK1B
3	Set sampling frequency	FS 8kHz, 16kHz, 32 kHz, 44.1 kHz, or 48 kHz
4	SG/DSP/ASI path switching	SLSORCE = 01B
5	Set ASIO mode	MS, ASIM, LRCLK, SLR MS = 0: Slave mode; external LRCLK and BCLK required. MS = 1: Master mode
6	Activate PLLs	STPLL1 = 1
7	Start to supply clock to CLKIN	CLKIN pin
8	Activate blocks	STDIG = STASI = STDAC = 1
9	Internal clock is enabled.	After activation, normal operation begins after at least 5 ms have elapsed.

(2) Music data transmission

(3) Volume up

Steps	Items	Target Register, etc.
10	Cancel analog volume to mute	AAULGA, AAURGA
11	Raise analog volume step by step (recommended)	AAULGA, AAURGA

10.3.6 ASI-ASO output

(1) Power up

Steps	Items	Target Register, etc.
1	Negate hardware reset	RESET_B pin (from low to high)
2	Set PLLs	MCLK1A, MCLK1B
3	Set sampling frequency	FS 8kHz, 16kHz, 32 kHz, 44.1 kHz, or 48 kHz
4	Sound generator/audio path switching	SLSORCE = 01B
5	Set ASIO mode	MS, ASIM, LRCLK, SLR MS = 0: Slave mode; external LRCLK and BCLK required. MS = 1: Master mode
6	Activate PLLs	STPLL1 = 1
7	Start to supply clock to CLKIN	CLKIN pin
8	Activate blocks standby	STDIG = STASI = STASO = 1
9	Internal clock is enabled	After activation, normal operation begins after at least 5 ms have elapsed.

(2) Music data transmission

10.4 Relationship between Setting Modes and Internal Operations (Relationship with Synchronization Clock)

Table 10-1. Relationship between Setting Modes and Internal Operations (Relationship with Synchronization Clock)

Mode	Path	Function	Register				Pin (Signal) Status					Actual Use	Remark
			MS	SLSORCE[1:0]	STASI	STASO	LRCLK, BCLK	Sync. Frame Clock	ASI	ASO	LINE_OUT		
Slave mode	SG path	Both ASI and ASO standby	0 slave	00 synth	0 off	0 off	Input	Internal	Invalid	Hi-Z	OUT	Sound generator-DAC	Even though slave mode has been set, the internal clock operates.
		ASI standby, ASO output	0 slave	00 synth	0 off	1 on	Input	External	Invalid	OUT	OUT	Sound generator-DAC, ASO	Have to input an external LRCLK. If the external LRCLK signal has not yet been input, output is stopped.
	DSP(MP3/AAC) path	Both ASI and ASO standby	0 slave	10 DSP	0 off	0 off	Input	Internal	Invalid	Hi-Z	OUT	DSP-DAC	Even though slave mode has been set, the internal clock operates.
		ASI standby, ASO output	0 slave	10 DSP	0 off	1 on	Input	External	Invalid	OUT	OUT	DSP-DAC, ASO	Have to input an external LRCLK. If the external LRCLK signal has not yet been input, output is stopped.
	ASI path	ASI input, ASO standby	0 slave	01 ASI	1 on	0 off	Input	External	IN	Hi-Z	OUT	ASI-DAC	Have to input an external LRCLK. If the external LRCLK signal has not yet been input, output is stopped.
		ASI input, ASO output	0 slave	01 ASI	1 on	1 on	Input	External	IN	OUT	OUT	ASI-DAC, ASO	Have to input an external LRCLK. If the external LRCLK signal has not yet been input, output is stopped.
Master mode	SG path	Both ASI and ASO standby	1 master	00 synth	0 off	0 off	Low output	Internal	Invalid	Hi-Z	OUT	Sound generator-DAC	The internal clock operates.
		ASI standby, ASO output	1 master	00 synth	0 off	1 on	Signal output	Internal	Invalid	OUT	OUT	Sound generator-DAC, ASO	The internal clock operates.
	DSP(MP3/AAC) path	Both ASI and ASO standby	1 master	10 DSP	0 off	0 off	Low output	Internal	Invalid	Hi-Z	OUT	DSP-DAC	The internal clock operates.
		ASI standby, ASO output	1 master	10 DSP	0 off	1 on	Signal output	Internal	Invalid	OUT	OUT	DSP-DAC, ASO	The internal clock operates.
	ASI path	ASI input, ASO standby	1 master	01 ASI	1 on	0 off	Signal output	Internal	IN	Hi-Z	OUT	ASI-DAC	The internal clock operates.
		ASI input, ASO output	1 master	01 ASI	1 on	1 on	Signal output	Internal	IN	OUT	OUT	ASI-DAC, ASO	The internal clock operates.

Remark The operations in Table 10-1 apply to the operations in mixing mode (address 05H, MIX = 1). Therefore, when setting mixing (MIX = 1) while the ASIO is in slave mode (address 08H, MS = 0), be sure to set STASI = 1 and input BCLK and LRCLK.

When stopping the ASI input and using the sound generator only, retain the settings of MS = 1, MIX = 1, and STASI = 1 or set MIX = 0 and SLSORCE[1:0] = 00.

11. STANDBY MODE

Standby mode for various blocks is described.

11.1 Clock Supply

In the standby mode for PLL1 and PLL2, access is enabled only for the standby register at address 00H, the master clock setting registers at addresses 01H, 02H, 03H, and 04H, the LED/VIB control register at address 0DH, and the general-purpose output pin setting register at address 0EH in the chip control registers (BANK).

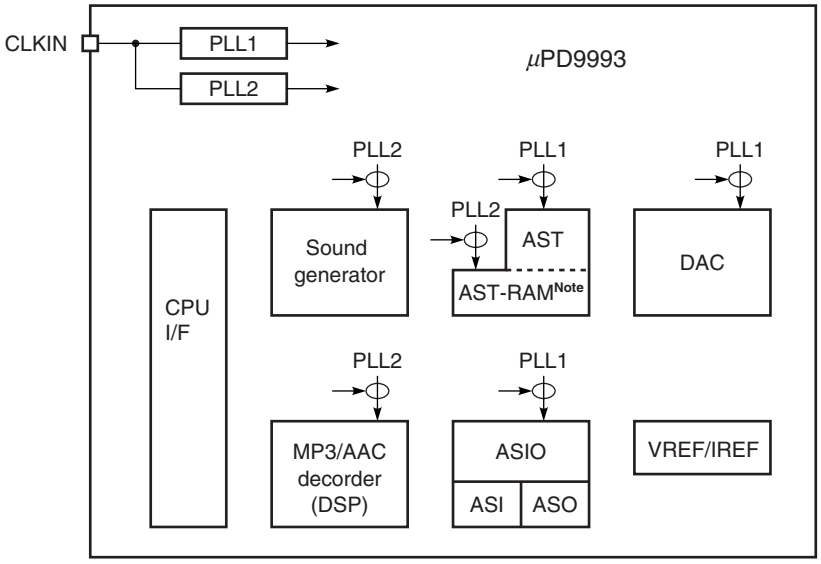
The sound generator registers (BANK), DSP registers (BANK), and all other registers except the ones above cannot be accessed during in standby mode for PLL1 and PLL2.

To use AST[Note], DAC and ASIO, the PLL1 must be activated.

To use the sound generator, MP3/AAC decoder, and to download AST coefficients, the PLL2 must be activated.

The supply of clock signals from the PLL to various blocks is illustrated in Figure 11-1.

Figure 11-1. Destination of Clocks Supplied from PLL1 and PLL2

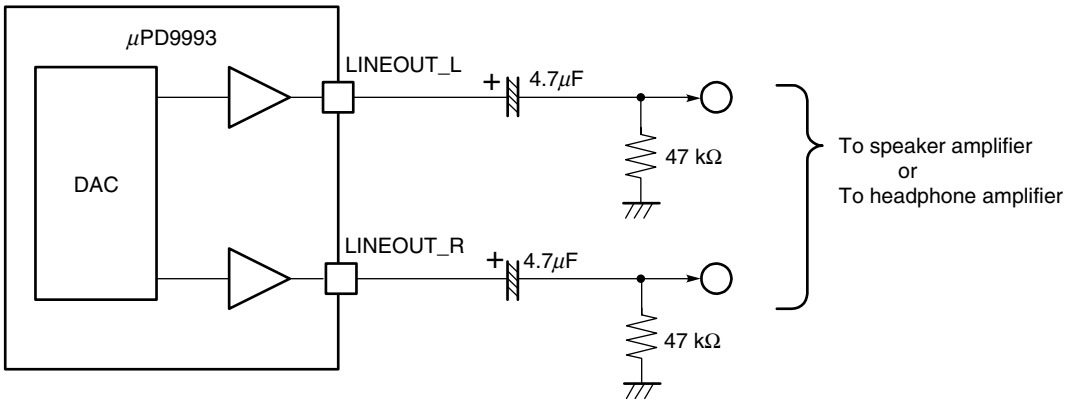


Note The coefficient RAM for AST (AST-RAM) uses PLL2 for the clock signal when coefficients are downloaded from the host CPU. In normal operation, AST uses only PLL1 for the clock signal.

12. REFERENCE SCHEMATICS

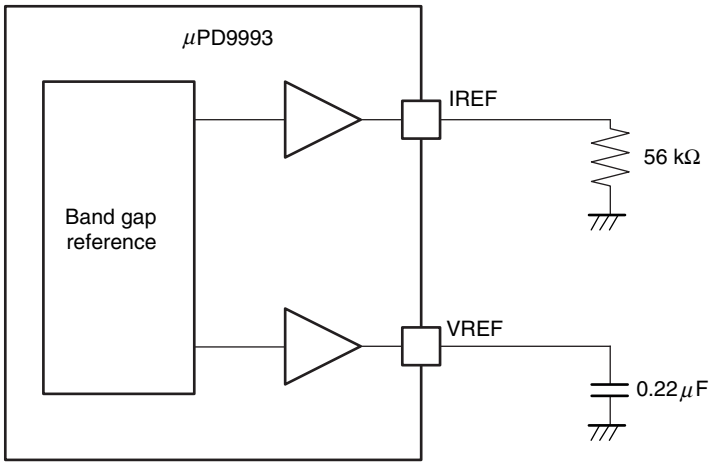
12.1 Line Out Pins (LINEOUT_L and LINEOUT_R)

Figure 12-1. Example of Connection to Line Out Pin



12.2 Reference Power Supply Voltage and Current Supply Pins (VREF and IREF)

Figure 12-2. Handling of VREF and IREF Pins



The VREF and IREF blocks include the following functions.

- Reference voltage is generated using band gap
- The reference current is generated using this reference voltage and an external resistance, and is supplied to all analog circuits.

The VREF and IREF blocks operates when STPLL1 = 1, STPLL2 = 1 or STDAC =1 in the STNBY register.
They become stable within 5ms after at least one of STPLL1, STPLL2 or STDAC is set to "1".

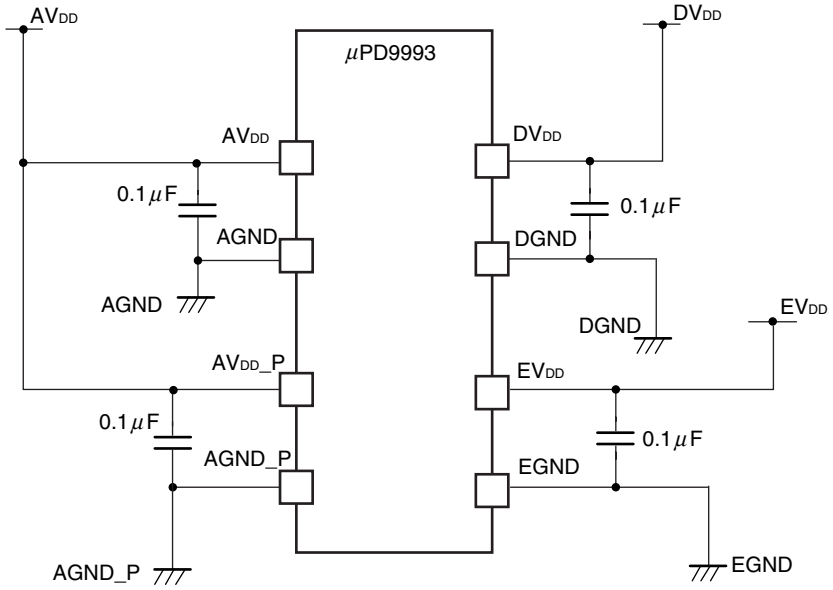
Cautions 1. Be sure to connect a 56 kΩ (±5%) resistor between the IREF pin and AGND. Do not connect any other resistors to the IREF pin.

2. Be sure to connect a 0.22 μF (±20%) capacitor between the VREF pin and AGND. Do not connect any other capacitors to the VREF pin.

12.3 Power Supply

Place decoupling capacitors as close as possible to any of the μPD9993 pins.

Figure 12-3. Placement of Decoupling Capacitor

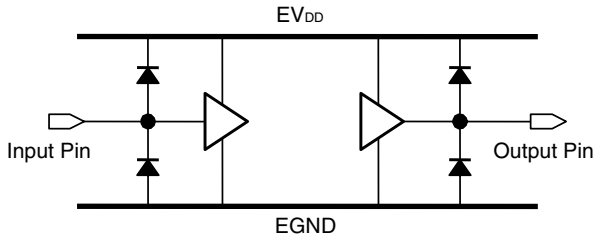
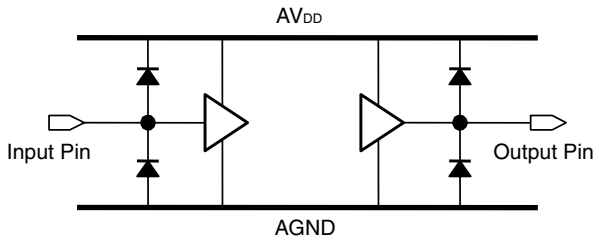
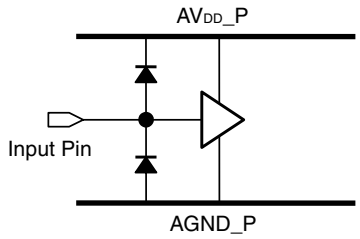
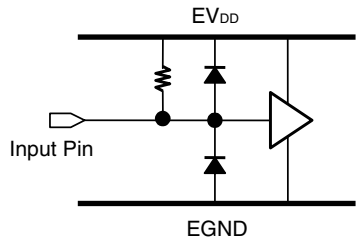
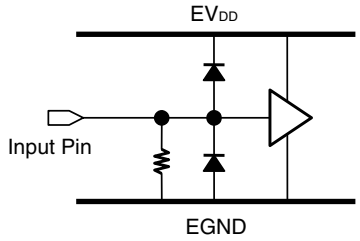


The pairing of pins between the power supply (with decoupling capacitor) and GND is as follows (pin numbers are indicated in parentheses).

AVDD (1E) – AGND (1D)
AVDD_P (2G) – AGND_P (1H)
DVDD (9K) – DGND (5K)
DVDD (10D) – DGND (10J)
EVDD (9C) – EGND (6A)
DVDD (9A) – EGND (6A)
DVDD (4C) – DGND (5C)
DVDD (8C) – DGND (8E)

Caution EVDD is used for digital operations. Therefore, it is recommended to use a different power supply to the analog power supplies (AVDD and AVDD_P) to avoid affecting the analog characteristics.

12.4 Pin Outline Schematics

Input Pin	Output Pin	Pin Outline Schematic
PO0 to PO3, A1/RXD, A0/Data, TXD, A2, CS_B/SCS, WR_B/SCLK, RD_B/SPIMODE, D0/SERINIT, D1 to D7, RESET_B, LRCLK, BCLK	PO0 to PO3, A0/Data,TXD, D0/SERINIT, D1to D7, INT_B, VIB, LED, LRCLK, BCLK, ASO, INT_SG_B, INT_DSP_B, TM3, TM4, TM10	
IREF, VREF	IREF, VREF, LINEOUT_L, LINEOUT_R	
CLKIN	–	
TM5, TM6	–	
ASI, PS, TRSCK, CLK8K, RDATA, TM0 to TM2, TM7 to TM9	–	

13. ELECTRICAL SPECIFICATIONS

13.1 Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	DV_{DD}	For digital block	–0.3 to +2.0	V
	EV_{DD}	For digital I/O block	–0.3 to +4.0	V
	AV_{DD}	For analog block	–0.3 to +4.0	V
	AV_{DD}_P	For analog PLL block	–0.3 to +4.0	V
Input voltage	V_I	$V_I/V_O < EV_{DD}$ + 0.5 V	–0.3 to +4.0	V
Output voltage	V_O		–0.3 to +4.0	V
Power dissipation	P_D		300	mW
Storage temperature	T_{stg}		–50 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

13.2 Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating voltage	DV_{DD}		1.425	1.5	1.575	V
	EV_{DD}		1.71	3.0	3.3	V
	AV_{DD}		2.7	3.0	3.3	V
	AV_{DD}_P		2.7	3.0	3.3	V
Input voltage	V_I		0		EV_{DD}	V
Operating ambient temperature	T_A		–20		+85	°C

13.3 Capacitance

(T_A = +25°C, DV_{DD} = 0 V, EV_{DD} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz, pins other than those tested: 0 V		10		pF
Output capacitance	C_O			10		pF
I/O capacitance	C_{IO}			10		pF

13.4 Load Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Load resistance of LINEOUT	R_L	Between LINEOUT and GND	10	47		kΩ
VREF capacitance	C_{ref}	Between VREF and GND, ±20%	0.17	0.22	0.27	μF
IREF resistance	R_{ref}	Between IREF and GND, ±5%	53	56	59	kΩ

13.5 DC Characteristics

(T_A = –20 to +85°C, with DV_{DD} and EV_{DD} within recommended operating condition range)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IHN}		0.8 EV_{DD}		EV_{DD}	V
Input voltage, low	V_{ILN}		0		0.2 EV_{DD}	V
Output voltage, high	V_{OH}	I_{OH} = –1 mA	0.8 EV_{DD}			V
Output voltage, low	V_{OL3}	I_{OL} = +1 mA			0.2 EV_{DD}	V
Input leakage current, high	I_{LHN}	$V_I = EV_{DD}$	0		20	μA
Input leakage current, low	I_{LLN}	V_I = 0 V	–20		0	μA
High-impedance leakage current	I_{ZI}	0 V ≤ V_I ≤ EV_{DD}	–20		+20	μA

13.6 AC Characteristics

(Unless otherwise specified, T_A = –20 to +85°C, with DV_{DD} and EV_{DD} within recommended operating condition range)

13.6.1 Clock

Timing requirements

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CLKIN input frequency	f_{CLKIN}	V_{CLKIN} = 0.5 V_{p-p}	2.688		26	MHz
CLKIN input level	V_{CLKIN}	f_{CLKIN} = 2.688 MHz to 26 MHz[Note 1]	0.5		**Note 2**	V_{p-p}

Notes 1. CLKIN input to be used as PLL input should have capacitive coupling (1000 pF).

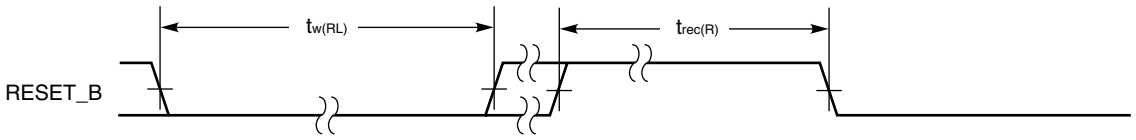
2. The maximum input level for CLKIN should not exceed the power supply (AV_{DD}_P) potential.

13.6.2 Reset

Timing requirements

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
RESET_B low-level width	$t_{w(RL)}$		250			ns
RESET_B recovery time	$t_{rec(R)}$		250			ns

Reset timing



13.6.3 Host interface

(1) Parallel I/F mode

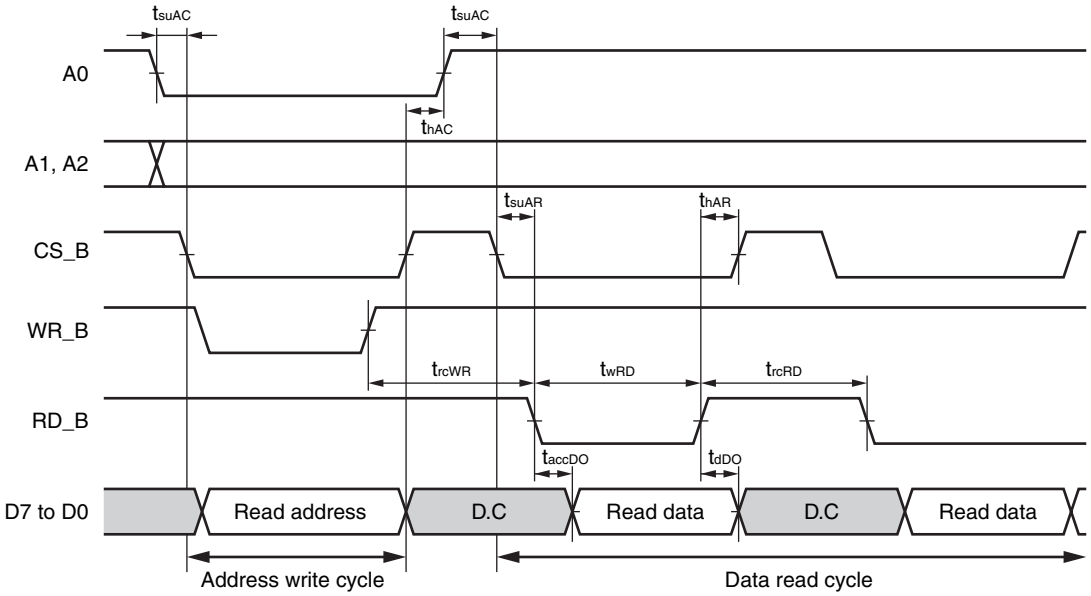
Timing requirements (Both EV_{DD} = 1.8 V and EV_{DD} = 3.0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
RD_B width	t_{wRD}		125			ns
WR_B width	t_{wWR}		125			ns
RD_B recovery time	t_{rcRD}		60			ns
WR_B recovery time	t_{rcWR}		100			ns
Data setup time	t_{suDI}	WR_B↑	50			ns
Data hold time	t_{hDI}	WR_B↑	0			ns
CS_B setup time	t_{suAW}	WR_B↓	0			ns
CS_B hold time	t_{hAW}	WR_B↑	0			ns
CS_B setup time	t_{suAR}	RD_B↓	0			ns
CS_B hold time	t_{hAR}	RD_B↑	0			ns
A setup time	t_{suAC}	CS_B↓	10			ns
A hold time	t_{hAC}	CS_B↑	10			ns

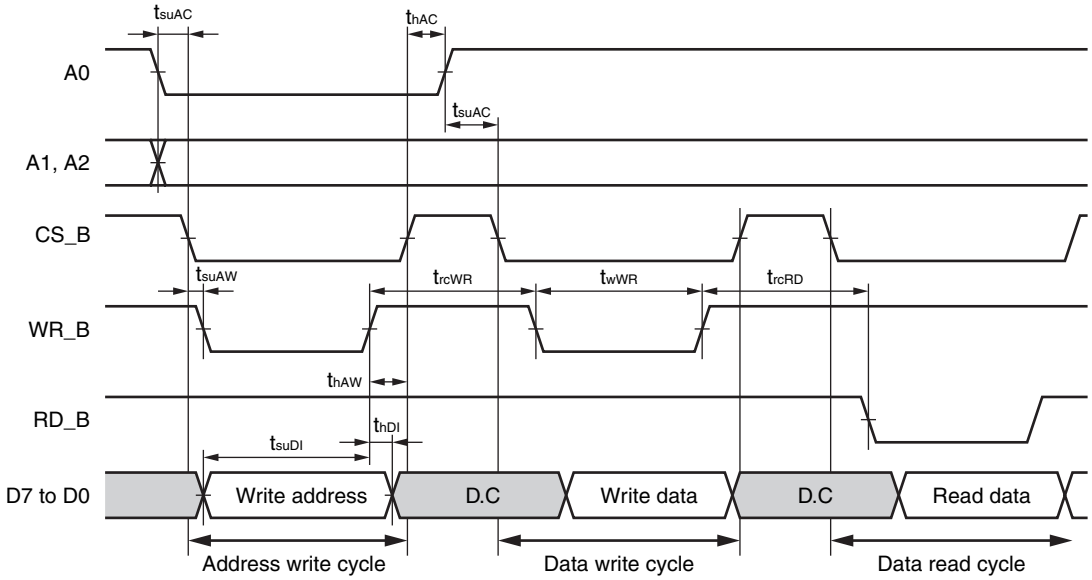
Switching characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data access time	t_{accDO}	RD_B↓, I_{sink} = 1 mA			125	ns
Data hold time	t_{dDO}	RD_B↑, I_{sink} = 1 mA	0		60	ns

Host interface read timing



Host interface write timing



(2) Serial I/F mode (Both 3-wire SPI mode and 4-wire SPI mode)

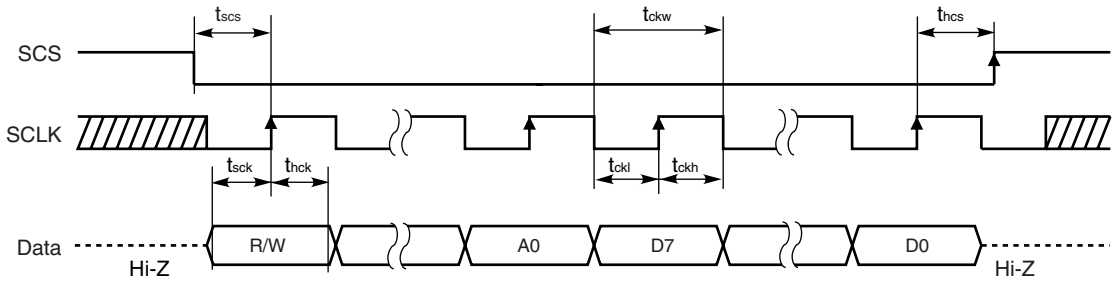
Timing requirements (EV_{DD} = 3.0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
A period of SCLK	t_{ckw}		76			ns
A high level width of SCLK	t_{ckh}		36			ns
A low level width of SCLK	t_{ckl}		36			ns
Setup time of data	t_{sck}	SCLK↑	10			ns
Hold time of data	t_{hck}	SCLK↑	10			ns
Setup time of SCS	t_{scs}	SCLK↑	30			ns
Hold time of SCS	t_{hcs}	SCLK↑	20			ns
Access time of read data	t_{racc}	SCLK↓	2		20	ns
Access time of next SCS	t_{csacc}	From SCS↑ to Next SCS↓	1			SCLK
High-impedance transition time	t_{dz}	SCLK↓	0		20	ns
Hold time of SERINIT	$t_{hcsinit}$	SCLK↑	80			ns
SERINIT active time after SCS not active	t_{dhh}	SERINIT↑	0			ns
SERINIT width	$t_{whSERINIT}$		10			ns
SERINIT inactive time before SCS active	t_{dll}	SERINIT↓	0			ns

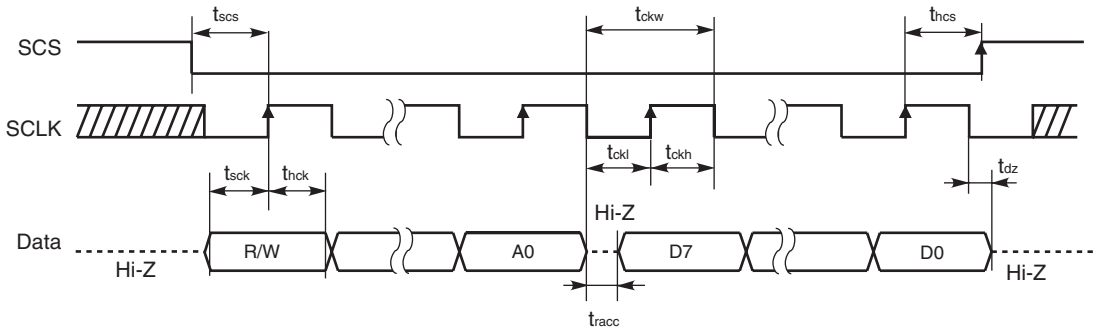
Timing requirements (EV_{DD} = 1.8 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
A period of SCLK	t_{ckw}		140			ns
A high level width of SCLK	t_{ckh}		68			ns
A low level width of SCLK	t_{ckl}		68			ns
Setup time of data	t_{sck}	SCLK↑	10			ns
Hold time of data	t_{hck}	SCLK↑	10			ns
Setup time of SCS	t_{scs}	SCLK↑	30			ns
Hold time of SCS	t_{hcs}	SCLK↑	20			ns
Access time of read data	t_{racc}	SCLK↓	2		50	ns
Access time of next SCS	t_{csacc}	From SCS↑ to Next SCS↓	1			SCLK
High-impedance transition time	t_{dz}	SCLK↓	0		20	ns
Hold time of SERINIT	$t_{hcsinit}$	SCLK↑	100			ns
SERINIT active time after SCS not active	t_{dhh}	SERINIT↑	0			ns
SERINIT width	$t_{whSERINIT}$		10			ns
SERINIT inactive time before SCS active	t_{dll}	SERINIT↓	0			ns

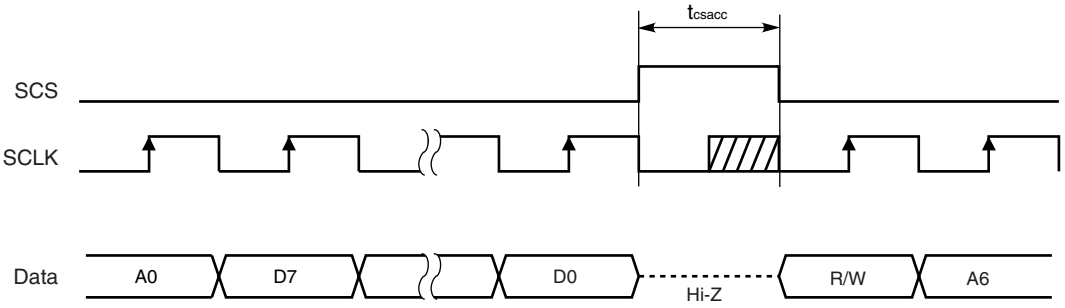
Serial interface write timing



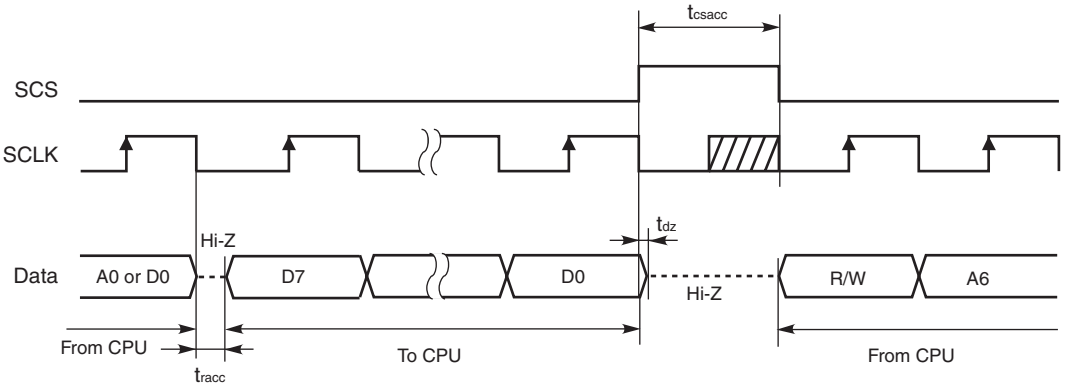
Serial interface read timing



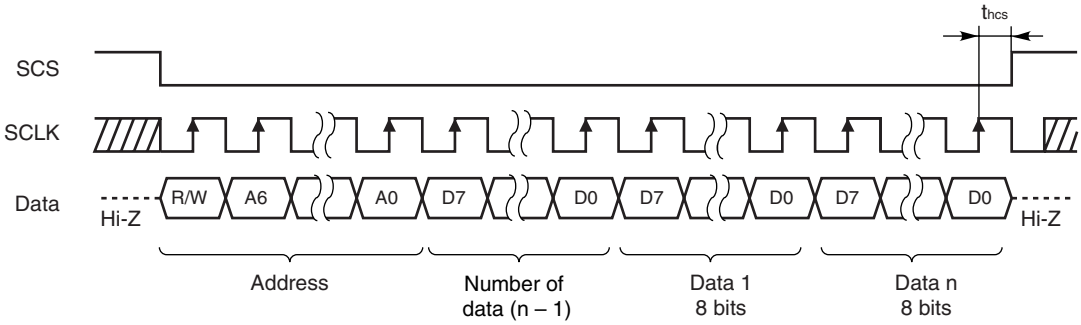
Serial interface write timing (Continuous access)



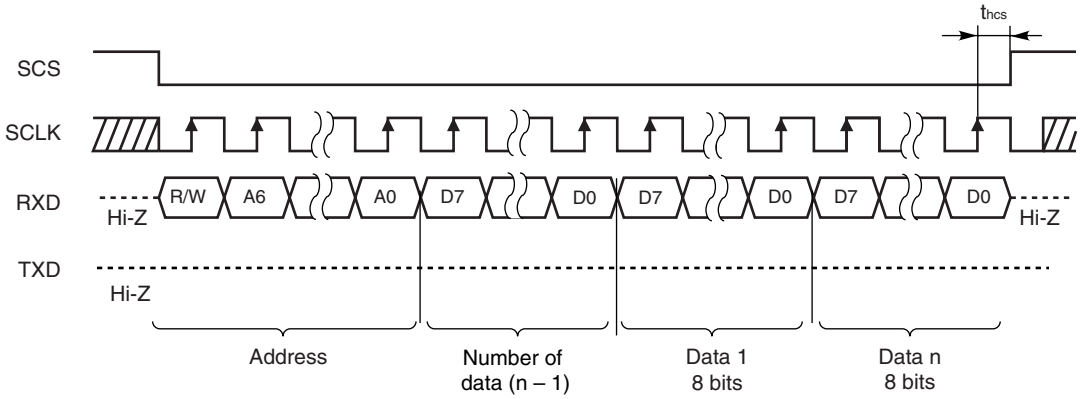
Serial interface read timing (Continuous access)



3-wire SPI mode (Format of host CPU access continuous access 2)



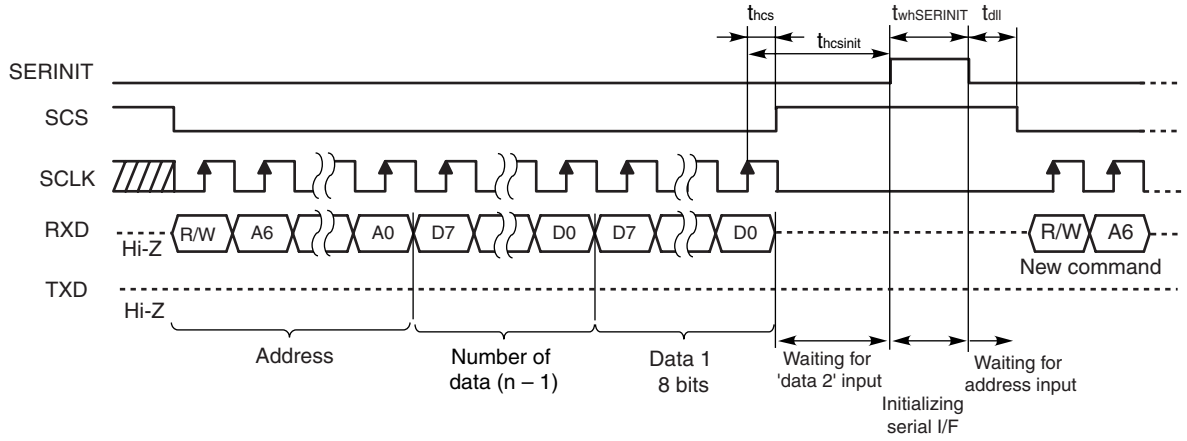
4-wire SPI mode (Format of host CPU access continuous access 2)



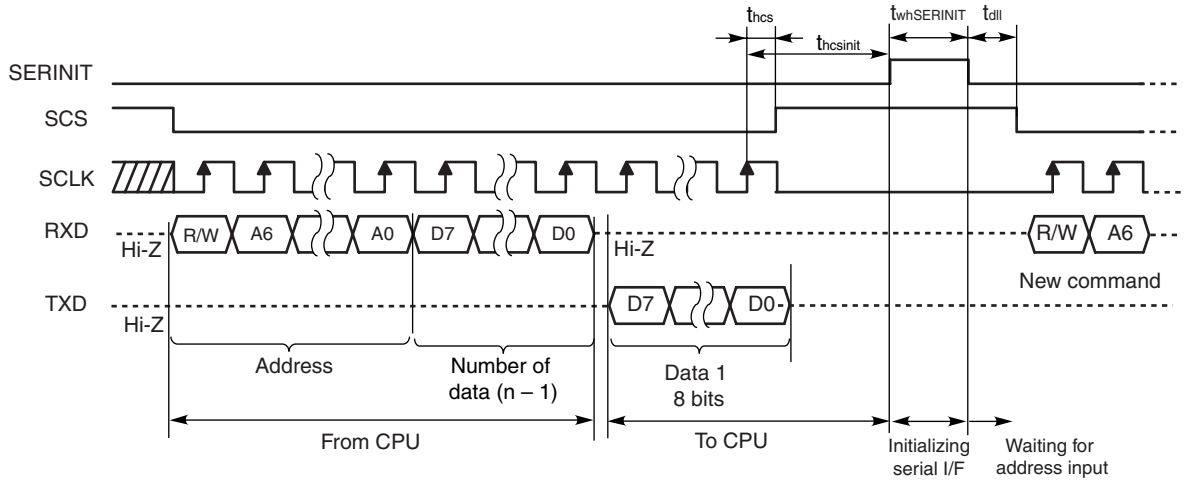
Initializing signal (SERINIT)

Canceling continuous access using SERINIT pin

Write access



Read access



13.6.4 Audio serial interface

Timing requirements

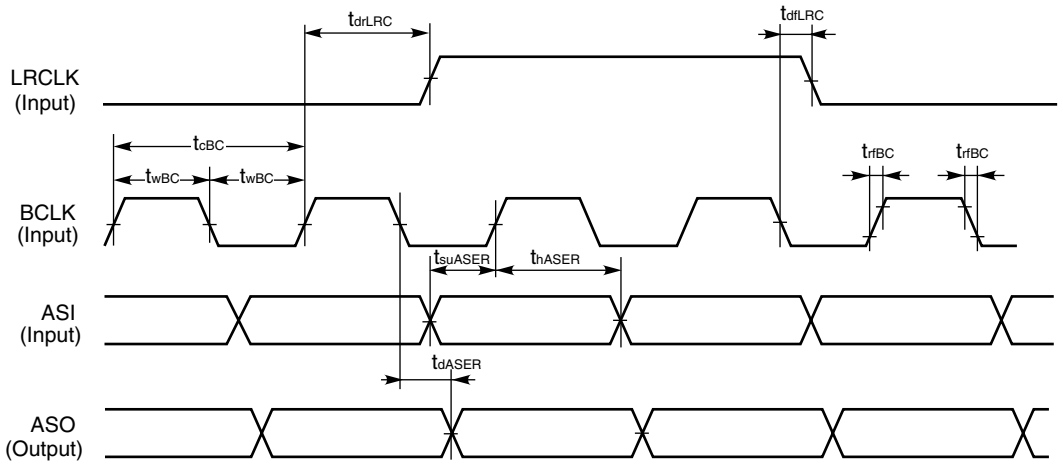
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LRCLK cycle time	t_{cLR}			1/fs		ns
BCLK cycle time	t_{cBC}	When set to 64 bits per frame[Note]		1/(fs × 64)		ns
BCLK high-/low-level width	t_{wBC}			t_{cBC}/2		ns
BCLK rise/fall time	t_{rfBC}				20	ns
LRCLK rising edge delay time	t_{drLRC}	BCLK↑	50			ns
LRCLK falling edge delay time	t_{dfLRC}	BCLK↓	50			ns
ASI input setup time	t_{suASER}	BCLK↑	50			ns
ASI input hold time	t_{hASER}	BCLK↑	50			ns

Note The configuration of each frame varies according to the settings in the BFS[4:0] bits of the SLFS register (07H).

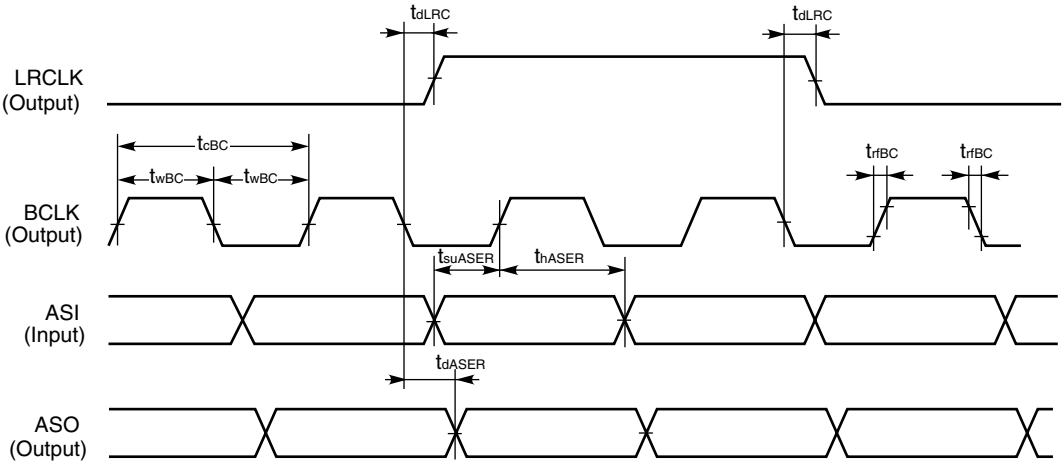
Switching characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LRCLK output delay time	t_{dLRC}	BCLK↓			50	ns
ASO output delay time	t_{dASER}	BCLK↓	–37.5		+50	ns

Audio serial I/O timing (slave mode)



Audio serial I/O timing (master mode)



13.7 Analog Characteristics

The propagation characteristics from the D/A converter to the line output are described below.
Unless otherwise specified, the following conditions must be met.

D/A converter input level INPUT = 0 dBFS (D/A converter's full scale input is defined as 0 dBFS)
D/A converter input frequency f_{IN} = 997 Hz
Measurement signal path from ASI to DAC (PLL1 ON, PLL2 OFF)
Sampling frequency fs = 48 kHz
Ambient temperature T_A = 25°C
Power supply voltage AV_{DD} = 2.7 V to 3.3 V
Output load R_L = 10 kΩ

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum output level	V_O	VOLUME = 0 dB	1.8	2.0	–	V_{p-p}
Gain error 1	GE_{max}	VOLUME = 0 dB, 0 dBr = 2.0 V_{p-p}	–1	0	+1	dBr
Gain error 2	GE_{min}	VOLUME = –45 dB, value relative to G_{Emax} reference	–47	–45	–43	dB
Gain adjustment resolution	G_{step}	VOLUME = When 0 to –45 dB, differential error	1	1.5	2	dB
THD	THD	VOLUME = 0 dB, INPUT = –3 dBFS, f = 20 Hz to 20 kHz	–	–80	–74	dB
Frequency characteristics 100 Hz to 19.2 kHz	GF	VOLUME = 0 dB, INPUT = –10 dBm@997 Hz, output when at 997 Hz is used as 0 dB reference	–1	0	+1	dB
Dynamic range	SND	VOLUME = 0 dB, INPUT = –60 dBFS, f = 20 Hz to 20 kHz, A-wgt filter	80	86	–	dB

13.8 Current Consumption

Unless otherwise specified, the following conditions must be met.

CLKIN = 13 MHz
D/A converter input level INPUT = 0 dBFS (D/A converter's full scale input is defined as 0 dBFS)
D/A converter input frequency f_{IN} = 1020 Hz
Sampling frequency fs = 32 kHz (SG), 48 kHz (Other)
Ambient temperature T_A = 25°C
Power supply voltage AV_{DD} = AV_{DD}_P = 2.7 V to 3.3 V, EV_{DD} = 1.71 V to 3.3 V, DV_{DD} = 1.425 V to 1.575 V
Output load R_L = 10 kΩ

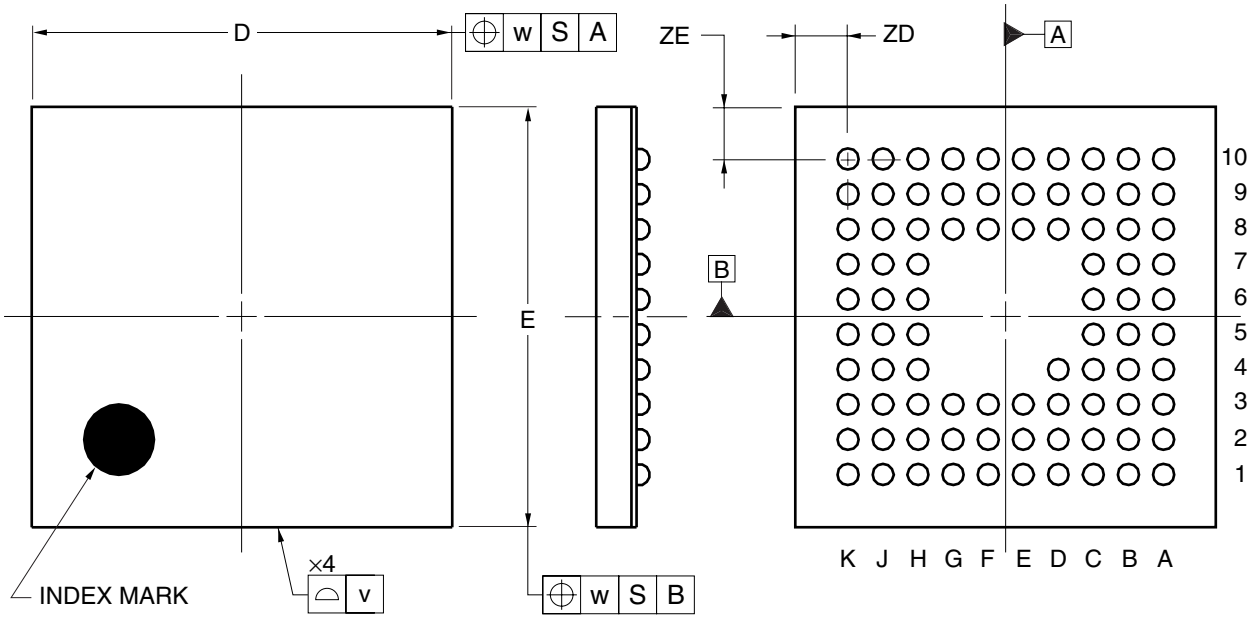
Parameter	Symbol	Conditions	Power Supply Pin	MIN.	TYP.	MAX.	Unit
Current consumption during output from SG to DAC	I_{DD1}	STDIG = STPLL2 = STPLL1 = STSYNTH = STDAC = 1, STDSP = 0, SLSORCE = 00B and SG is operating normally	DV_{DD}		35	59	mA
			AV_{DD}		7.7	16	mA
			AV_{DD}_P		4.4	8	mA
			EV_{DD} Note 1			3	mA
Current consumption during output from DSP to DAC	I_{DD2}	STDIG = STPLL2 = STPLL1 = STDSP = STDAC = 1, STSYNTH = 0, SLSORCE = 10B and DSP is operating normally	DV_{DD}		36	60	mA
			AV_{DD}		7.7	16	mA
			AV_{DD}_P		4.4	8	mA
			EV_{DD} Note 1			3	mA
Current consumption during output from ASI to DAC	I_{DD3}	STDIG = STPLL1 = STDAC = 1, SLSORCE = 01B, ASI = 1	DV_{DD}		8.5	30	mA
			AV_{DD}		7.7	16	mA
			AV_{DD}_P		1	4	mA
			EV_{DD} Note 1			3	mA
Current consumption during output from SG to ASO	I_{DD4}	STDIG = STPLL2 = STPLL1 = STSYNTH = 1, STDSP = 0, SLSORCE = 00B, ASO = 1 and SG is operating normally	DV_{DD}		35	59	mA
			AV_{DD}		2	6	mA
			AV_{DD}_P		4.4	8	mA
			EV_{DD} Note 1			5	mA
Current consumption during output from DSP to ASO	I_{DD5}	STDIG = STPLL2 = STPLL1 = STDSP = 1, STSYNTH = 0, SLSORCE = 10B, ASO = 1 and DSP is operating normally	DV_{DD}		36	60	mA
			AV_{DD}		2	6	mA
			AV_{DD}_P		4.4	8	mA
			EV_{DD} Note 1			5	mA
Current consumption during output from ASI to ASO	I_{DD6}	STDIG = STPLL1 = 1, SLSORCE = 01B, ASI = ASO =1	DV_{DD}		8.5	30	mA
			AV_{DD}		2	6	mA
			AV_{DD}_P		1.2	4	mA
			EV_{DD} Note 1			5	mA
Standby consumption current (Software power saving mode)	I_{STB}	STDIG = STPLL2 = STPLL1 = STASI = STASO = STSYNTH = STDAC = STDSP = 0	DV_{DD}		0.09	15	mA
			AV_{DD}		0.5	5	μA
			AV_{DD}_P		0.5	5	μA
			EV_{DD} Note 2		0.6	10	μA
Standby consumption current (Hardware power saving mode)	I_{HSTB}	RESET_B = 0, EVDD: ON, AVDD, AVDD_P and DVDD: OFF	EV_{DD} Note 2		0.6	10	μA

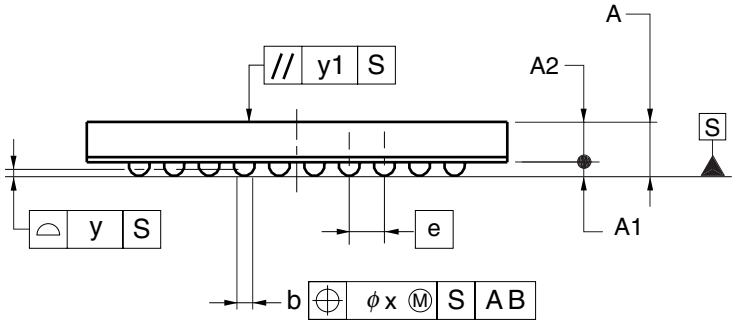
Notes 1. The EV_{DD} pin current is measured when there is no load. In the actual operation of the μPD9993, the EV_{DD} pin current differs depending on the external environment such as the clock rate, load capacitance, and load resistance.

2. Input pins: Low level or High level, Output pins: No load.

14. PACKAGE DRAWING

85-PIN TAPE FBGA (6x6)





(UNIT:mm)

ITEM	DIMENSIONS
D	6.00±0.10
E	6.00±0.10
v	0.15
w	0.20
e	0.50
A	0.83±0.10
A1	0.18±0.05
A2	0.65
b	0.32±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.75
ZE	0.75

P85F9-50-BA3

★ 15. RECOMMENDED SOLDERING CONDITIONS

The μPD9993 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

- **μPD9993F9-BA3: 85-pin tape FBGA (6 × 6)**

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 sec. max. (at 220°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after that prebaking is necessary at 125°C for 10 to 72 hours) **<Caution>** **Products packed in a medium other than a heat-resistance tray (such as a magazine, taping, and non-heat-resistance tray) cannot be baked.**	IR60-107-2

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
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