PRELIMINARY PRODUCT INFORMATION

NEC

MOS INTEGRATED CIRCUIT

μPD78F4943

16/8-BIT SINGLE-CHIP MICROCONTROLLER

The μPD78F4943 is a product of the 78K/IV series. It contains various peripheral hardware such as flash memory, RAM, I/O ports, 8-bit resolution A/D converters, timers, serial interface, and interrupt functions, as well as a high-speed, high-performance CPU.

For specific functions and other detailed information, consult the following user's manual.
This manual is required reading for design work.

μPD78F4943 Sub-Series User's Manual, Hardware : To be released soon
78K/IV Series User's Manual, Instruction : U10905E

FEATURES

- 78K/IV series
- Minimum instruction execution time: 118 ns (at 34 MHz)
- Separate bus interface
- Chip select output: 2
- Number of I/O ports: 66
- Timer/counters: 16-bit timer/counter × 3 units
  16-bit timer × 1 unit
- Synchronous serial interface: 2 channels
  Three-wire serial I/O mode : 2 channels
- Standby function
  HALT/STOP/IDLE mode
- Clock frequency division function
- Watchdog timer: 1 channel
- Clock output function
  Selectable from f_{CLK}, $f_{CLK}/2$, $f_{CLK}/4$, $f_{CLK}/8$, or $f_{CLK}/16$
- A/D converter: 8-bit resolution × 8 channels
- Supply voltage: V_{DD} = +5.0 V ±10 %

APPLICATIONS

CD-ROM

ORDERING INFORMATION

Part number	Package	Flash memory (bytes)	Internal RAM (bytes)
μPD78F4943GC-8BT	80-pin plastic QFP (14 × 14 × 1.4 mm)	56K	2048
μPD78F4943GC-3B9	80-pin plastic QFP (14 × 14 × 2.7 mm)	56K	2048

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

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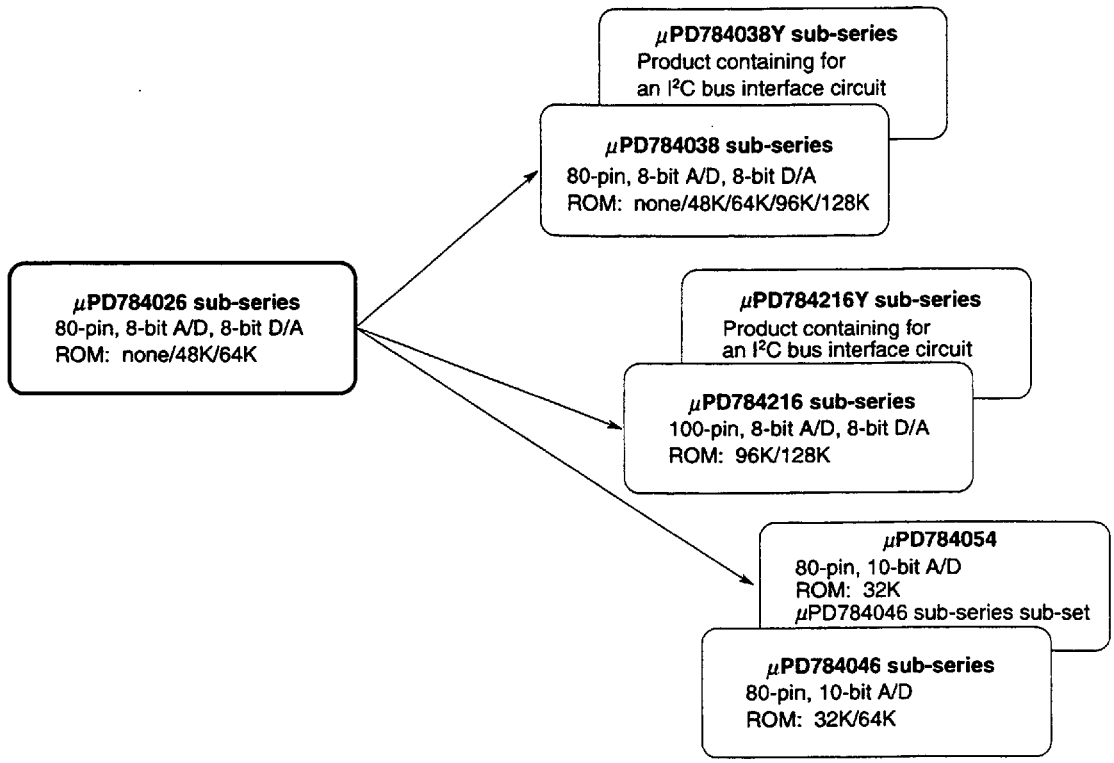
Date Published November 1996 P
Printed in Japan

78K/IV SERIES PRODUCT DEVELOPMENT DIAGRAM

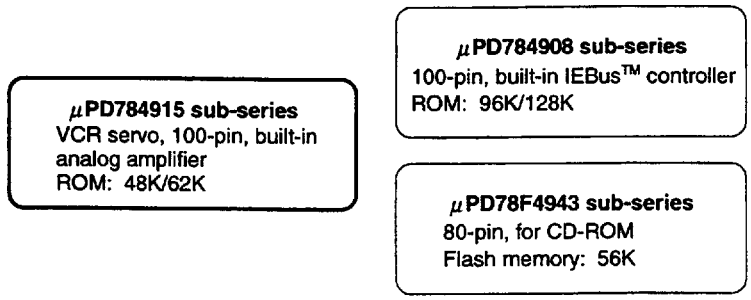
: Product under mass production

: Product under development

Standard Products Development



ASSP Development

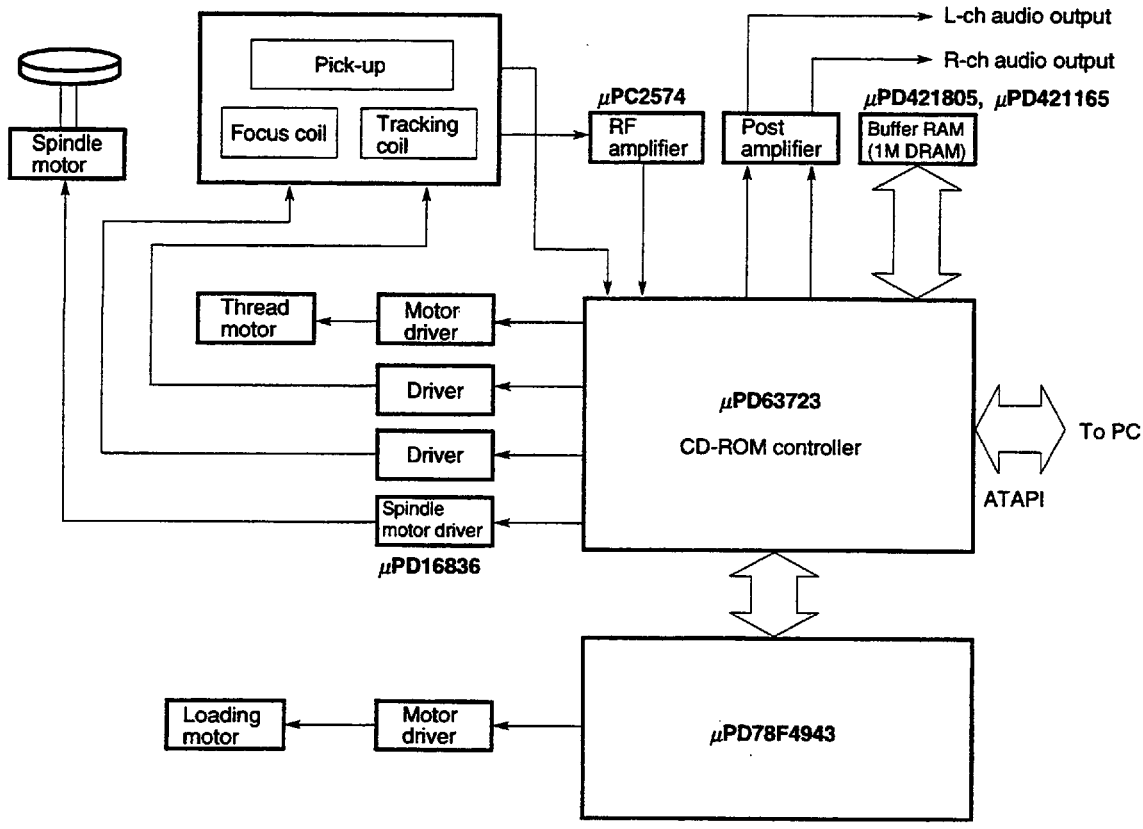


FUNCTIONS

Item		Function
Number of basic instructions (mnemonics)		113
General-purpose register		8 bits × 16 registers × 8 banks, or 16 bits × 8 registers × 8 banks (memory mapping)
Minimum instruction execution time		118 ns/235 ns/470 ns/941 ns (at 34 MHz)
Internal memory	Flash memory	56K bytes
	RAM	2048 bytes
Memory space		Program and data: 1M byte
Chip select output		2
Local bus interface		Selectable from multiplexed bus or separate bus
I/O ports	Total	66
	Input	8
	Input/output	58
Additional function pins[Note]	Pins with pull-up resistor	58
	LED direct drive outputs	4
	Transistor direct drive	12
	N-ch open-drain mode	4
Timer/counter		Timer/counter 0: (16 bits) — Timer register × 1, Capture register × 1, Compare register × 2 — Pulse output capability: • Toggle output • PWM/PPG output • One-shot pulse output
		Timer/counter 1: (8/16 bits) — Timer register × 1, Capture register × 1, Capture/compare register × 1, Compare register × 1
		Timer/counter 2: (8/16 bits) — Timer register × 1, Capture register × 1, Capture/compare register × 1, Compare register × 1 — Pulse output capability: • Toggle output • PWM/PPG output
		Timer 3 : (8/16 bits) — Timer register × 1, Compare register × 1
Synchronous serial interface		Three-wire serial I/O mode: 2 channels
A/D converter		8-bit resolution × 8 channels
Clock output		Selected from f_{CLK}, $f_{CLK}/2$, $f_{CLK}/4$, $f_{CLK}/8$, or $f_{CLK}/16$ (can be used as a 1-bit output port)
Watchdog timer		1 channel
Standby		HALT/STOP/IDLE mode
Interrupt	Hardware source	18 (11 internal, 7 external (sampling clock variable input: 1))
	Software	BRK instruction, BRKCS instruction, operand error
	Nonmaskable	1 internal, 1 external
	Maskable	10 internal, 6 external
		• 4-level programmable priority • 3 operation statuses: vectored interrupt, macro service, context switching
Supply voltage		V_{DD} = +5.0 V ±10 %
Package		80-pin plastic QFP (14 × 14 × 1.4 mm) 80-pin plastic QFP (14 × 14 × 2.7 mm)

Note Additional function pins are included in the I/O pins.

SYSTEM CONFIGURATION EXAMPLE (CD-ROM)

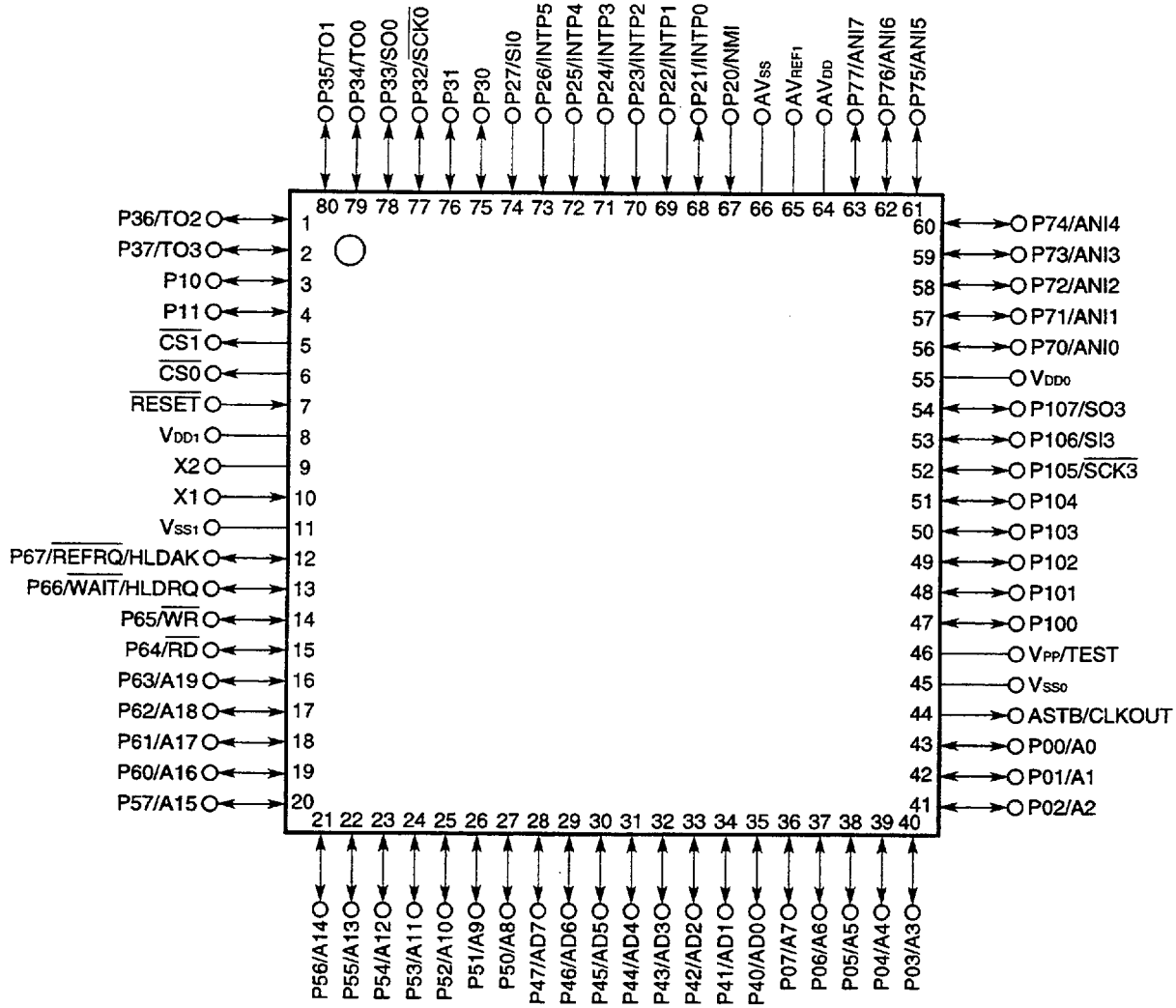


Caution The μPD78F4943, μPD421805, μPD421165, μPD16836, and μPC2574 are under development.

CONTENTS

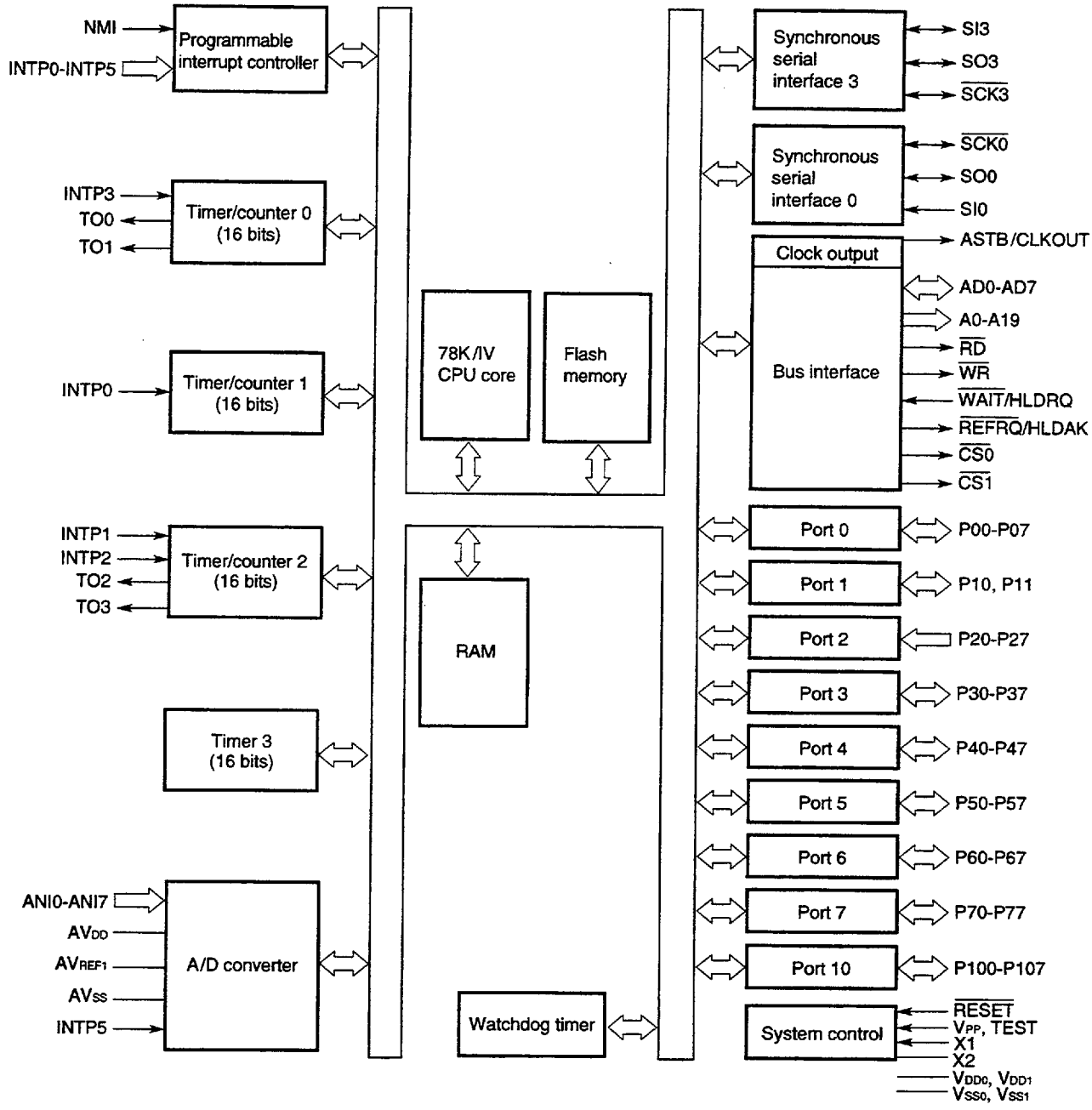
1. PIN CONFIGURATION (TOP VIEW)

- 80-pin plastic QFP (14 × 14 × 1.4 mm)
  μPD78F4943GC-8BT
- 80-pin plastic QFP (14 × 14 × 2.7 mm)
  μPD78F4943GC-3B9



A0-A19	:	Address bus	P50-P57	:	Port 5
AD0-AD7	:	Address/data bus	P60-P67	:	Port 6
ANI0-ANI7	:	Analog input	P70-P77	:	Port 7
ASTB	:	Address strobe	P100-P107	:	Port 10
AV_{DD}	:	Analog power supply	$\overline{RD}$	:	Read strobe
AV_{REF1}	:	Reference voltage	$\overline{REFRQ}$	:	Refresh request
AV_{SS}	:	Analog ground	$\overline{RESET}$	:	Reset
CLKOUT	:	Clock out	$\overline{SCK0}$, $\overline{SCK3}$	:	Serial clock
CS0, CS1	:	Chip select	SI0, SI3	:	Serial input
HLDAK	:	Hold acknowledge	SO0, SO3	:	Serial output
HLDRQ	:	Hold request	TEST	:	Test
INTP0-INTP5	:	Interrupt from peripherals	TO0-TO3	:	Timer output
NMI	:	Non-maskable interrupt	V_{DD0}, V_{DD1}	:	Power supply
P00-P07	:	Port 0	V_{PP}	:	Programming power supply
P10, P11	:	Port 1	V_{SS0}, V_{SS1}	:	Ground
P20-P27	:	Port 2	$\overline{WAIT}$	:	Wait
P30-P37	:	Port 3	$\overline{WR}$	:	Write strobe
P40-P47	:	Port 4	X1, X2	:	Crystal

2. BLOCK DIAGRAM



3. LIST OF PIN FUNCTIONS

3.1 PORT PINS (1/2)

Pin	I/O	Dual-function	Function
P00-P07	I/O	A0-A7	Port 0 (P0): • 8-bit I/O port. • Inputs and outputs can be specified bit by bit. • The use of the pull-up resistors can be specified by software for the pins in the input mode together. • Can drive a transistor.
P10	I/O	—	Port 1 (P1): • 2-bit I/O port. • Inputs and outputs can be specified bit by bit. • The use of the pull-up resistors can be specified by software for the pins in the input mode together.
P11		—	
P20	Input	NMI	Port 2 (P2): • 8-bit input-only port. • P20 does not function as a general-purpose port (nonmaskable interrupt). However, the input level can be checked by an interrupt service routine. • The use of the pull-up resistors can be specified by software for pins P22 to P27 (in units of 6 bits).
P21		INTP0	
P22		INTP1	
P23		INTP2	
P24		INTP3	
P25		INTP4	
P26		INTP5	
P27		SI0	
P30	I/O	—	Port 3 (P3): • 8-bit I/O port. • Inputs and outputs can be specified bit by bit. • The use of the pull-up resistors can be specified by software for the pins in the input mode together. • P32 and P33 can be set to the N-ch open-drain mode.
P31		—	
P32		$\overline{SCK0}$	
P33		SO0	
P34-P37		TO0-TO3	
P40-P47	I/O	AD0-AD7	Port 4 (P4): • 8-bit I/O port. • Inputs and outputs can be specified bit by bit. • The use of the pull-up resistors can be specified by software for the pins in the input mode together.
P50-P57	I/O	A8-A15	Port 5 (P5): • 8-bit I/O port. • Inputs and outputs can be specified bit by bit. • The use of the pull-up resistors can be specified by software for the pins in the input mode together.

3.1 PORT PINS (2/2)

Pin	I/O	Dual-function	Function
P60-P63	I/O	A16-A19	Port 6 (P6): • 8-bit I/O port. • Inputs and outputs can be specified bit by bit. • The use of the pull-up resistors can be specified by software for the pins in the input mode together.
P64		$\overline{RD}$	
P65		$\overline{WR}$	
P66		$\overline{WAIT}$/HLDRQ	
P67		$\overline{REFRQ}$/HLDAK	
P70-P77	I/O	ANI0-ANI7	Port 7 (P7): • 8-bit I/O port. • Inputs and outputs can be specified bit by bit.
P100-P103	I/O	—	Port 10 (P10): • 8-bit I/O port. • Inputs and outputs can be specified bit by bit. • The use of the pull-up resistors can be specified by software for the pins in the input mode together. • P100-P103 can drive LED. • P104-P107 can drive a transistor. • P105 and P107 can be set to the N-ch open-drain mode.
P104		—	
P105		$\overline{SCK3}$	
P106		SI3	
P107		SO3	

3.2 NON-PORT PINS (1/2)

Pin	I/O	Dual-function	Function	
TO0-TO3	Output	P34-P37	Timer output	
SI0	Input	P27	Serial data input (Three-wire serial I/O0)	
SI3		P106	Serial data input (Three-wire serial I/O3)	
SO0	Output	P33	Serial data output (Three-wire serial I/O0)	
SO3		P107	Serial data output (Three-wire serial I/O3)	
$\overline{SCK0}$	I/O	P32	Serial clock I/O (Three-wire serial I/O0)	
$\overline{SCK3}$		P105	Serial clock I/O (Three-wire serial I/O3)	
NMI	Input	P20	External interrupt request	—
INTP0		P21	External interrupt request	• Input of a count clock for timer/counter 1 • Capture/trigger signal for CR11 or CR12
INTP1		P22	External interrupt request	• Input of a count clock for timer/counter 2 • Capture/trigger signal for CR22
INTP2		P23	External interrupt request	• Input of a count clock for timer/counter 2 • Capture/trigger signal for CR21
INTP3		P24	External interrupt request	• Input of a count clock for timer/counter 0 • Capture/trigger signal for CR02
INTP4		P25	External interrupt request	—
INTP5		P26	External interrupt request	Input of a conversion start trigger for A/D converter
AD0-AD7	I/O	P40-P47	Time multiplexing address/data bus (for connecting external memory)	
A0-A7	I/O	P00-P07	Low-order address bus (for using separate bus)	
A8-A15	Output	P50-P57	High-order address bus (for connecting external memory)	
A16-A19		P60-P63		
$\overline{RD}$	Output	P64	Strobe signal output for reading the contents of external memory	
$\overline{WR}$	Output	P65	Strobe signal output for writing on external memory	
$\overline{WAIT}$	Input	P66/HLDRQ	Wait signal insertion	
$\overline{REFRQ}$	Output	P67/HLDAK	Refresh pulse output to external pseudo static memory	
HLDRQ	Input	P66/$\overline{WAIT}$	Input of bus hold request	
HLDAK	Output	P67/$\overline{REFRQ}$	Output of bus hold response	
ASTB	Output	CLKOUT	Latch timing output of time multiplexing address (A0-A7) (for connecting external memory)	
CLKOUT	Output	ASTB	Clock output	
$\overline{CS0}$	Output	—	Chip select output (Chip select 0)	
$\overline{CS1}$			Chip select output (Chip select 1)	
$\overline{RESET}$	Input		Chip reset	
X1	Input		Crystal input for system clock oscillation	
X2	—		(Clocks can also be input to the X1 pin.)	
ANI0-ANI7	Input	P70-P77	Analog voltage inputs for the A/D conversion	

3.2 NON-PORT PINS (2/2)

Pin	I/O	Dual-function	Function
AV_{REF1}	—	—	Application of A/D converter reference voltage
AV_{DD}			Positive power supply for the A/D converter
AV_{SS}			Ground for the A/D converter
V_{DD0}			Positive power of the port part
V_{DD1}			Positive power of other than the port part
V_{SS0}			Ground of the port part
V_{SS1}			Ground of other than the port part
TEST	Input	V_{PP}	Pin for the IC test
V_{PP}	—	TEST	Power supply at writing to the flash memory

3.3 I/O CIRCUITS FOR PINS AND HANDLING OF UNUSED PINS

Table 3-1 describes the types of I/O circuits for pins and the handling of unused pins.

Fig. 3-1 shows the configuration of these various types of I/O circuits.

Table 3-1 Types of I/O Circuits for Pins and Handling of Unused Pins (1/2)

Pin	I/O circuit type	I/O	Recommended connection method for unused pins
P00/A0-P07/A7	5-H	I/O	Input state : To be connected to V_{DD0} Output state: To be left open
P10, P11			
P20/NMI	2	Input	To be connected to V_{DD0} or V_{SS0}
P21/INTP0			
P22/INTP1	2-C		To be connected to V_{DD0}
P23/INTP2			
P24/INTP3			
P25/INTP4	8-C	I/O	Input state : To be connected to V_{DD0} Output state: To be left open
P26/INTP5	2-C	Input	To be connected to V_{DD0}
P27/SI0			
P30, P31	5-H	I/O	Input state : To be connected to V_{DD0} Output state: To be left open
P32/$\overline{SCK0}$	10-B		
P33/SO0			
P34/TO0-P37/TO3	5-H		
P40/AD0-P47/AD7			
P50/A8-P57/A15			
P60/A16-P63/A19			
P64/$\overline{RD}$			
P65/$\overline{WR}$			
P66/$\overline{WAIT}$/HLDRQ			
P67/$\overline{REFRQ}$/HLDAK			
P70/ANI0-P77/ANI7	20-A	I/O	Input state : To be connected to V_{DD0} or AVss Output state: To be left open
P100-P104	5-H		Input state : To be connected to V_{DD0} Output state: To be left open
P105/$\overline{SCK3}$	10-B		Input state : To be connected to V_{DD0} Output state: To be connected to V_{SS0} or to be left open
P106/SI3	5-H		Input state : To be connected to V_{DD0} Output state: To be left open
P107/SO3	10-B		Input state : To be connected to V_{DD0} Output state: To be connected to V_{SS0} or to be left open
ASTB/CLKOUT	4-B	Output	To be left open

Table 3-1 Types of I/O Circuits for Pins and Handling of Unused Pins (2/2)

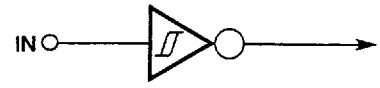
Pin	I/O circuit type	I/O	Recommended connection method for unused pins
CS0	4-B	Output	To be left open
CS1			
$\overline{\text{RESET}}$	2	Input	—
TEST/V_{PP}	—		—
AV_{REF1}	—		To be connected to V_{SS0}
AV_{SS}			
AV_{DD}			To be connected to V_{DD0}

Caution When the I/O mode of an I/O dual-function pin is unpredictable, connect the pin to V_{DD} through a resistor of 10 to 100 kilohms (particularly when the voltage of the reset input pin becomes higher than that of the low level input at power-on or when I/O is switched by software).

Remark Since type numbers are consistent in the 78K series, those numbers are not always serial in each product. (Some circuits are not included.)

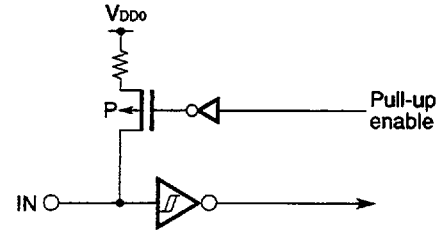
Fig. 3-1 I/O Circuits for Pins

Type 2



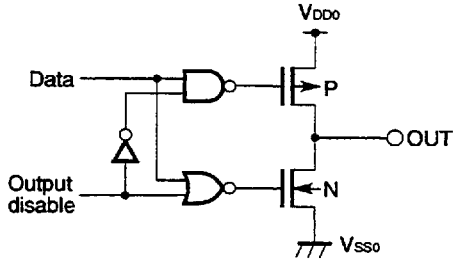
Schmitt trigger input with hysteresis characteristics

Type 2-C



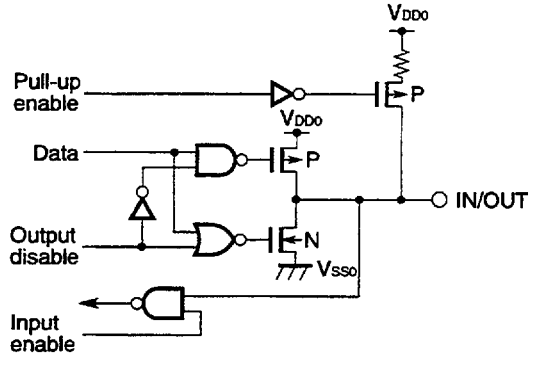
Schmitt trigger input with hysteresis characteristics

Type 4-B

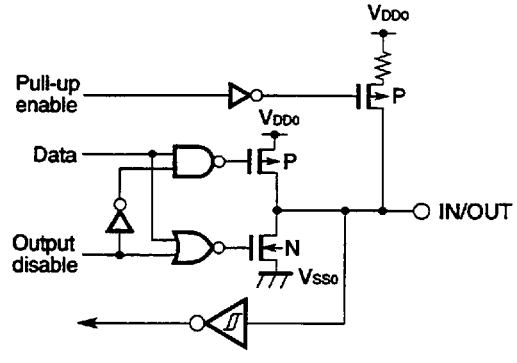


Push-pull output which can output high impedance
(both the positive and negative channels are off.)

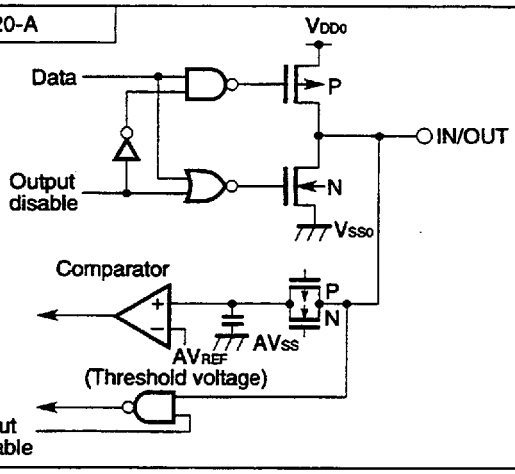
Type 5-H



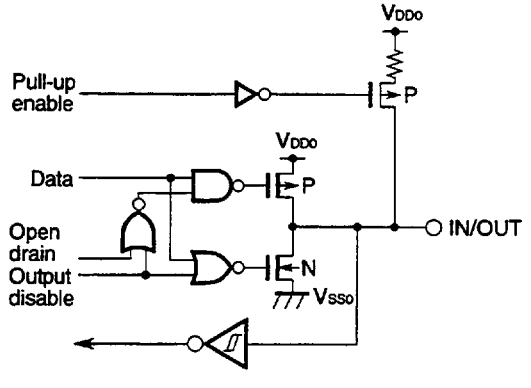
Type 8-C



Type 20-A



Type 10-B



4. CPU ARCHITECTURE

4.1 MEMORY SPACE

A 1M-byte memory space can be accessed. By using a LOCATION instruction, the mode for mapping internal data areas (special function registers and internal RAM) can be selected. A LOCATION instruction must always be executed after a reset, and can be used only once.

(1) When the LOCATION 0 instruction is executed

- **Internal memory**
  The internal data area is mapped to 0F700H-0FFFFH and the flash memory area to 00000H-0DFFFH.

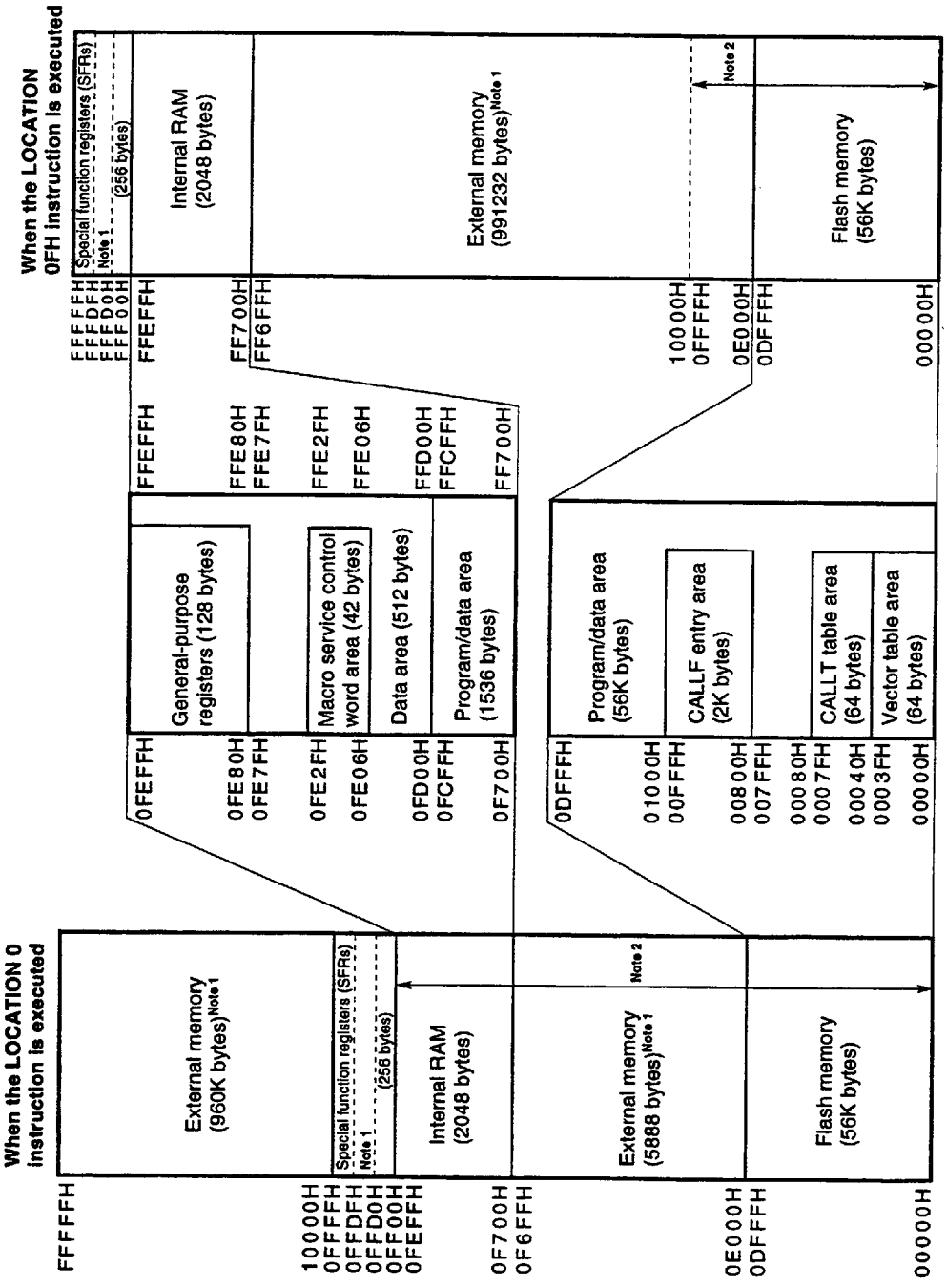
- **External memory**
  External memory is accessed in external memory expansion mode.

(2) When the LOCATION 0FH instruction is executed

- **Internal memory**
  The internal data area is mapped to FF700H-FFFFFH and the flash memory area to 00000H-0DFFFH.

- **External memory**
  External memory is accessed in external memory expansion mode.

Fig. 4-1 μPD78F4943 Memory Map



Notes 1. Accessed in external memory expansion mode.

2. Base area, or entry area based on a reset or interrupt. Internal RAM is excluded in the case of a reset.

4.2 CPU REGISTERS

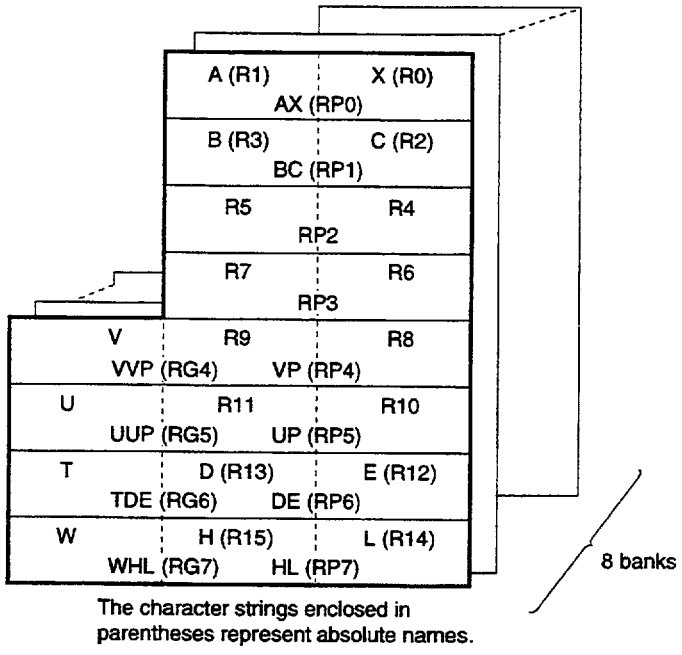
4.2.1 General-Purpose Registers

A set of general-purpose registers consists of sixteen general-purpose 8-bit registers. Two 8-bit general-purpose registers can be combined to form a 16-bit general-purpose register. Moreover, four 16-bit general-purpose registers, when combined with an 8-bit register for address extension, can be used as 24-bit address specification registers.

Eight banks of this register set are provided. The user can switch between banks by software or the context switching function.

General-purpose registers other than the V, U, T, and W registers used for address extension are mapped onto internal RAM.

Fig. 4-2 General-Purpose Register Format



The character strings enclosed in parentheses represent absolute names.

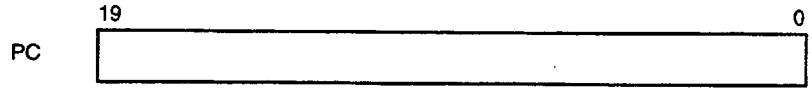
Caution By setting the RSS bit of PSW to 1, R4, R5, R6, R7, RP2, and RP3 can be used as the X, A, C, B, AX, and BC registers, respectively. However, this function must be used only when using programs for the 78K/III series.

4.2.2 Control Registers

(1) Program counter (PC)

This register is a 20-bit program counter. The program counter is automatically updated by program execution.

Fig. 4-3 Format of Program Counter (PC)



(2) Program Status Word (PSW)

This register holds the CPU state. The program status word is automatically updated by program execution.

Fig. 4-4 Format of Program Status Word (PSW)

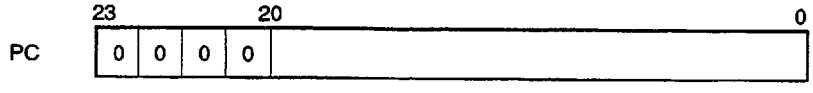
		15	14	13	12	11	10	9	8
PSW	PSWH	UF	RBS2	RBS1	RBS0	—	—	—	—
		7	6	5	4	3	2	1	0
	PSWL	S	Z	RSS[Note]	AC	IE	P/V	0	CY

Note This flag is used to maintain compatibility with the 78K/III series. This flag must be set to 0 when programs for the 78K/III series are being used.

(3) Stack pointer (SP)

This register is a 24-bit pointer for holding the start address of the stack. The 4 high-order bits must be set to 0.

Fig. 4-5 Format of Stack Pointer (SP)



4.2.3 Special Function Registers (SFRs)

The special function registers are registers with special functions such as mode registers and control registers for built-in peripheral hardware. The special function registers are mapped onto the 256-byte space between 0FF00H and 0FFFFH[Note].

Note Applicable when the LOCATION 0 instruction is executed. FFF00H-FFFFFH when the LOCATION 0FH instruction is executed.

Caution Never attempt to access addresses in this area where no SFR is allocated. Otherwise, the μPD78F4943 may be placed in the deadlock state. The deadlock state can be cleared only by a reset.

Table 4-1 lists the special function registers (SFRs). The titles of the table columns are explained below.

- Abbreviation ..... Symbol used to represent a built-in SFR. The abbreviations listed in the table are reserved words for the NEC assembler (RA78K4). The C compiler (CC78K4) allows the abbreviations to be used as sfr variables of bit type with the #pragma sfr command.
- R/W ..... Indicates whether each SFR allows read and/or write operations.
  R/W : Allows both read and write operations.
  R : Allows read operations only.
  W : Allows write operations only.
- Manipulatable bits ..... Indicates the maximum number of bits that can be manipulated whenever an SFR is manipulated. An SFR that supports 16-bit manipulation can be described in the sfrp operand. For address specification, an even-numbered address must be specified.
  An SFR that supports 1-bit manipulation can be described in a bit manipulation instruction.
- When reset ..... Indicates the state of each register when $\overline{\text{RESET}}$ is applied.

Table 4-1 Special Function Registers (SFRs) (1/3)

Address[Note]	Special function register (SFR) name	Abbreviation		R/W	Manipulatable bits			When reset
					1 bit	8 bits	16 bits	
0FF00H	Port 0	P0		R/W	○	○	–	Undefined
0FF01H	Port 1	P1			○	○	–	
0FF02H	Port 2	P2		R	○	○	–	
0FF03H	Port 3	P3		R/W	○	○	–	
0FF04H	Port 4	P4			○	○	–	
0FF05H	Port 5	P5			○	○	–	
0FF06H	Port 6	P6			○	○	–	00H
0FF07H	Port 7	P7			○	○	–	Undefined
0FF0AH	Port 10	P10			○	○	–	
0FF10H	Compare register (timer/counter 0)	CR00			–	–	○	
0FF12H	Capture/compare register (timer/counter 0)	CR01			–	–	○	
0FF14H	Compare register L (timer/counter 1)	CR10	CR10W		–	○	○	
0FF15H	Compare register H (timer/counter 1)	–			–	–		
0FF16H	Capture/compare register L (timer/counter 1)	CR11	CR11W		–	○	○	
0FF17H	Capture/compare register H (timer/counter 1)	–			–	–		
0FF18H	Compare register L (timer/counter 2)	CR20	CR20W		–	○	○	
0FF19H	Compare register H (timer/counter 2)	–			–	–		
0FF1AH	Capture/compare register L (timer/counter 2)	CR21	CR21W		–	○	○	
0FF1BH	Capture/compare register H (timer/counter 2)	–			–	–		
0FF1CH	Compare register L (timer 3)	CR30	CR30W		–	○	○	
0FF1DH	Compare register H (timer 3)	–			–	–		
0FF20H	Port 0 mode register	PM0			○	○	–	FFH
0FF21H	Port 1 mode register	PM1			○	○	–	
0FF23H	Port 3 mode register	PM3			○	○	–	
0FF24H	Port 4 mode register	PM4			○	○	–	
0FF25H	Port 5 mode register	PM5			○	○	–	
0FF26H	Port 6 mode register	PM6			○	○	–	
0FF27H	Port 7 mode register	PM7			○	○	–	
0FF2AH	Port 10 mode register	PM10			○	○	–	
0FF30H	Capture/compare control register 0	CRC0			–	○	–	10H
0FF31H	Timer output control register	TOC			○	○	–	00H
0FF32H	Capture/compare control register 1	CRC1			–	○	–	
0FF33H	Capture/compare control register 2	CRC2			–	○	–	10H
0FF36H	Capture register (timer/counter 0)	CR02		R	–	–	○	0000H
0FF38H	Capture register L (timer/counter 1)	CR12	CR12W		–	○	○	
0FF39H	Capture register H (timer/counter 1)	–			–	–		
0FF3AH	Capture register L (timer/counter 2)	CR22	CR22W		–	○	○	
0FF3BH	Capture register H (timer/counter 2)	–			–	–		
0FF43H	Port 3 mode control register	PMC3		R/W	○	○	–	00H

Note Applicable when the LOCATION 0 instruction is executed. When the LOCATION 0FH instruction is executed, F0000H is added to each address.

Table 4-1 Special Function Registers (SFRs) (2/3)

Address[Note]	Special function register (SFR) name	Abbreviation	R/W	Manipulatable bits			When reset
				1 bit	8 bits	16 bits	
0FF4AH	Port 10 mode control register	PMC10	R/W	○	○	–	00H
0FF4EH	Register L for optional pull-up resistor	PUOL		○	○	–	
0FF4FH	Register H for optional pull-up resistor	PUOH		○	○	–	
0FF50H	Timer register 0	TM0	R	–	–	○	0000H
0FF51H				–	–		
0FF52H	Timer register 1	TM1 TM1W		–	○	○	
0FF53H		–		–	–		
0FF54H	Timer register 2	TM2 TM2W		–	○	○	
0FF55H		–		–	–		
0FF56H	Timer register 3	TM3 TM3W		–	○	○	
0FF57H		–		–	–		
0FF5CH	Prescaler mode register 0	PRM0	R/W	–	○	–	11H
0FF5DH	Timer control register 0	TMC0		○	○	–	00H
0FF5EH	Prescaler mode register 1	PRM1		–	○	–	11H
0FF5FH	Timer control register 1	TMC1		○	○	–	00H
0FF68H	A/D converter mode register	ADM		○	○	–	
0FF6AH	A/D conversion result register	ADCR	R	–	○	–	Undefined
0FF7DH	One-shot pulse output control register	OSPC	R/W	○	○	–	00H
0FF80H	Synchronous serial interface mode register 3	CSIM3		○	○	–	
0FF82H	Synchronous serial interface mode register 0	CSIM0		○	○	–	
0FF86H	Serial shift register: IOE0	SIO0		–	○	–	Undefined
0FF8EH	Serial shift register: IOE3	SIO3		–	○	–	
0FFA0H	External interrupt mode register 0	INTM0		○	○	–	00H
0FFA1H	External interrupt mode register 1	INTM1		○	○	–	
0FFA8H	In-service priority register	ISPR	R	○	○	–	
0FFAAH	Interrupt mode control register	IMC	R/W	○	○	–	80H
0FFACH	Interrupt mask register 0L	MK0L MK0		○	○	○	FFFFH
0FFADH	Interrupt mask register 0H	MK0H		○	○		
0FFAEH	Interrupt mask register 1L	MK1L MK1		○	○	○	
0FFAFH	Interrupt mask register 1H	MK1H		○	○		
0FFB1H	Flash read buffer register	FLRB	R	–	○	–	Undefined
0FFB2H	Flash write buffer register	FLWB	W	–	○	–	
0FFB3H	Flash address pointer register L	FLAPL	R/W	–	○	–	00H
0FFB4H	Flash address pointer register M	FLAPM		–	○	–	
0FFB5H	Flash address pointer register H	FLAPH		–	○	–	
0FFB7H	Flash programming mode control register	FLPMC		○	○	–	08H
0FFB8H	Register 0 for specifying the chip select output space	CSA0		○	○	–	0FH
0FFB9H	Register 1 for specifying the chip select output space	CSA1		○	○	–	00H

Note Applicable when the LOCATION 0 instruction is executed. When the LOCATION 0FH instruction is executed, F0000H is added to each address.

Table 4-1 Special Function Registers (SFRs) (3/3)

Address[Note 1]	Special function register (SFR) name	Abbreviation	R/W	Manipulatable bits			When reset
				1 bit	8 bits	16 bits	
0FFC0H	Standby control register	STBC	R/W	–	○[Note 2]	–	30H
0FFC2H	Watchdog timer mode register	WDM		–	○[Note 2]	–	00H
0FFC3H	External bus type select register	EBTS		○	○	–	
0FFC4H	Memory expansion mode register	MM		○	○	–	20H
0FFC5H	Hold mode register	HLDM		○	○	–	00H
0FFC6H	Clock output mode register	CLOM		○	○	–	
0FFC7H	Programmable wait control register 1	PWC1		–	○	–	AAH
0FFC8H	Programmable wait control register 2	PWC2		–	–	○	AAAAH
0FFCCH	Refresh mode register	RFM		○	○	–	00H
0FFCDH	Refresh area specification register	RFA		○	○	–	
0FFCFH	Oscillation settling time specification register	OSTS		–	○	–	
0FFD0H-0FFDFH	External SFR area	–		○	○	–	–
0FFE0H	Interrupt control register (INTP0)	PIC0		○	○	–	43H
0FFE1H	Interrupt control register (INTP1)	PIC1		○	○	–	
0FFE2H	Interrupt control register (INTP2)	PIC2		○	○	–	
0FFE3H	Interrupt control register (INTP3)	PIC3		○	○	–	
0FFE4H	Interrupt control register (INTC00)	CIC00		○	○	–	
0FFE5H	Interrupt control register (INTC01)	CIC01		○	○	–	
0FFE6H	Interrupt control register (INTC10)	CIC10		○	○	–	
0FFE7H	Interrupt control register (INTC11)	CIC11		○	○	–	
0FFE8H	Interrupt control register (INTC20)	CIC20		○	○	–	
0FFE9H	Interrupt control register (INTC21)	CIC21		○	○	–	
0FFEAH	Interrupt control register (INTC30)	CIC30		○	○	–	
0FFEBH	Interrupt control register (INTP4)	PIC4		○	○	–	
0FFECH	Interrupt control register (INTP5)	PIC5		○	○	–	
0FFEDH	Interrupt control register (INTAD)	ADIC		○	○	–	
0FFF1H	Interrupt control register (INTCSI0)	CSIIC0		○	○	–	
0FFF9H	Interrupt control register (INTCSI3)	CSIIC3		○	○	–	

Notes 1. Applicable when the LOCATION 0 instruction is executed. When the LOCATION 0FH instruction is executed, F0000H is added to each address.

2. A write operation can be performed only with special instructions MOV STBC,#byte and MOV WDM,#byte. Other instructions cannot perform a write operation.

5. FLASH MEMORY

The 56K-byte flash memory is incorporated.

This flash memory can be cleared or written by the dedicated writer and modified by the program.

A +10 V power supply is needed to modify the flash memory (see **Fig. 5-1**). The boot area is provided in the flash memory to store the program to modify the flash memory. The area cannot be cleared by the program. The size of the area can be selected from 4K, 8K, or 12K bytes by the software (see **Fig. 5-2**).

Fig. 5-1 Circuit for Modifying the Flash Memory

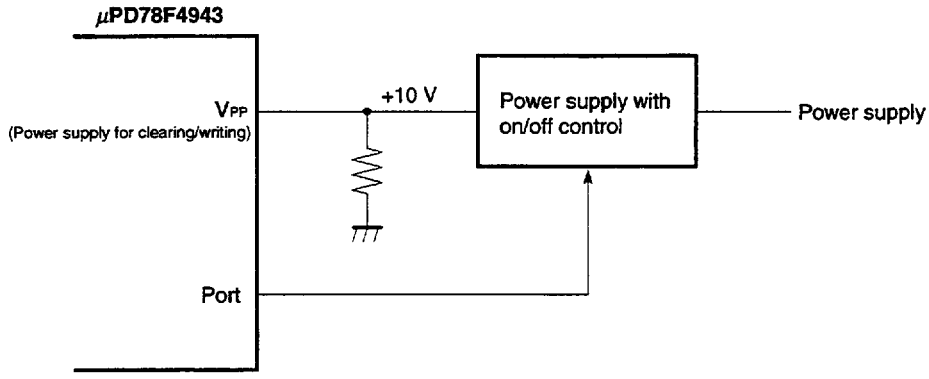
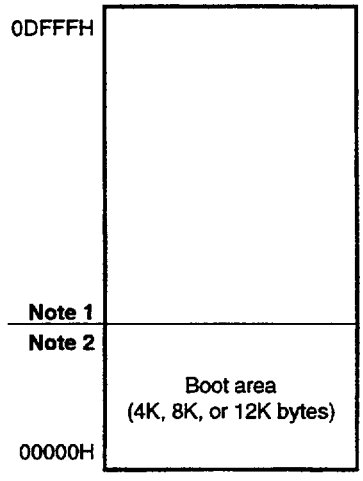


Fig. 5-2 Boot Area



Notes 1. 3000H/2000H/1000H
2. 2FFFH/1FFFH/0FFFH

6. PERIPHERAL HARDWARE FUNCTIONS

6.1 PORTS

The ports shown in Fig. 6-1 are provided to enable the application of wide-ranging control. Table 6-1 lists the functions of the ports. For the inputs to port 0 to port 6 and port 10, a built-in pull-up resistor can be specified by software.

Fig. 6-1 Port Configuration

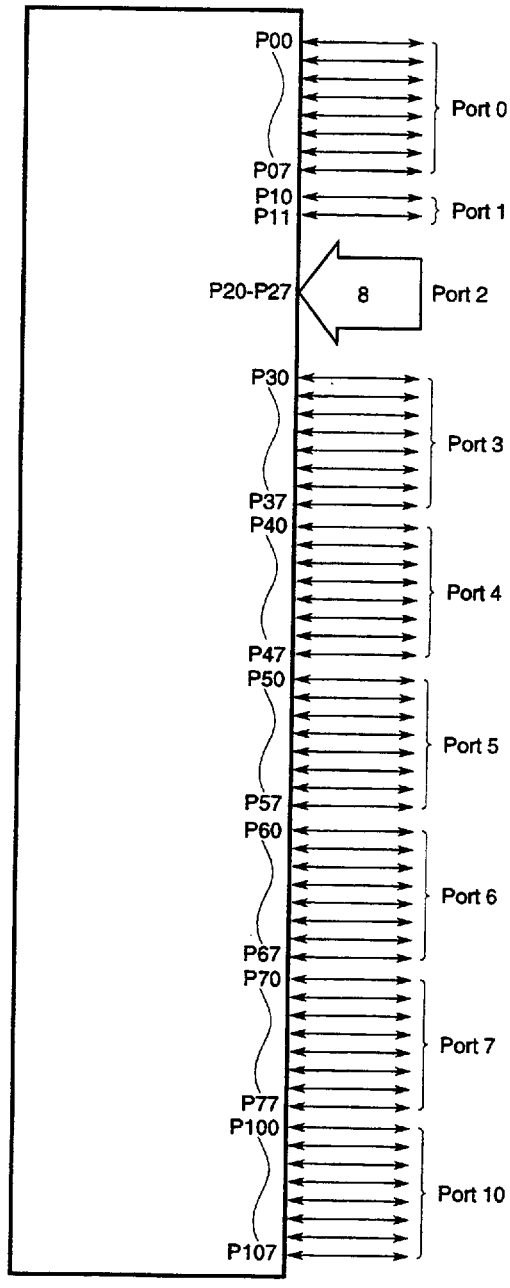


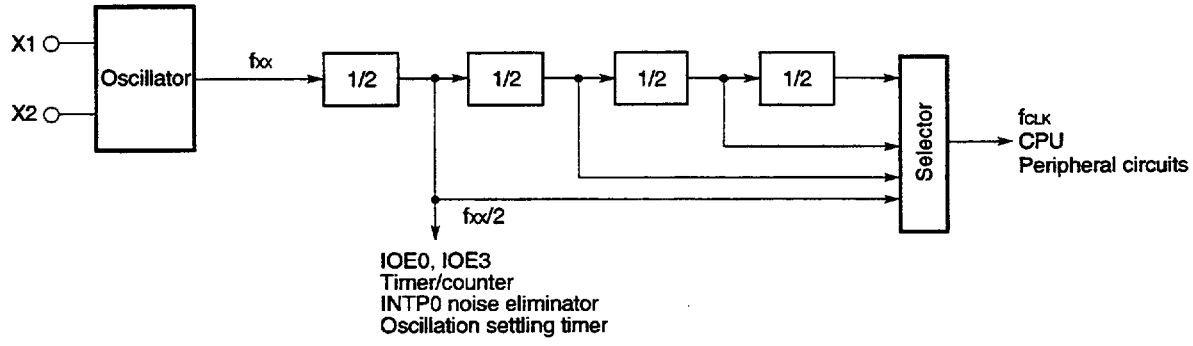
Table 6-1 Port Functions

Port name	Pin	Function	Pull-up specification by software
Port 0	P00-P07	• Bit-by-bit input/output setting supported • Capable of driving transistors	Specified as a batch for all pins placed in input mode.
Port 1	P10, P11	• Bit-by-bit input/output setting supported	Specified as a batch for all pins placed in input mode.
Port 2	P20-P27	• Input port	Specified for the 6 bits (P22-P27) as a batch.
Port 3	P30-P37	• Bit-by-bit input/output setting supported • P32 and P33 can be set to the N-ch open-drain mode.	Specified as a batch for all pins placed in input mode.
Port 4	P40-P47	• Bit-by-bit input/output setting supported	Specified as a batch for all pins placed in input mode.
Port 5	P50-P57	• Bit-by-bit input/output setting supported	Specified as a batch for all pins placed in input mode.
Port 6	P60-P67	• Bit-by-bit input/output setting supported	Specified as a batch for all pins placed in input mode.
Port 7	P70-P77	• Bit-by-bit input/output setting supported	—
Port 10	P100-P107	• Bit-by-bit input/output setting supported • Capable of driving LEDs for P100-P103 • Capable of driving transistors for P104-P107 • P105 and P107 can be set to the N-ch open-drain mode.	Specified as a batch for all pins placed in input mode.

6.2 CLOCK GENERATOR

A circuit for generating the clock signal required for operation is provided. The clock generator includes a frequency divider; low current consumption can be achieved by operating at a lower internal frequency when high-speed operation is not necessary.

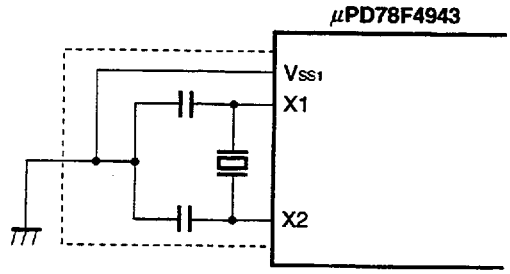
Fig. 6-2 Block Diagram of Clock Generator



Remark fxx : Oscillator frequency or external clock input
fCLK: Internal operating frequency

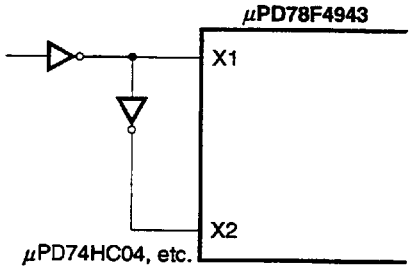
Fig. 6-3 Examples of Using Oscillator

(1) Crystal/ceramic oscillation

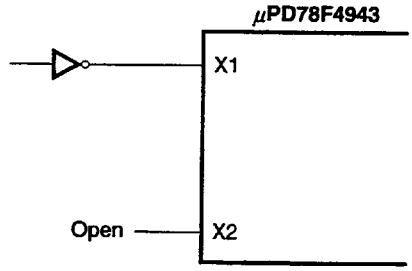


(2) External clock

- When EXTC bit of OSTS = 1



- When EXTC bit of OSTS = 0



Caution When using the clock generator, to avoid problems caused by influences such as stray capacitance, run all wiring within the area indicated by the dotted lines according to the following rules:

- Minimize the wiring length.
- Wires must never cross other signal lines.
- Wires must never run near a line carrying a large varying current.
- The grounding point of the capacitor of the oscillator circuit must always be at the same potential as VSS1. Never connect the capacitor to a ground pattern carrying a large current.
- Never extract a signal from the oscillator circuit.

6.3 TIMERS/COUNTERS

Three timer/counter units and one timer unit are incorporated.

Moreover, seven interrupt requests are supported, allowing these units to function as seven timer/counter units.

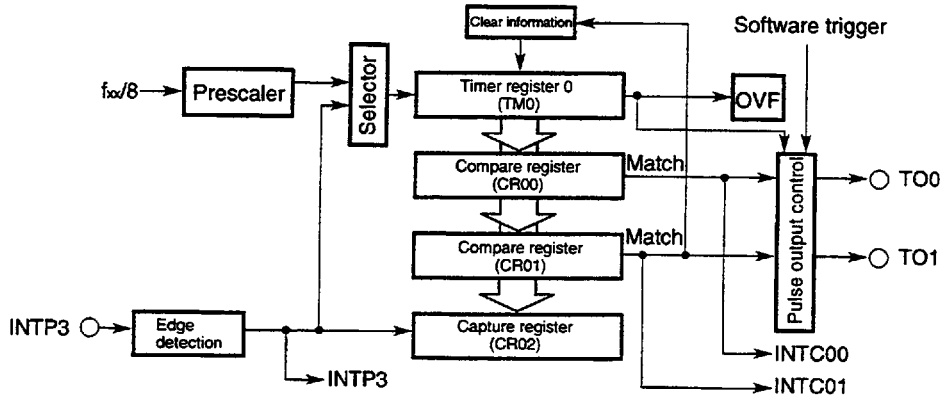
Table 6-2 Timer/Counter Operation

Item \ Name		Timer/counter 0	Timer/counter 1	Timer/counter 2	Timer 3
Count pulse width	8 bits	–	○	○	○
	16 bits	○	○	○	○
Operating mode	Interval timer	2ch	2ch	2ch	1ch
	External event counter	○	○	○	–
	One-shot timer	–	–	○	–
Function	Timer output	2ch	–	2ch	–
	Toggle output	○	–	○	–
	PWM/PPG output	○	–	○	–
	One-shot pulse output[Note]	○	–	–	–
	Pulse width measurement	1 input	1 input	2 inputs	–
	Number of interrupt requests	2	2	2	1

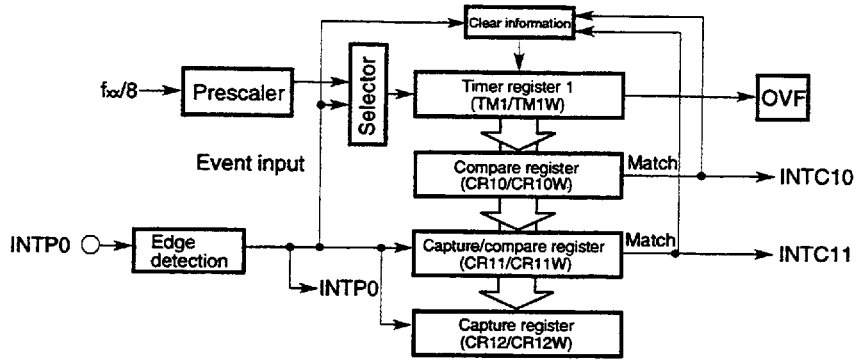
Note The one-shot pulse output function makes the level of a pulse output active by software, and makes the level of a pulse output inactive by hardware (interrupt request signal).
Note that this function differs from the one-shot timer function of timer/counter 2.

Fig. 6-4 Timer/Counter Block Diagram

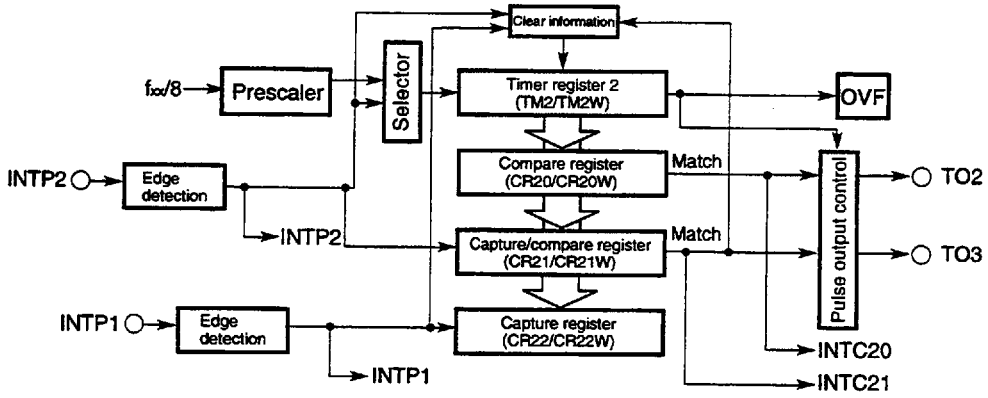
Timer/counter 0



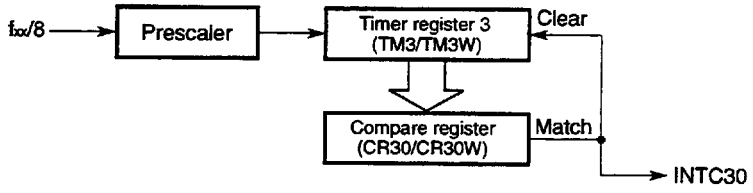
Timer/counter 1



Timer/counter 2



Timer 3



Remark OVF: Overflow flag

6.4 A/D CONVERTER

An analog/digital (A/D) converter having 8 multiplexed analog inputs (ANI0-ANI7) is incorporated.

The successive approximation system is used for conversion. The result of conversion is held in the 8-bit A/D conversion result register (ADCR). Thus, speedy high-precision conversion can be achieved. (The conversion time is about 7 μs at f_{CLK} = 17 MHz.)

A/D conversion can be started in any of the following modes:

- Hardware start: Conversion is started by means of trigger input (INTP5).
- Software start : Conversion is started by means of bit setting the A/D converter mode register (ADM).

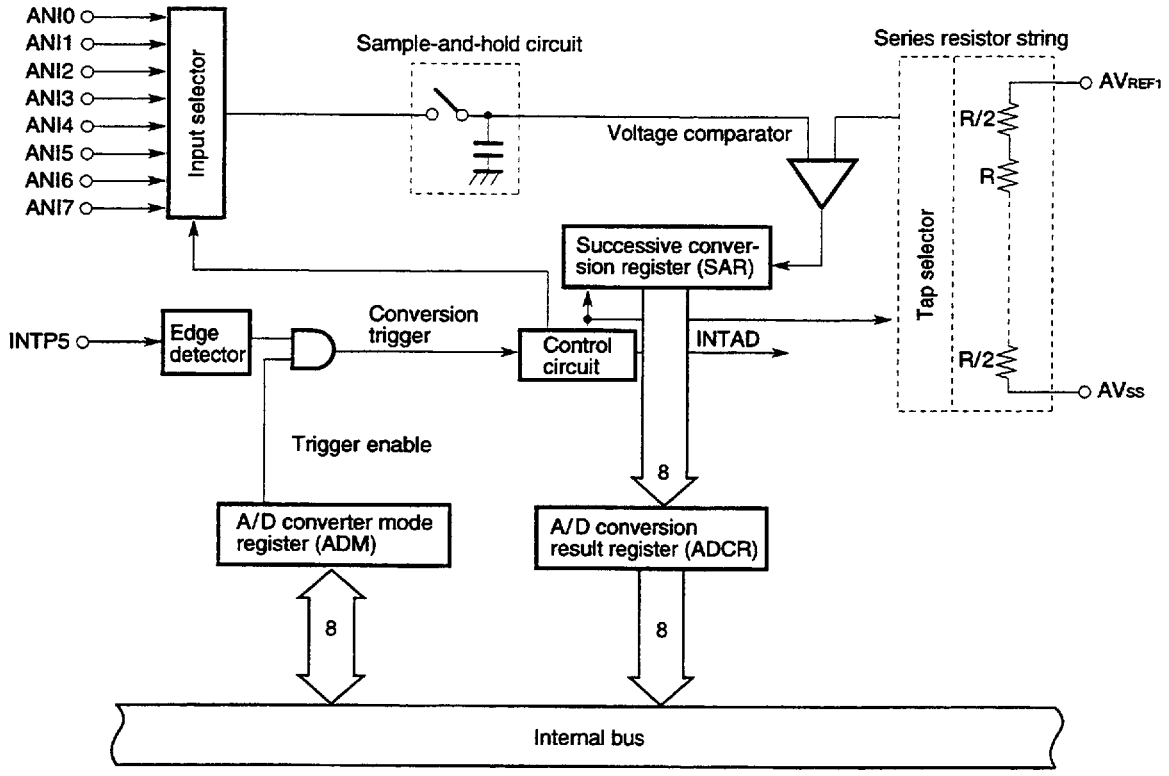
After conversion has started, one of the following modes can be selected:

- Scan mode : Multiple analog inputs are selected sequentially to obtain conversion data from all pins.
- Select mode: A single analog input is selected at all times to enable conversion data to be obtained continuously.

ADM is used to specify the above modes, as well as the termination of conversion.

When the result of conversion is transferred to ADCR, an interrupt request (INTAD) is generated. Using this feature, the results of conversion can be continuously transferred to memory by the macro service.

Fig. 6-5 Block Diagram of A/D Converter

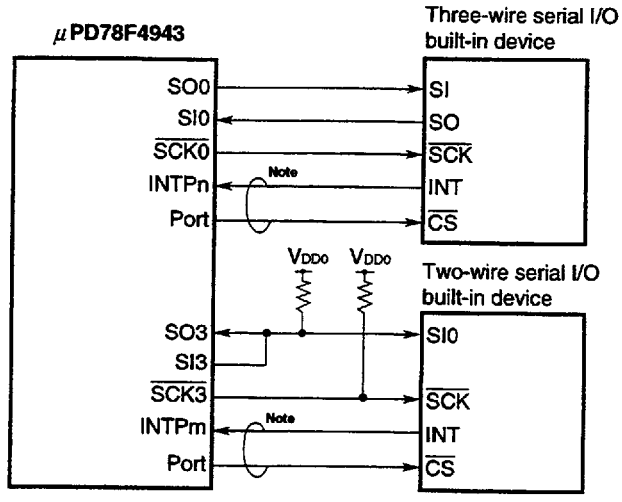


6.5 SYNCHRONOUS SERIAL INTERFACE

Two independent synchronous serial interface channels (three-wire serial I/O mode: IOE0, IOE3) are incorporated.

So, communication with points external to the system and local communication within the system can be performed at the same time. (See **Fig. 6-6**.)

Fig. 6-6 Example of Serial Interfaces



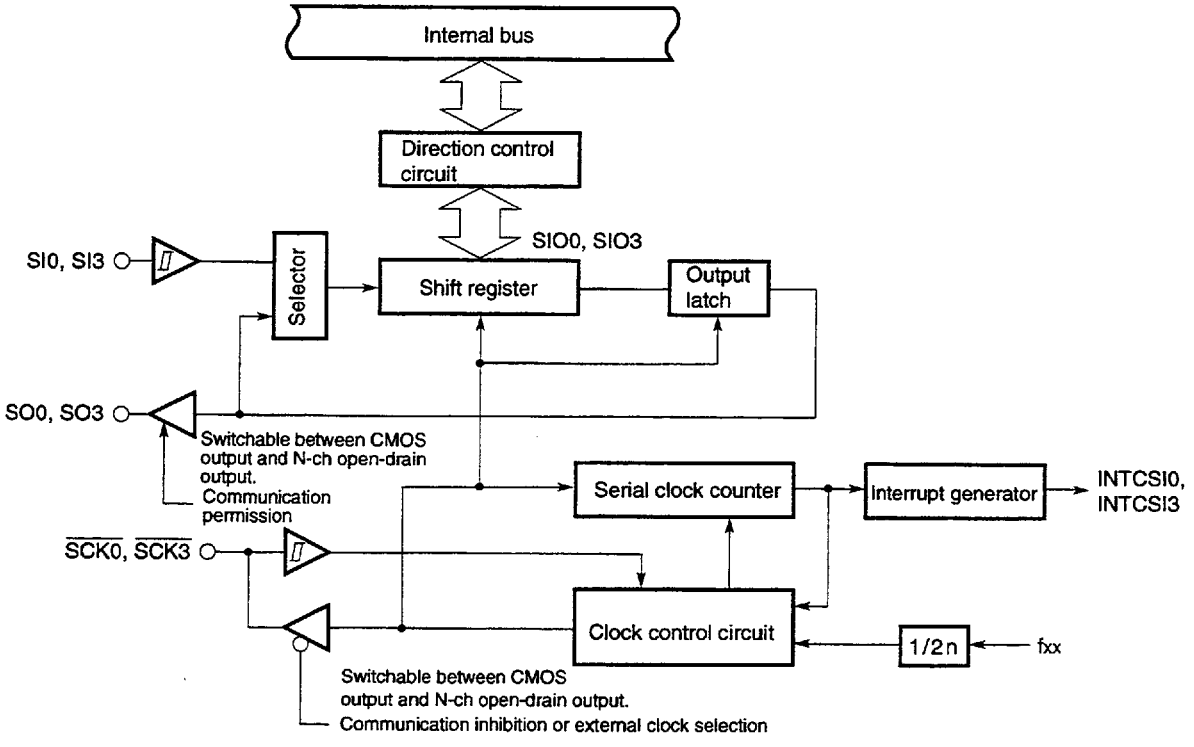
Note Handshake line

In the three-wire serial I/O mode, the master device makes the serial clock active to start transmission, then transfers 1-byte data in phase with the clock.

This mode is designed for communication with a device incorporating a conventional synchronous serial interface. Basically, three lines are used for communication: the serial clock line ($\overline{SCK}$) and the two serial data lines (SI and SO). Both $\overline{SCK}$ and SO can switch between the CMOS output and the N-ch open-drain output.

In general, a handshake line is required to check the state of reception.

Fig. 6-7 Block Diagram of Three-Wire Serial I/O Mode



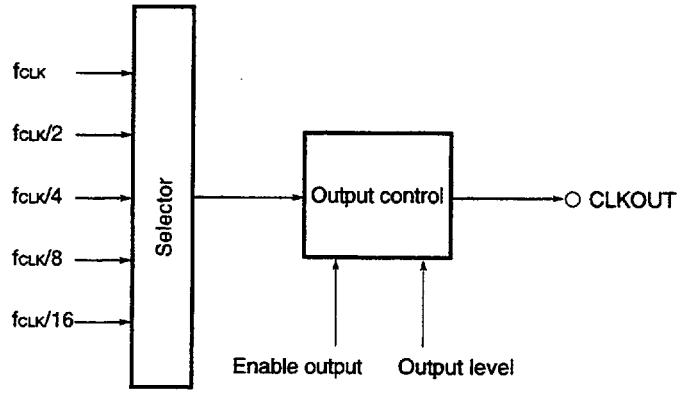
Remark fxx: Oscillator frequency or external clock input
n = 3 to 8

6.6 CLOCK OUTPUT FUNCTION

The frequency of the CPU clock signal can be divided for output to a point external to the system. Moreover, the port can be used as a 1-bit port.

The ASTB pin is also used for the CLKOUT pin, so that when this function is used, the local bus interface cannot be used.

Fig. 6-8 Block Diagram of Clock Output Function



6.7 EDGE DETECTION FUNCTION

The interrupt input pins (NMI, INTP0-INTP5) are used to apply not only interrupt requests but also trigger signals for the built-in circuits. As these pins are triggered by an edge (rising or falling) of an input signal, a function for edge detection is incorporated. Moreover, a noise suppression function is provided to prevent erroneous edge detection caused by noise.

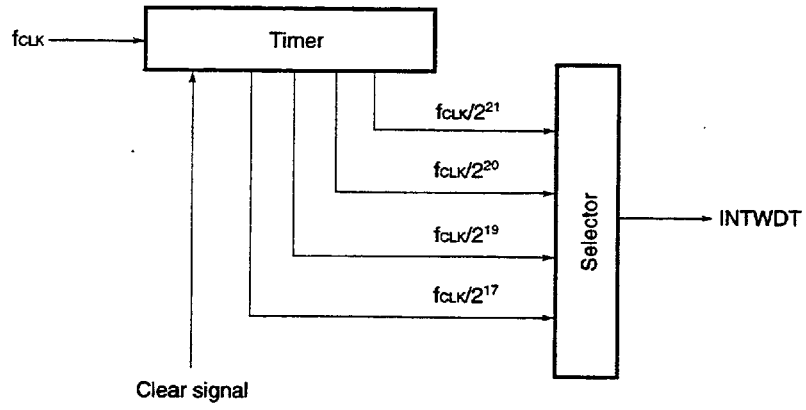
Pin	Detectable edge	Noise suppression method
NMI	Rising edge or falling edge	Analog delay
INTP0-INTP3	Rising edge or falling edge, or both edges	Clock sampling[Note]
INTP4, INTP5		Analog delay

Note INTP0 is used for sampling clock selection.

6.8 WATCHDOG TIMER

A watchdog timer is incorporated for CPU runaway detection. The watchdog timer, if not cleared by software within a specified interval, generates a nonmaskable interrupt. Furthermore, once watchdog timer operation is enabled, it cannot be disabled by software. The user can specify whether priority is placed on an interrupt based on the watchdog timer or on an interrupt based on the NMI pin.

Fig. 6-9 Block Diagram of Watchdog Timer



7. INTERRUPT FUNCTION

Table 7-1 lists the interrupt request handling modes. These modes are selected by software.

Table 7-1 Interrupt Request Handling Modes

Handling mode	Handled by	Handling	PC and PSW contents
Vectored interrupt	Software	Branches to a handling routine for execution (arbitrary handling).	The PC and PSW contents are pushed to and popped from the stack.
Context switching		Automatically selects a register bank, and branches to a handling routine for execution (arbitrary handling).	The PC and PSW contents are saved to and read from a fixed area in the register bank.
Macro service	Firmware	Performs operations such as memory-to-I/O-device data transfer (fixed handling).	Maintained

7.1 INTERRUPT SOURCE

An interrupt can be issued from any one of the interrupt sources listed in Table 7-2: execution of BRK and BRKCS instructions, an operand error, or any of the 18 other interrupt sources.

Four levels of interrupt handling priority can be set. Priority levels can be set to nest control during interrupt handling or to concurrently generate interrupt requests. Nested macro services, however, are performed without suspension.

When interrupt requests having the same priority level are generated, they are handled according to the default priority (fixed). (See **Table 7-2.**)

Table 7-2 Interrupt Sources

Type	Default priority	Source		Internal/ external	Macro service
		Name	Trigger		
Software	–	BRK instruction	Instruction execution	–	–
		BRKCS instruction			
		Operand error	When the MOV STBC,#byte, MOV WDM,#byte, or LOCATION instruction is executed, exclusive OR of the byte operand and $\overline{byte}$ does not produce FFH.		
Nonmaskable	–	NMI	Detection of edge input on the pin	External	–
		WDT	Watchdog timer overflow	Internal	
Maskable	0 (highest)	INTP0	Detection of edge input on the pin (TM1/TM1W capture trigger, TM1/TM1W event counter input)	External	Enabled
	1	INTP1	Detection of edge input on the pin (TM2/TM2W capture trigger, TM2/TM2W event counter input)		
	2	INTP2	Detection of edge input on the pin (TM2/TM2W capture trigger, TM2/TM2W event counter input)		
	3	INTP3	Detection of edge input on the pin (TM0 capture trigger, TM0 event counter input)		
	4	INTC00	TM0-CR00 match signal issued	Internal	Enabled
	5	INTC01	TM0-CR01 match signal issued		
	6	INTC10	TM1-CR10 match signal issued (in 8-bit operation mode) TM1W-CR10W match signal issued (in 16-bit operation mode)		
	7	INTC11	TM1-CR11 match signal issued (in 8-bit operation mode) TM1W-CR11W match signal issued (in 16-bit operation mode)		
	8	INTC20	TM2-CR20 match signal issued (in 8-bit operation mode) TM2W-CR20W match signal issued (in 16-bit operation mode)		
	9	INTC21	TM2-CR21 match signal issued (in 8-bit operation mode) TM2W-CR21W match signal issued (in 16-bit operation mode)		
	10	INTC30	TM3-CR30 match signal issued (in 8-bit operation mode) TM3W-CR30W match signal issued (in 16-bit operation mode)		
	11	INTP4	Detection of edge input on the pin	External	Enabled
	12	INTP5	Detection of edge input on the pin		
	13	INTAD	A/D converter processing completed (ADCR transfer)	Internal	Enabled
	14	INTCSI0	CSI0 transfer completed		
	15 (lowest)	INTCSI3	CSI3 transfer completed		

Remark CSI: Synchronous serial interface

7.2 VECTORED INTERRUPT

When a branch to an interrupt handling routine occurs, the vector table address corresponding to the interrupt source is used as the branch address.

Interrupt handling by the CPU consists of the following operations:

- When a branch occurs : Save the CPU status (PC and PSW contents) to the stack.
- When control is returned: Restore the CPU status (PC and PSW contents) from the stack.

To return control from the handling routine to the main routine, use the RETI instruction. The branch destination addresses must be within the range of 0 to FFFFH.

Table 7-3 Vector Table Address

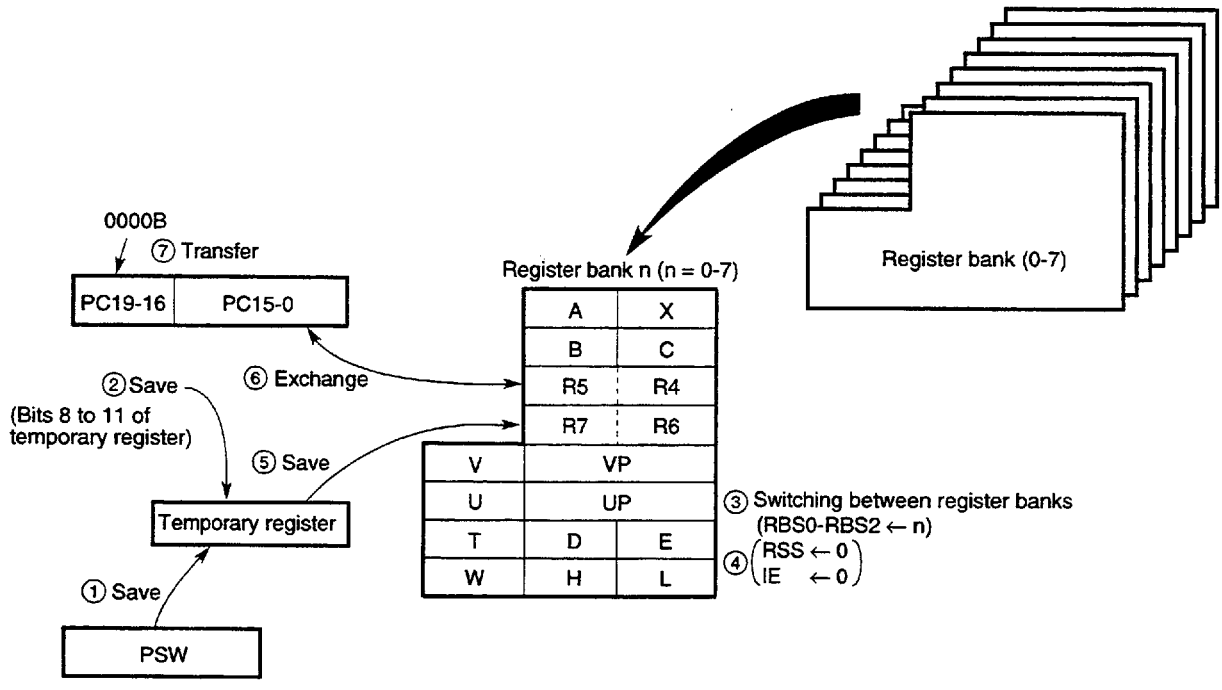
Interrupt source	Vector table address
BRK instruction	003EH
Operand error	003CH
NMI	0002H
WDT	0004H
INTP0	0006H
INTP1	0008H
INTP2	000AH
INTP3	000CH
INTC00	000EH
INTC01	0010H
INTC10	0012H
INTC11	0014H
INTC20	0016H
INTC21	0018H
INTC30	001AH
INTP4	001CH
INTP5	001EH
INTAD	0020H
INTCSI0	0028H
INTCSI3	0038H

7.3 CONTEXT SWITCHING

When an interrupt request is generated, or when the BRKCS instruction is executed, an appropriate register bank is selected by the hardware. Then, a branch to a vector address stored in that register bank occurs. At the same time, the contents of the current program counter (PC) and program status word (PSW) are stacked in the register bank.

The branch address must be within the range of 0 to FFFFH.

Fig. 7-1 Context Switching Caused by an Interrupt Request

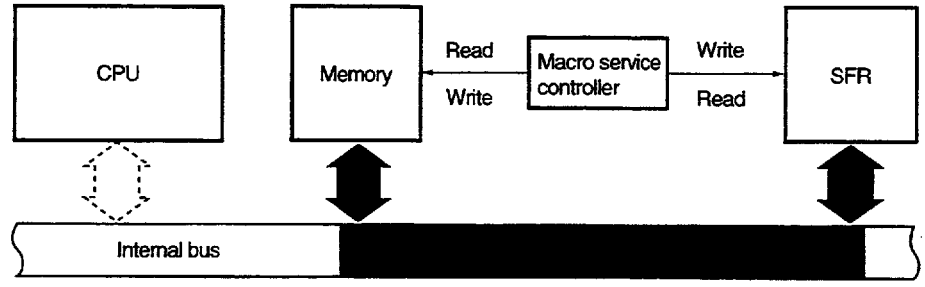


7.4 MACRO SERVICE

The macro service function enables data transfer between memory and special function registers (SFRs) without requiring the intervention of the CPU. The macro service controller accesses both memory and SFRs within the same transfer cycle to directly transfer data without having to perform data fetch.

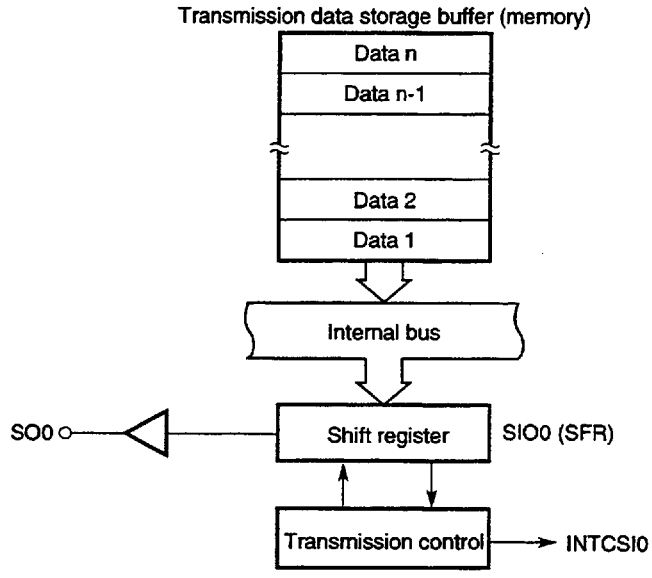
Since the CPU status is neither saved nor restored, nor is data fetch performed, high-speed data transfer is possible.

Fig. 7-2 Macro Service



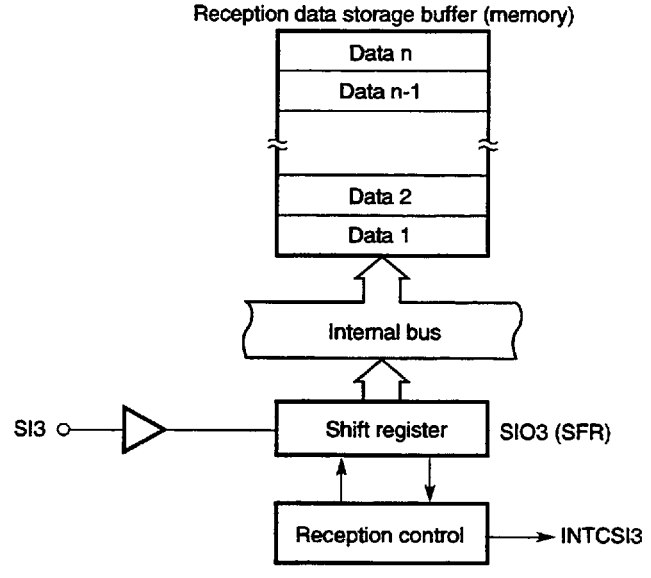
7.5 EXAMPLES OF MACRO SERVICE APPLICATIONS

(1) Serial interface transmission



Each time macro service request (INTCSI0) is generated, the next transmission data is transferred from memory to SIO0. When data n (last byte) has been transferred to SO0 (that is, once the transmission data storage buffer becomes empty), vectored interrupt request INTCSI0 is generated.

(2) Serial interface reception

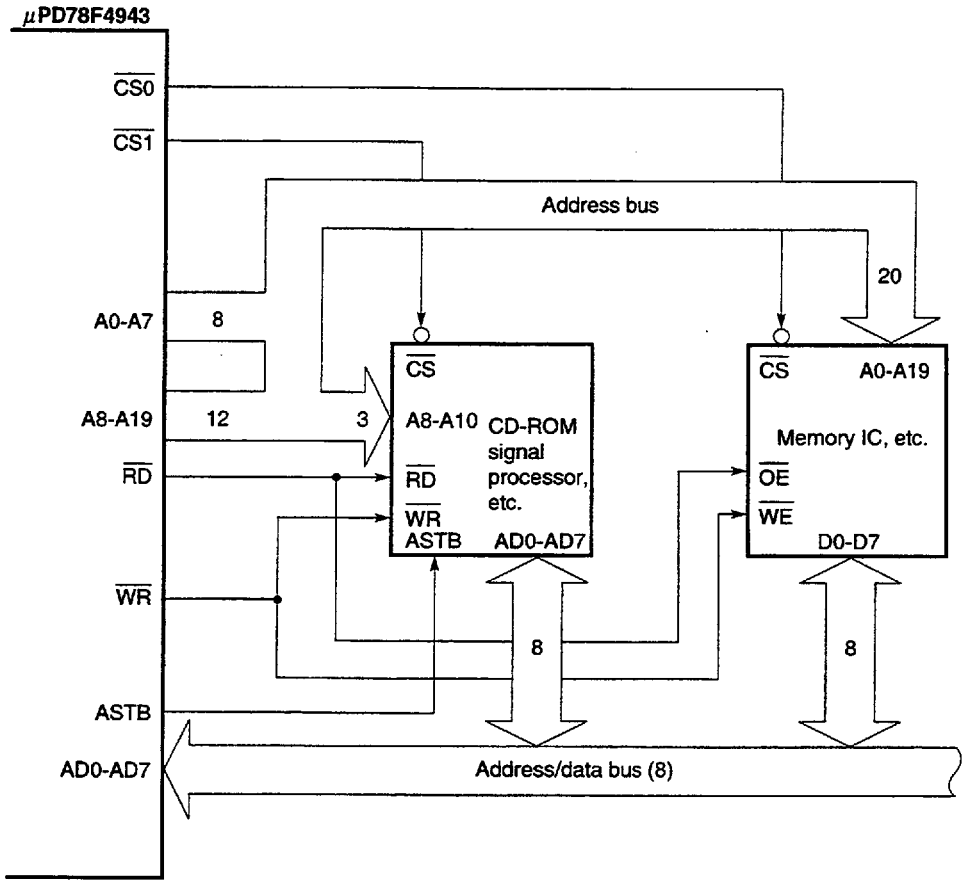


Each time macro service request (INTCSI3) is generated, reception data is transferred from SIO3 to memory. When data n (last byte) has been transferred to memory (that is, once the reception data storage buffer becomes full), vectored interrupt request (INTCSI3) is generated.

8. LOCAL BUS INTERFACE

The local bus interface enables the connection of external memory and I/O devices (memory-mapped I/O). It supports a 1M-byte memory space. (See **Fig. 8-1**.)

Fig. 8-1 Example of Local Bus Interface



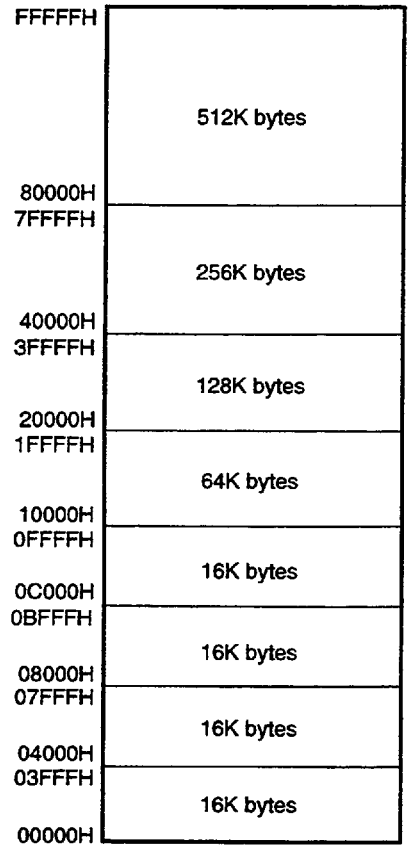
8.1 MEMORY EXPANSION

By adding external memory, program memory or data memory can be expanded, 256 bytes at a time, to approximately 1M byte (seven steps).

8.2 MEMORY SPACE

The 1M-byte memory space is divided into eight spaces, each having a logical address. Each of these spaces can be controlled using the programmable wait and pseudo-static RAM refresh functions.

Fig. 8-2 Memory Space



8.3 PROGRAMMABLE WAIT

When the memory space is divided into eight spaces, a wait state can be separately inserted for each memory space while the $\overline{RD}$ or $\overline{WR}$ signal is active. This prevents the overall system efficiency from being degraded even when memory devices having different access times are connected.

In addition, an address wait function that extends the ASTB signal active period is provided to produce a longer address decode time. (This function is set for the entire space.)

8.4 PSEUDO-STATIC RAM REFRESH FUNCTION

Refresh is performed as follows:

- Pulse refresh : A bus cycle is inserted where a refresh pulse is output on the $\overline{REFRQ}$ pin at regular intervals. When the memory space is divided into eight, and a specified area is being accessed, refresh pulses can also be output on the $\overline{REFRQ}$ pin as the memory is being accessed. This can prevent the refresh cycle from suspending normal memory access.
- Power-down self-refresh : In standby mode, a low-level signal is output on the $\overline{REFRQ}$ pin to maintain the contents of pseudo-static RAM.

8.5 BUS HOLD FUNCTION

A bus hold function is provided to facilitate connection to devices such as a DMA controller. Suppose that a bus hold request signal (HLDRQ) is received from an external bus master. In this case, upon the completion of the bus cycle being performed, the address bus, address/data bus, ASTB, $\overline{RD}$, and $\overline{WR}$ pins are placed in the high-impedance state, and the bus hold acknowledge signal (HLDAK) is made active to release the bus for the external bus master.

While the bus hold function is being used, the external wait and pseudo-static RAM refresh functions are disabled.

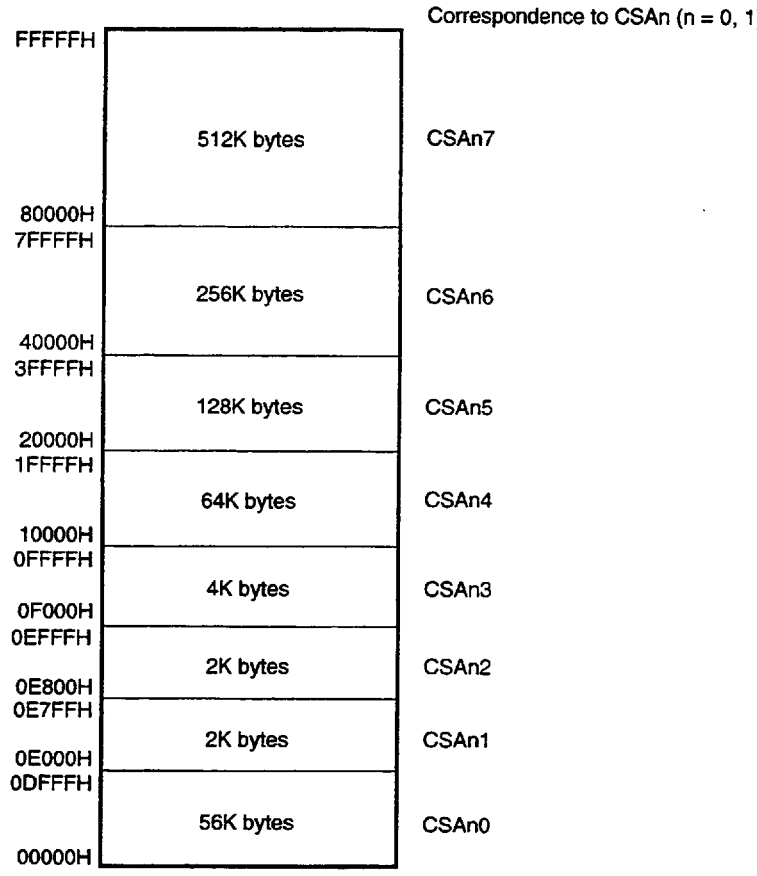
8.6 CHIP SELECT OUTPUT

The $\overline{CS0}$ and $\overline{CS1}$ outputs control the external device. The address decoder which has been configured in the external circuitry can be omitted.

These two chip select outputs can be activated separately for any memory spaces divided into eight spaces shown in Fig. 8-3.

Set the specified data to the 8-bit registers that specify the chip select output space (CSA0 and CSA1) to specify the memory space for which $\overline{CS0}$ or $\overline{CS1}$ is activated.

Fig. 8-3 Memory Space for Chip Select Output



8.7 SEPARATE BUS FUNCTION

Port 0 can be used as 8 low-order bits of the address bus. This function provides an interface to the memory device without adding an address latch externally.

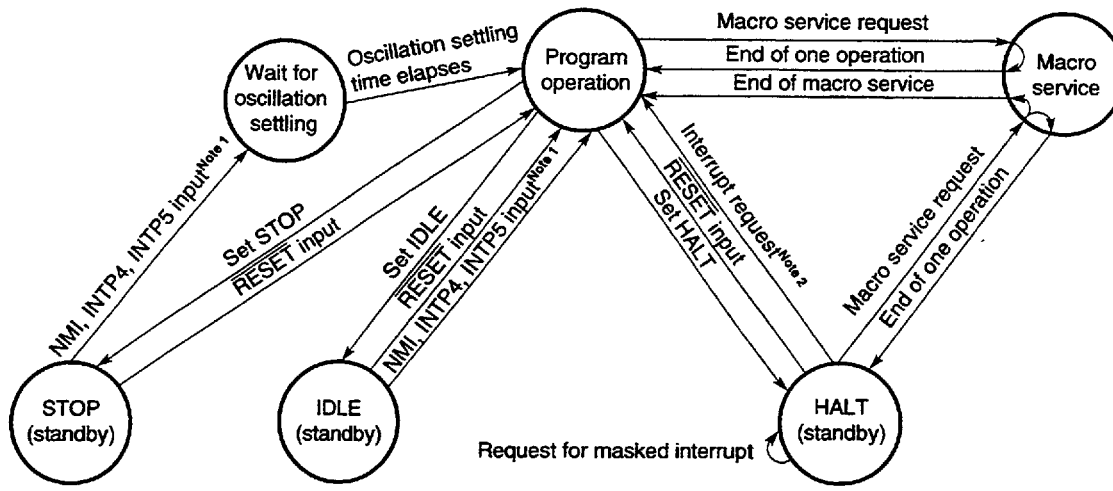
9. STANDBY FUNCTION

The standby function allows the power consumption of the chip to be reduced. The following standby modes are supported:

- HALT mode : The CPU operation clock is stopped. By occassionally inserting the HALT mode during normal operation, the overall average power consumption can be reduced.
- IDLE mode : The entire system is stopped, with the exception of the oscillator circuit. This mode consumes only very little more power than STOP mode, but normal program operation can be restored in almost as little time as that required to restore normal program operation from HALT mode.
- STOP mode: The oscillator is stopped. All operations in the chip stop, such that only leakage current flows.

These modes can be selected by software.
A macro service can be initiated in HALT mode.

Fig. 9-1 Standby Mode Status Transition



Notes 1. INTP4 and INTP5 are applied when not masked.
2. Only when the interrupt request is not masked

Remark NMI is enabled only by external input. The watchdog timer cannot be used to release one of the standby modes (STOP or IDLE mode).

10. RESET FUNCTION

Applying a low-level signal to the $\overline{\text{RESET}}$ pin initializes the internal hardware (reset status).

When the $\overline{\text{RESET}}$ input makes a low-to-high transition, the following data is loaded into the program counter (PC):

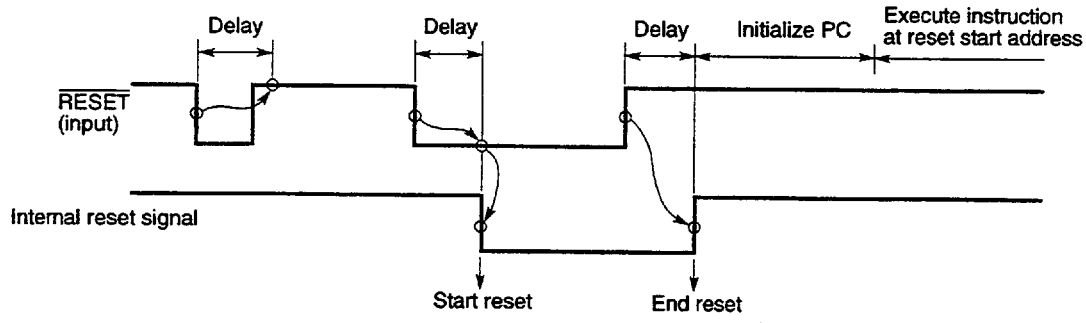
- Eight low-order bits of the PC : Contents of location at address 0000H
- Intermediate eight bits of the PC : Contents of location at address 0001H
- Four high-order bits of the PC : 0

The PC contents are used as a branch destination address. Program execution starts from that address. Therefore, a reset start can be performed from an arbitrary address.

The contents of each register can be set by software, as required.

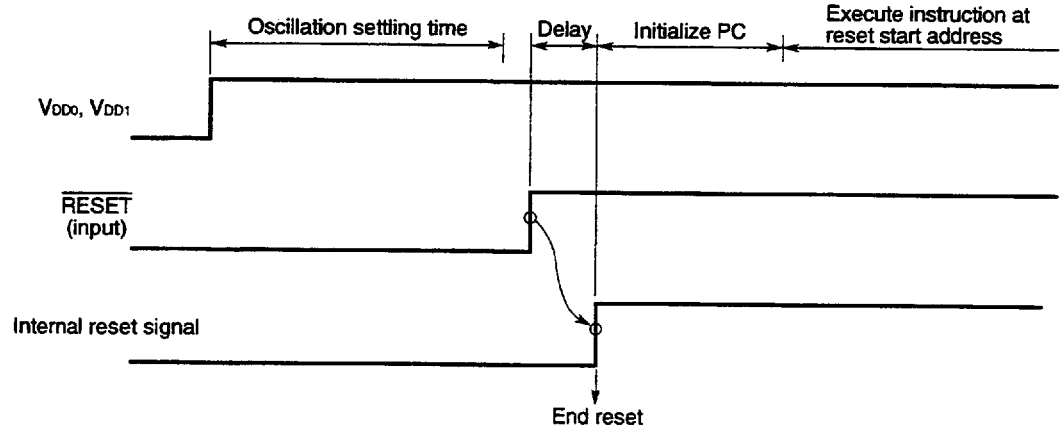
The $\overline{\text{RESET}}$ input circuit contains a noise eliminator to prevent malfunctions caused by noise. This noise eliminator is an analog delay sampling circuit.

Fig. 10-1 Accepting a Reset



For power-on reset, the $\overline{\text{RESET}}$ signal must be held active until the oscillation settling time (approximately 40 ms) has elapsed.

Fig. 10-2 Power-On Reset



11. INSTRUCTION SET

(1) 8-bit instructions (The instructions enclosed in parentheses are implemented by a combination of operands, where A is described as r.)

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, SHR, SHL, ROR4, ROL4, DBNZ, PUSH, POP, MOVM, XCHM, CMPME, CMPMNE, CMPMNC, CMPMC, MOVBK, XCHBK, CMPBKE, CMPBKNE, CMPBKNC, CMPBKC, CHKL, CHKLA

Table 11-1 Instructions Implemented by 8-Bit Addressing

1st operand \ 2nd operand	#byte	A	r r'	saddr saddr'	sfr	!addr16 !!addr24	mem [saddrp] [%saddrg]	r3 PSWL PSWH	[WHL+] [WHL−]	n	None[Note 2]
A	(MOV) ADD[Note 1]	(MOV) (XCH) (ADD)[Note 1]	MOV XCH (ADD)[Note 1]	(MOV)[Note 6] (XCH)[Note 6] (ADD)[Notes 1, 6]	MOV (XCH) (ADD)[Note 1]	(MOV) (XCH) ADD[Note 1]	MOV XCH ADD[Note 1]	MOV	(MOV) (XCH) (ADD)[Note 1]		
r	MOV ADD[Note 1]	(MOV) (XCH) (ADD)[Note 1]	MOV XCH ADD[Note 1]	MOV XCH ADD[Note 1]	MOV XCH ADD[Note 1]	MOV XCH				ROR[Note 3]	MULU DIVUW INC DEC
saddr	MOV ADD[Note 1]	(MOV)[Note 6] (ADD)[Note 1]	MOV ADD[Note 1]	MOV XCH ADD[Note 1]							INC DEC DBNZ
sfr	MOV ADD[Note 1]	MOV (ADD)[Note 1]	MOV ADD[Note 1]								PUSH POP CHKL CHKLA
!addr16 !!addr24	MOV	(MOV) ADD[Note 1]	MOV								
mem [saddrp] [%saddrg]		MOV ADD[Note 1]									
mem3											ROR4 ROL4
r3 PSWL PSWH	MOV	MOV									
B, C											DBNZ
STBC, WDM	MOV										
[TDE+] [TDE−]		(MOV) (ADD)[Note 1] MOVM[Note 4]							MOVBK[Note 5]		

Notes 1. ADDC, SUB, SUBC, AND, OR, XOR, and CMP are the same as ADD.

2. There is no second operand, or the second operand is not an operand address.

3. ROL, RORC, ROLC, SHR, and SHL are the same as ROR.

4. XCHM, CMPME, CMPMNE, CMPMNC, and CMPMC are the same as MOVM.

5. XCHBK, CMPBKE, CMPBKNE, CMPBKNC, and CMPBKC are the same as MOVBK.

6. When saddr is saddr2 with this combination, an instruction with a short code exists.

(2) 16-bit instructions (The instructions enclosed in parentheses are implemented by a combination of operands, where AX is described as rp.)

MOVW, XCHW, ADDW, SUBW, CMPW, MULUW, MULW, DIVUX, INCW, DECW, SHRW, SHLW, PUSH, POP, ADDWG, SUBWG, PUSHU, POPU, MOVTBLW, MACW, MACSW, SACW

Table 11-2 Instructions Implemented by 16-Bit Addressing

1st operand \ 2nd operand	#word	AX	rp rp'	saddrp saddrp'	sfrp	!addr16 !!addr24	mem [saddrp] [%saddrg]	[WHL+]	byte	n	None[Note 2]
AX	(MOVW) ADDW[Note 1]	(MOVW) (XCHW) (ADD)[Note 1]	(MOVW) (XCHW) (ADDW)[Note 1]	(MOVW)[Note 3] (XCHW)[Note 3] (ADDW)[Notes 1,3]	MOVW (XCHW) (ADDW)[Note 1]	(MOVW) XCHW	MOVW XCHW	(MOVW) (XCHW)			
rp	MOVW ADDW[Note 1]	(MOVW) (XCHW) (ADDW)[Note 1]	MOVW XCHW ADDW[Note 1]	MOVW XCHW ADDW[Note 1]	MOVW XCHW ADDW[Note 1]	MOVW				SHRW SHLW	MULW[Note 4] INCW DECW
saddrp	MOVW ADDW[Note 1]	(MOVW)[Note 3] (ADDW)[Note 1]	MOVW ADDW[Note 1]	MOVW XCHW ADDW[Note 1]							INCW DECW
sfrp	MOVW ADDW[Note 1]	MOVW (ADDW)[Note 1]	MOVW ADDW[Note 1]								PUSH POP
!addr16 !!addr24	MOVW	(MOVW)	MOVW						MOVTBLW		
mem [saddrp] [%saddrg]		MOVW									
PSW											PUSH POP
SP	ADDWG SUBWG										
post											PUSH POP PUSHU POPU
[TDE+]		(MOVW)						SACW			
byte											MACW MACSW

Notes 1. SUBW and CMPW are the same as ADDW.

2. There is no second operand, or the second operand is not an operand address.

3. When saddrp is saddrp2 with this combination, an instruction with a short code exists.

4. MULUW and DIVUX are the same as MULW.

(3) 24-bit instructions (The instructions enclosed in parentheses are implemented by a combination of operands, where WHL is described as rg.)

MOVG, ADDG, SUBG, INCG, DECG, PUSH, POP

Table 11-3 Instructions Implemented by 24-Bit Addressing

1st operand \ 2nd operand	#imm24	WHL	rg rg'	saddrg	!!addr24	mem1	[%saddrg]	SP	None[Note]
WHL	(MOVG) (ADDG) (SUBG)	(MOVG) (ADDG) (SUBG)	(MOVG) (ADDG) (SUBG)	(MOVG) ADDG SUBG	(MOVG)	MOVG	MOVG	MOVG	
rg	MOVG ADDG SUBG	(MOVG) (ADDG) (SUBG)	MOVG ADDG SUBG	MOVG	MOVG				INCG DECG PUSH POP
saddrg		(MOVG)	MOVG						
!!addr24		(MOVG)	MOVG						
mem1		MOVG							
[%saddrg]		MOVG							
SP	MOVG	MOVG							INCG DECG

Note There is no second operand, or the second operand is not an operand address.

(4) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR, BFSET

Table 11-4 Bit Manipulation Instructions Implemented by Addressing

2nd operand / 1st operand	CY	saddr.bit sfr.bit A.bit X.bit PSWL.bit PSWH.bit mem2.bit !addr16.bit !!addr24.bit	/saddr.bit /sfr.bit /A.bit /X.bit /PSWL.bit /PSWH.bit /mem2.bit /!addr16.bit /!!addr24.bit	None[Note]
CY		MOV1 AND1 OR1 XOR1	AND1 OR1	NOT1 SET1 CLR1
saddr.bit sfr.bit A.bit X.bit PSWL.bit PSWH.bit mem2.bit !addr16.bit !!addr24.bit	MOV1			NOT1 SET1 CLR1 BF BT BTCLR BFSET

Note There is no second operand, or the second operand is not an operand address.

(5) Call/return instructions and branch instructions

CALL, CALLF, CALLT, BRK, RET, RETI, RETB, RETCS, RETCSB, BRKCS, BR, BNZ, BNE, BZ, BE, BNC, BNL, BC, BL, BNV, BPO, BV, BPE, BP, BN, BLT, BGE, BLE, BGT, BNH, BH, BF, BT, BTCLR, BFSET, DBNZ

Table 11-5 Call/Return and Branch Instructions Implemented by Addressing

Instruction address operand	$addr20	$!addr20	!addr16	!!addr20	rp	rg	[rp]	[rg]	!addr11	[addr5]	RBn	None
Basic instruction	BC[Note] BR	CALL BR	CALL BR RETCS RETCSB	CALL BR	CALL BR	CALL BR	CALL BR	CALL BR	CALLF	CALLF	BRKCS	BRK RET RETI RETB
Composite instruction	BF BT BTCLR BFSET DBNZ											

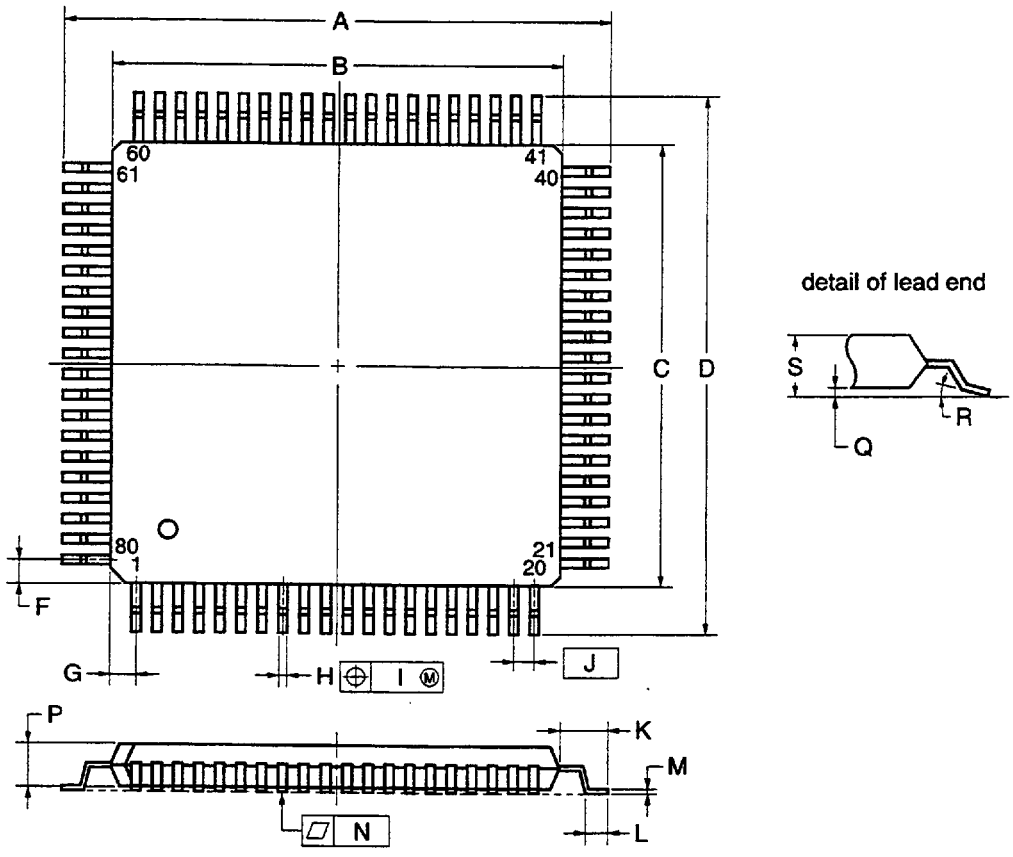
Note BNZ, BNE, BZ, BE, BNC, BNL, BL, BNV, BPO, BV, BPE, BP, BN, BLT, BGE, BLE, BGT, BNH, and BH are the same as BC.

(6) Other instructions

ADJBA, ADJBS, CVTBW, LOCATION, SEL, NOT, EI, DI, SWRS

12. PACKAGE DRAWINGS

80 PIN PLASTIC QFP (14×14)



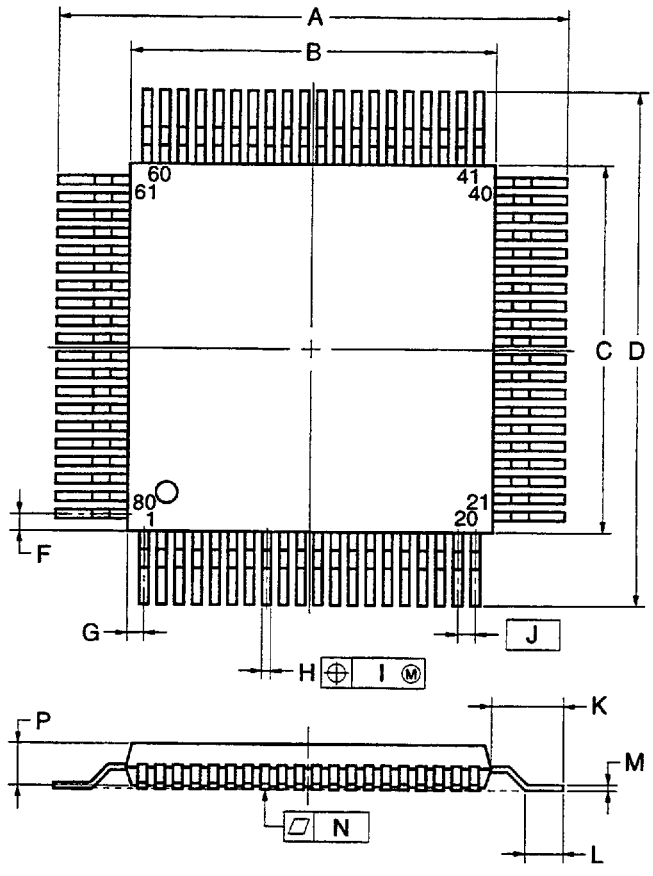
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

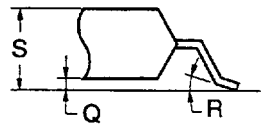
ITEM	MILLIMETERS	INCHES
A	17.20±0.20	0.677±0.008
B	14.00±0.20	$0.551^{+0.009}_{-0.008}$
C	14.00±0.20	$0.551^{+0.009}_{-0.008}$
D	17.20±0.20	0.677±0.008
F	0.825	0.032
G	0.825	0.032
H	0.32±0.06	$0.013^{+0.002}_{-0.003}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.60±0.20	0.063±0.008
L	0.80±0.20	$0.031^{+0.009}_{-0.008}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.10	0.004
P	1.40±0.10	0.055±0.004
Q	0.125±0.075	0.005±0.003
R	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$
S	1.70 MAX.	0.067 MAX.

P80GC-65-8BT

80 PIN PLASTIC QFP (14×14)



detail of lead end



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.4	0.677±0.016
F	0.825	0.032
G	0.825	0.032
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

S80GC-65-3B9-4

APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78F4943.

Language Processing Software

RA78K4[Note 1]	Assembler package for all 78K/IV series models
CC78K4[Note 1]	C compiler package for all 78K/IV series models
CC78K4-L[Note 1]	C compiler library source file for all 78K/IV series models

Flash Memory Write Tools

Flashpro	Dedicated flash writer. The Flashpro is a product from NAITO DENSEI MACHIDA SEISAKUSHO CO., LTD.

Debugging Tools

IE-784000-R	In-circuit emulator for all 78K/IV series models
IE-784000-R-BK	Break board for all 78K/IV series models
IE-784943-R-EM1 IE-784000-R-EM	Emulation board for evaluating μPD78F4943 sub-series models
IE-70000-98-IF-B	Interface adapter when the PC-9800 series computer (other than a notebook) is used as the host machine
IE-70000-98N-IF	Interface adapter and cable when a PC-9800 series notebook is used as the host machine
IE-70000-PC-IF-B	Interface adapter when the IBM PC/AT™ is used as the host machine
IE-78000-R-SV3	Interface adapter and cable when the EWS is used as the host machine
EP-78230GC-R	Emulation probe for 80-pin plastic QFP (GC-8BT and GC-3B9 types) for all μPD78F4943 sub-series
EV-9200GC-80	Socket for mounting on target system board made for 80-pin plastic QFP (GC-8BT and GC-3B9 types)
SM78K4[Note 3]	System simulator for all 78K/IV series models
ID78K4[Note 3]	Integrated debugger for IE-784000-R
DF784943[Note 4]	Device file for all μPD78F4943 sub-series models

Real-time OS

RX78K/IV[Note 4]	Real-time OS for 78K/IV series models
MX78K4[Note 2]	OS for all 78K/IV series models

Remark The RA78K4, CC78K4, SM78K4, and ID78K4 are used with the DF784943.

Notes 1. • Based on PC-9800 series (MS-DOS™)
- Based on IBM PC/AT and compatibles (PC DOS™, Windows™, MS-DOS, and IBM DOS™)
- Based on HP9000 series 700™ (HP-UX™)
- Based on SPARCstation™ (SunOS™)
- Based on NEWS™ (NEWS-OS™)

2. • Based on PC-9800 series (MS-DOS)
- Based on IBM PC/AT and compatibles (PC DOS, Windows, MS-DOS, and IBM DOS)

3. • Based on PC-9800 series (MS-DOS + Windows)
- Based on IBM PC/AT and compatibles (PC DOS, Windows, MS-DOS, and IBM DOS)
- Based on HP9000 series 700 (HP-UX)
- Based on SPARCstation (SunOS)

4. • Based on PC-9800 series (MS-DOS)
- Based on IBM PC/AT and compatibles (PC DOS, Windows, MS-DOS, and IBM DOS)
- Based on HP9000 series 700 (HP-UX)
- Based on SPARCstation (SunOS)

APPENDIX B RELATED DOCUMENTS

Documents Related to Devices

Document name	Document No.	
	Japanese	English
μPD78F4943 Preliminary Product Information	U11783J	This manual
μPD78F4943 Sub-Series User's Manual, Hardware	To be released soon	To be created
μPD78F4943 Sub-Series Special Function Registers	U11782J	—
78K/IV Series User's Manual, Instruction	U10905J	U10905E
78K/IV Series Instruction Summary Sheet	U10594J	—
78K/IV Series Instruction Set	U10595J	—
78K/IV Series Application Note, Software Basic	U10095J	—

Documents Related to Development Tools (User's Manual)

Document name		Document No.	
		Japanese	English
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
CC78K Series Library Source File		EEU-777	—
PG-1500 PROM Programmer		EEU-651	EEU-1335
PG-1500 Controller PC-9800 Series (MS-DOS) Base		EEU-704	EEU-1291
PG-1500 Controller IBM PC Series (PC DOS) Base		EEU-5008	U10540E
IE-784000-R		EEU-5004	EEU-1534
IE-784943-R-EM1		To be created	—
EP-78230		EEU-985	EEU-1515
SM78K4 System Simulator Windows Base	Reference	U10093J	U10093E
SM78K Series System Simulator	External Parts User Open Interface Specifications	U10092J	U10092E
ID78K4 Integrated Debugger	Reference	U10440J	U10440E

Caution The above documents may be revised without notice. Use the latest versions when you design application systems.

Documents Related to Software to Be Incorporated into the Product (User's Manual)

Document name		Document No.	
		Japanese	English
78K/IV Series Real-Time OS	Basic	U10603J	—
	Installation	U10604J	—
	Debugger	U10364J	—
OS for 78K/IV Series MX78K4		To be created	—

Other Documents

Document name	Document No.	
	Japanese	English
IC Package Manual	C10943X	
SMD Surface Mount Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Device	IEI-620	IEI-1209
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Electrostatic Discharge (ESD) Test	MEM-539	—
Guide to Quality Assurance for Semiconductor Device	MEI-603	MEI-1202
Guide for Products Related to Micro-Computer: Other Companies	MEI-604	—

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